

74LVT574 • 74LVTH574

Low Voltage Octal D-Type Flip-Flop with 3-STATE Outputs

General Description

The LVT574 and LVTH574 are high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

The LVTH574 data inputs include bushhold, eliminating the need for external pull-up resistors to hold unused inputs.

These octal flip-flops are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT574 and LVTH574 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

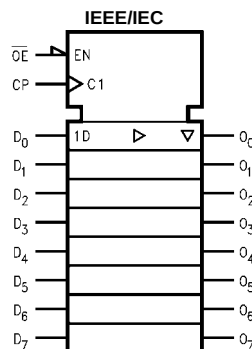
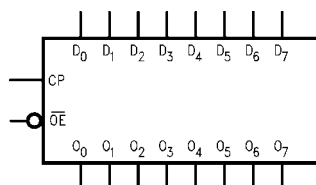
- Input and output interface capability to systems at 5V V_{CC}
- Bushhold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH574), also available without bushhold feature (74LVT574).
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink $-32\text{ mA}/+64\text{ mA}$
- Functionally compatible with the 74 series 574
- Latch-up performance exceeds 500 mA

Ordering Code:

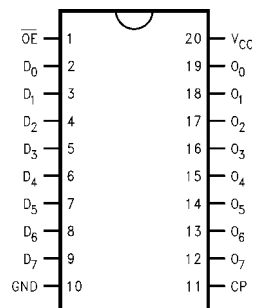
Order Number	Package Number	Package Description
74LVT574WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, .300" Wide
74LVT574SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II 5.3mm Wide
74LVT574MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74LVT574MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74LVTH574WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, .300" Wide
74LVTH574SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II 5.3mm Wide
74LVTH574MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74LVTH574MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Pin Descriptions

Pin Names	Description
D ₀ –D ₇	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-STATE Output Enable Input
O ₀ –O ₇	3-STATE Outputs

Truth Table

Inputs			Outputs
D _n	CP	$\overline{OE}$	O _n
H	↗	L	H
L	↗	L	L
X	L	L	O ₀
X	X	H	Z

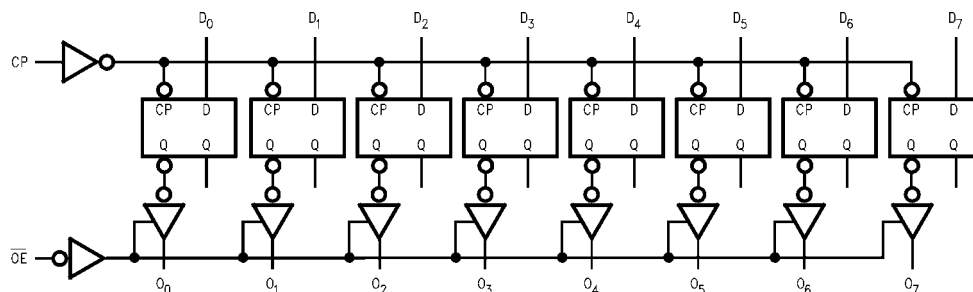
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 ↗ = LOW-to-HIGH Transition
 O₀ = Previous O₀ before HIGH to LOW of CP

Functional Description

The LVT574 and LVTH574 consist of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D-type inputs that meet the setup and hold time requirements on the LOW-to-HIGH

Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings ^(Note 1)						
Symbol	Parameter	Value	Conditions	Units		
V_{CC}	Supply Voltage	−0.5 to +4.6		V		
V_I	DC Input Voltage	−0.5 to +7.0		V		
V_O	DC Output Voltage	−0.5 to +7.0	Output in 3-STATE	V		
		−0.5 to +7.0	Output in High or Low State (Note 2)			
I_{IK}	DC Input Diode Current	−50	$V_I < \text{GND}$	mA		
I_{OK}	DC Output Diode Current	−50	$V_O < \text{GND}$	mA		
I_O	DC Output Current	64	$V_O > V_{CC}$ Output at High State	mA		
		128	$V_O > V_{CC}$ Output at Low State			
I_{CC}	DC Supply Current per Supply Pin	±64		mA		
I_{GND}	DC Ground Current per Ground Pin	±128		mA		
T_{STG}	Storage Temperature	−65 to +150		°C		

Recommended Operating Conditions					
Symbol	Parameter	Min	Max	Units	
V_{CC}	Supply Voltage	2.7	3.6	V	
V_I	Input Voltage	0	5.5	V	
I_{OH}	High-Level Output Current		−32	mA	
I_{OL}	Low-Level Output Current		64	mA	
T_A	Free-Air Operating Temperature	−40	85	°C	
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V\text{--}2.0V$, $V_{CC} = 3.0V$	0	10	ns/V	

Note 1: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 2: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics						
Symbol	Parameter	V_{CC} (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			Conditions
			Min	Typ (Note 3)	Max	
V_{IK}	Input Clamp Diode Voltage	2.7			−1.2	$I_I = -18\text{ mA}$
V_{IH}	Input HIGH Voltage	2.7–3.6	2.0			$V_O \leq 0.1V$ or $V_O \geq V_{CC} - 0.1V$
V_{IL}	Input LOW Voltage	2.7–3.6			0.8	
V_{OH}	Output HIGH Voltage	2.7–3.6	$V_{CC} - 0.2$			$I_{OH} = -100\text{ }\mu\text{A}$
		2.7	2.4			$I_{OH} = -8\text{ mA}$
		3.0	2.0			$I_{OH} = -32\text{ mA}$
V_{OL}	Output LOW Voltage	2.7			0.2	$I_{OL} = 100\text{ }\mu\text{A}$
		2.7			0.5	$I_{OL} = 24\text{ mA}$
		3.0			0.4	$I_{OL} = 16\text{ mA}$
		3.0			0.5	$I_{OL} = 32\text{ mA}$
		3.0			0.55	$I_{OL} = 64\text{ mA}$
$I_{I(HOLD)}$ (Note 4)	Bushold Input Minimum Drive	3.0	75			$V_I = 0.8V$
			−75			$V_I = 2.0V$
$I_{I(OD)}$ (Note 4)	Bushold Input Over-Drive Current to Change State	3.0	500			(Note 5)
			−500			(Note 6)
I_I	Input Current	3.6			10	$V_I = 5.5V$
		Control Pins	3.6		±1	$V_I = 0V$ or V_{CC}
		Data Pins	3.6		−5	$V_I = 0V$
					1	$V_I = V_{CC}$
I_{OFF}	Power Off Leakage Current	0			±100	$0V \leq V_I$ or $V_O \leq 5.5V$
$I_{PUI/PD}$	Power up/down 3-STATE	0–1.5V			±100	$V_O = 0.5V$ to $3.0V$
	Output Current					$V_I = \text{GND}$ or V_{CC}
I_{OZL}	3-STATE Output Leakage Current	3.6			−5	$V_O = 0.5V$
I_{OZH}	3-STATE Output Leakage Current	3.6			5	$V_O = 3.0V$

DC Electrical Characteristics (Continued)

Symbol	Parameter	V _{CC} (V)	T _A = -40°C to +85°C			Units	Conditions
			Min	Typ (Note 3)	Max		
I _{OZH} ⁺	3-STATE Output Leakage Current	3.6			10	μA	V _{CC} < V _O ≤ 5.5V
I _{CCH}	Power Supply Current	3.6			0.19	mA	Outputs High
I _{CCL}	Power Supply Current	3.6			5	mA	Outputs Low
I _{CCZ}	Power Supply Current	3.6			0.19	mA	Outputs Disabled
I _{CCZ} ⁺	Power Supply Current	3.6			0.19	mA	V _{CC} ≤ V _O ≤ 5.5V, Outputs Disabled
ΔI _{CC}	Increase in Power Supply Current (Note 7)	3.6			0.2	mA	One Input at V _{CC} – 0.6V Other Inputs at V _{CC} or GND

Note 3: All typical values are at V_{CC} = 3.3V, T_A = 25°C.

Note 4: Applies to bushold versions only (74LVTH574).

Note 5: An external driver must source at least the specified current to switch from LOW to HIGH.

Note 6: An external driver must sink at least the specified current to switch from HIGH to LOW.

Note 7: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 8)

Symbol	Parameter	V _{CC} (V)	T _A = 25°C			Units	Conditions C _L = 50 pF, R _L = 500Ω
			Min	Typ	Max		
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3		0.8		V	(Note 9)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3		–0.8		V	(Note 9)

Note 8: Characterized in SOIC package. Guaranteed parameter, but not tested.

Note 9: Max number of outputs defined as (n). n–1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Symbol	Parameter	T _A = -40°C to +85°C C _L = 50 pF, R _L = 500Ω					Units
		V _{CC} = 3.3V ±0.3V			V _{CC} = 2.7V		
		Min	Typ (Note 10)	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	150			150		MHz
t _{PHL}	Propagation Delay	1.8		4.6	1.8	5.3	ns
t _{PLH}	CP to O _n	1.8		4.5	1.8	5.3	
t _{PZL}	Output Enable Time	1.5		5.2	1.5	6.1	ns
t _{PZH}		1.5		4.8	1.5	5.9	
t _{PLZ}	Output Disable Time	2.0		4.4	2.0	4.4	ns
t _{PHZ}		2.0		4.8	2.0	5.1	
t _S	Setup Time	2.0			2.4		ns
t _H	Hold Time	0.3			0.0		ns
t _W	Pulse Width	3.3			3.3		ns
t _{OSHL}	Output to Output Skew (Note 11)			1.0		1.0	ns
t _{OSLH}				1.0		1.0	

Note 10: All typical values are at V_{CC} = 3.3V, T_A = 25°C.

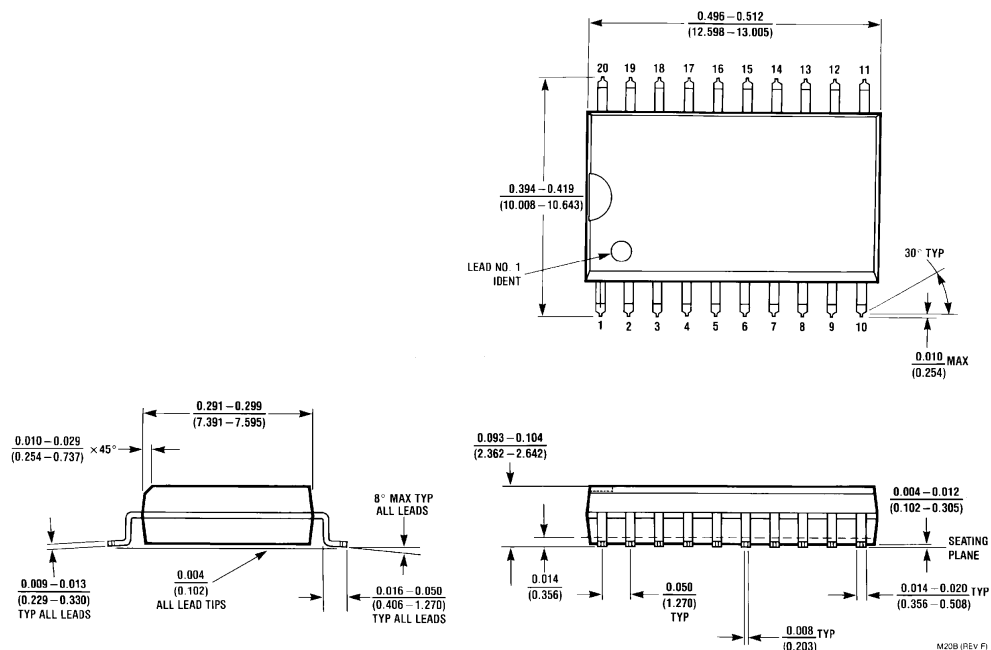
Note 11: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Capacitance (Note 12)

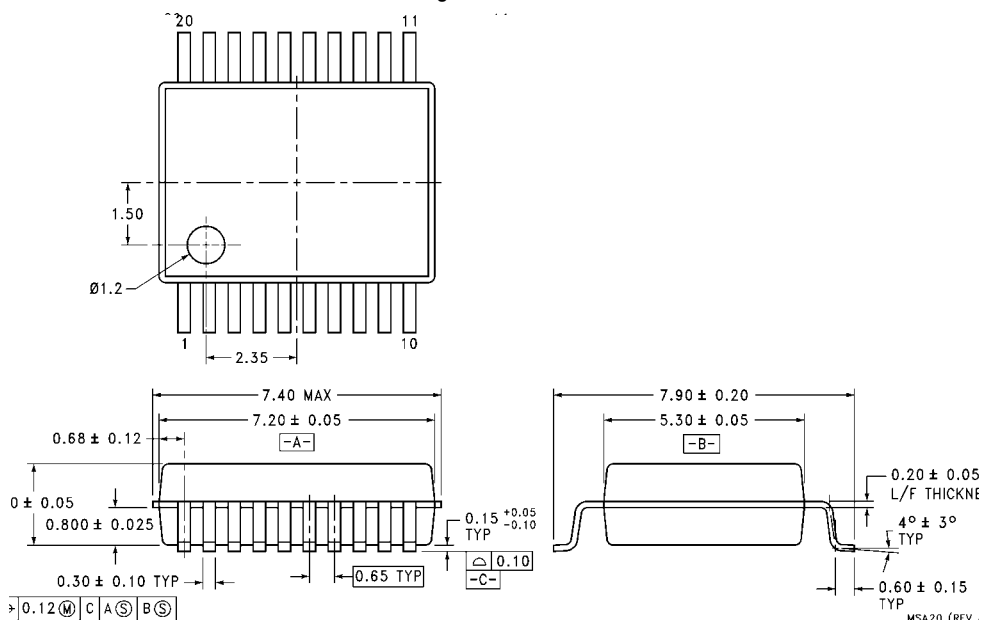
Symbol	Parameter	Conditions	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = Open, V _I = 0V or V _{CC}	4	pF
C _{OUT}	Output Capacitance	V _{CC} = 3.0V, V _O = 0V or V _{CC}	6	pF

Note 12: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted

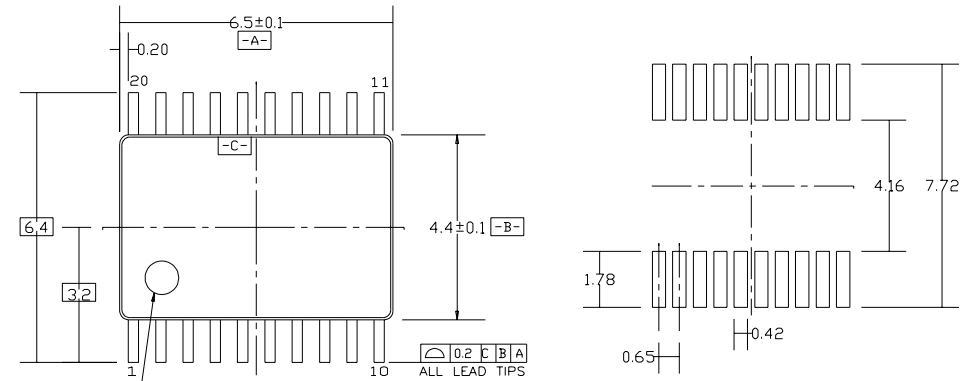


20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, .300" Wide Package Number M20B

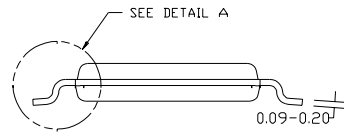
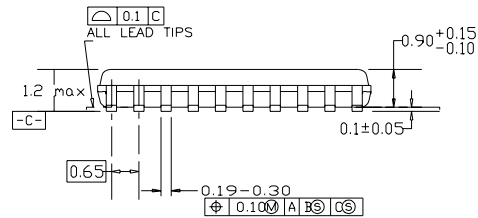


20-Lead Small Outline Package (SOP), EIAJ TYPE II 5.3mm Wide Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



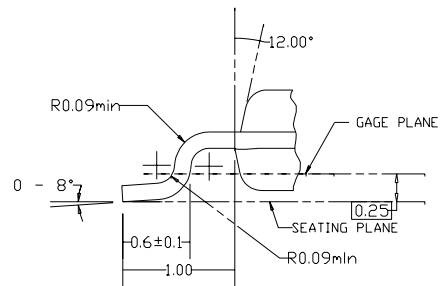
LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

NOTES:

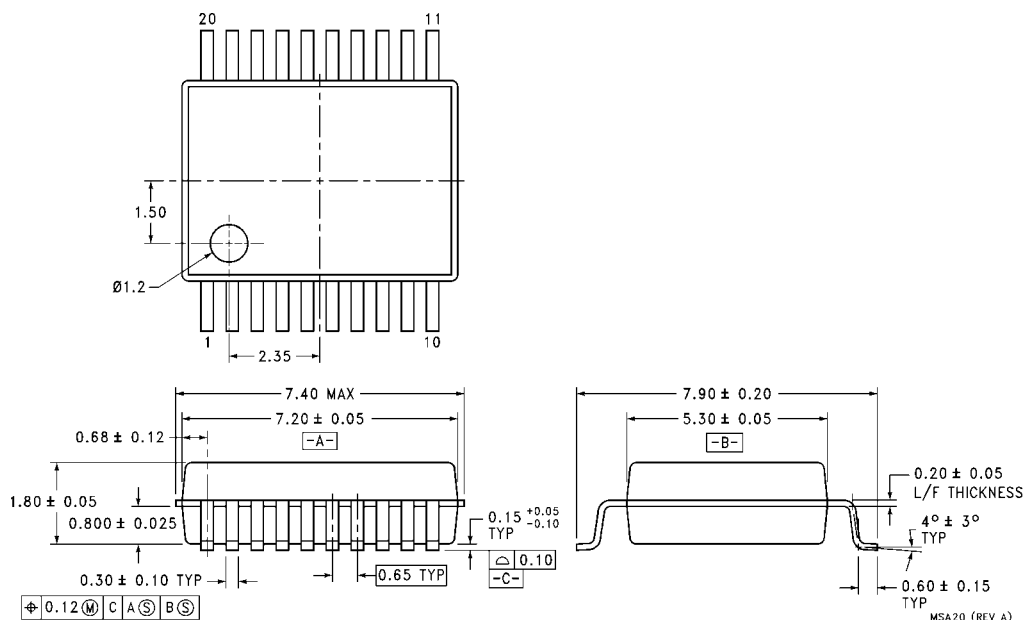
- CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.



DETAIL A

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA20

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