

## 74VCX162240

### Low Voltage 16-Bit Inverting Buffer/Line Driver with 3.6V Tolerant Inputs and Outputs and 26Ω Series Resistors in Outputs

#### General Description

The VCX162240 contains sixteen inverting buffers with 3-STATE outputs to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble (4-bit) controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

The 74VCX162240 is designed for low voltage (1.65V to 3.6V)  $V_{CC}$  applications with I/O capability up to 3.6V. The 74VCX162240 is also designed with 26Ω series resistors in the outputs. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The 74VCX162240 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

#### Features

- 1.65V–3.6V  $V_{CC}$  supply operation
- 3.6V tolerant inputs and outputs
- 26Ω series resistors in outputs
- $t_{PD}$ 
  - 3.3 ns max for 3.0V to 3.6V  $V_{CC}$
  - 3.8 ns max for 2.3V to 2.7V  $V_{CC}$
  - 7.6 ns max for 1.65V to 1.95V  $V_{CC}$
- Power-off high impedance inputs and outputs
- Supports live insertion and withdrawal (Note 1)
- Static Drive ( $I_{OH}/I_{OL}$ )
  - ±12 mA @ 3.0V  $V_{CC}$
  - ±8 mA @ 2.3V  $V_{CC}$
  - ±3 mA @ 1.65V  $V_{CC}$
- Uses patented noise/EMI reduction circuitry
- Latch-up performance exceeds 300 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V

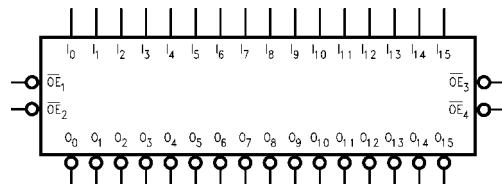
**Note 1:** To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

#### Ordering Code:

Order Number	Package Number	Package Descriptions
74VCX162240MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JECED MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

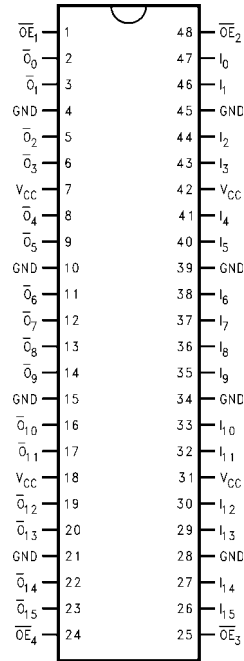
#### Logic Symbol



#### Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$I_0$ – $I_{15}$	Inputs
$\overline{O}_0$ – $\overline{O}_{15}$	Outputs

**Connection Diagram**



**Truth Tables**

Inputs		Outputs
$\overline{OE}_1$	$I_0-I_3$	$\overline{O}_0-\overline{O}_3$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	$I_4-I_7$	$\overline{O}_4-\overline{O}_7$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	$I_8-I_{11}$	$\overline{O}_8-\overline{O}_{11}$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	$I_{12}-I_{15}$	$\overline{O}_{12}-\overline{O}_{15}$
L	L	H
L	H	L
H	X	Z

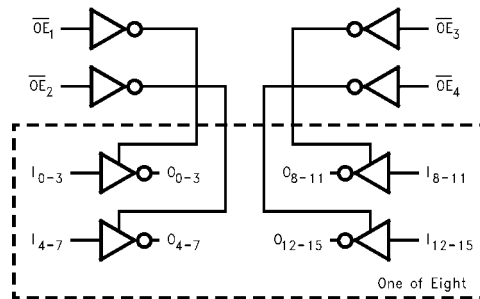
H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial (HIGH or LOW, inputs may not float)  
 Z = High Impedance

**Functional Description**

The 74VCX162240 contains sixteen inverting buffers with 3-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of each other. The control pins may be shorted together to obtain full 16-bit operation. The 3-STATE outputs are controlled by an Output Enable ( $\overline{OE}_n$ ) input. When  $\overline{OE}_n$  is LOW, the outputs are in the 2-state mode. When  $\overline{OE}_n$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the inputs.

When  $\overline{OE}_n$  is LOW, the outputs are in the 2-state mode. When  $\overline{OE}_n$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the inputs.

**Logic Diagram**



**Absolute Maximum Ratings** (Note 2)

Supply Voltage ( $V_{CC}$ )	-0.5V to +4.6V
DC Input Voltage ( $V_I$ )	-0.5V to +4.6V
Output Voltage ( $V_O$ )	
Outputs 3-STATED	-0.5V to +4.6V
Outputs Active (Note 3)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0V$	-50 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O < 0V$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	$\pm 50$ mA
DC $V_{CC}$ or GND Current per Supply Pin ( $I_{CC}$ or GND)	$\pm 100$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

**Recommended Operating Conditions** (Note 4)

Power Supply	
Operating	1.65V to 3.6V
Data Retention Only	1.2V to 3.6V
Input Voltage	-0.3V to +3.6V
Output Voltage ( $V_O$ )	
Output in Active States	0V to $V_{CC}$
Output in 3-State	0.0V to 3.6V
Output Current in $I_{OH}/I_{OL}$	
$V_{CC} = 3.0V$ to 3.6V	$\pm 12$ mA
$V_{CC} = 2.3V$ to 2.7V	$\pm 8$ mA
$V_{CC} = 1.65V$ to 2.3V	$\pm 3$ mA
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

**Note 2:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 3:**  $I_O$  Absolute Maximum Rating must be observed.

**Note 4:** Floating or unused inputs must be held HIGH or LOW.

**DC Electrical Characteristics (2.7V <  $V_{CC}$  ≤ 3.6V)**

Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units
$V_{IH}$	HIGH Level Input Voltage		2.7 – 3.6	2.0		V
$V_{IL}$	LOW Level Input Voltage		2.7 – 3.6		0.8	V
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.7 – 3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -6 \text{ mA}$	2.7	2.2		V
		$I_{OH} = -8 \text{ mA}$	3.0	2.4		V
		$I_{OH} = -12 \text{ mA}$	3.0	2.2		V
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.7 – 3.6		0.2	V
		$I_{OL} = 6 \text{ mA}$	2.7		0.4	V
		$I_{OL} = 8 \text{ mA}$	3.0		0.55	V
		$I_{OL} = 12 \text{ mA}$	3.0		0.80	V
$I_I$	Input Leakage Current	$0 \leq V_I \leq 3.6V$	2.7 – 3.6		$\pm 5.0$	$\mu A$
$I_{OZ}$	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ $V_I = V_{IH}$ or $V_{IL}$	2.7 – 3.6		$\pm 10$	$\mu A$
$I_{OFF}$	Power-OFF Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$	0		10	$\mu A$
$I_{CC}$	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.7 – 3.6		20	$\mu A$
		$V_{CC} \leq (V_I, V_O) \leq 3.6V$ (Note 5)	2.7 – 3.6		$\pm 20$	$\mu A$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	$V_{IH} = V_{CC} - 0.6V$	2.7 – 3.6		750	$\mu A$

**Note 5:** Outputs disabled or 3-STATE only.

### DC Electrical Characteristics ( $2.3V \leq V_{CC} \leq 2.7V$ )

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	Min	Max	Units
V <sub>IH</sub>	HIGH Level Input Voltage		2.3 - 2.7	1.6		V
V <sub>IL</sub>	LOW Level Input Voltage		2.3 - 2.7		0.7	V
V <sub>OH</sub>	HIGH Level Output Voltage	I <sub>OH</sub> = -100 μA	2.3 - 2.7	V <sub>CC</sub> - 0.2		V
		I <sub>OH</sub> = -4 mA	2.3	2.0		V
		I <sub>OH</sub> = -6 mA	2.3	1.8		V
		I <sub>OH</sub> = -8 mA	2.3	1.7		V
V <sub>OL</sub>	LOW Level Output Voltage	I <sub>OL</sub> = 100 μA	2.3 - 2.7		0.2	V
		I <sub>OL</sub> = 6 mA	2.3		0.4	V
		I <sub>OL</sub> = 8 mA	2.3		0.6	V
I <sub>I</sub>	Input Leakage Current	0 ≤ V <sub>I</sub> ≤ 3.6V	2.3 - 2.7		±5.0	μA
I <sub>OZ</sub>	3-STATE Output Leakage	0 ≤ V <sub>O</sub> ≤ 3.6V V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.3 - 2.7		±10	μA
I <sub>OFF</sub>	Power-OFF Leakage Current	0 ≤ (V <sub>I</sub> , V <sub>O</sub> ) ≤ 3.6V	0		10	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND	2.3 - 2.7		20	μA
		V <sub>CC</sub> ≤ (V <sub>I</sub> , V <sub>O</sub> ) ≤ 3.6V (Note 6)	2.3 - 2.7		±20	μA

Note 6: Outputs disabled or 3-STATE only.

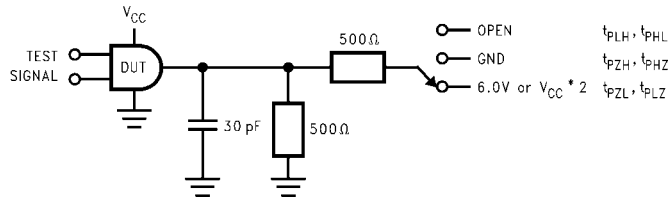
### DC Electrical Characteristics ( $1.65V \leq V_{CC} < 2.3V$ )

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	Min	Max	Units
V <sub>IH</sub>	HIGH Level Input Voltage		1.65 - 2.3	0.65 × V <sub>CC</sub>		V
V <sub>IL</sub>	LOW Level Input Voltage		1.65 - 2.3		0.35 × V <sub>CC</sub>	V
V <sub>OH</sub>	HIGH Level Output Voltage	I <sub>OH</sub> = -100 μA	1.65 - 2.3	V <sub>CC</sub> - 0.2		V
		I <sub>OH</sub> = -3 mA	1.65	1.25		V
V <sub>OL</sub>	LOW Level Output Voltage	I <sub>OL</sub> = 100 μA	1.65 - 2.3		0.2	V
		I <sub>OL</sub> = 3 mA	1.65		0.3	V
I <sub>I</sub>	Input Leakage Current	0 ≤ V <sub>I</sub> ≤ 3.6V	1.65 - 2.3		±5.0	μA
I <sub>OZ</sub>	3-STATE Output Leakage	0 ≤ V <sub>O</sub> ≤ 3.6V V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	1.65 - 2.3		±10	μA
I <sub>OFF</sub>	Power-OFF Leakage Current	0 ≤ (V <sub>I</sub> , V <sub>O</sub> ) ≤ 3.6V	0		10	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND	1.65 - 2.3		20	μA
		V <sub>CC</sub> ≤ (V <sub>I</sub> , V <sub>O</sub> ) ≤ 3.6V (Note 7)	1.65 - 2.3		±20	μA

Note 7: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 8)								
Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}, C_L = 30\text{ pF}, R_L = 500\Omega$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 1.8V \pm 0.15V$		
		Min	Max	Min	Max	Min	Max	
$t_{PHL}, t_{PLH}$	Prop Delay	0.8	3.3	1.0	3.8	1.5	7.6	ns
$t_{PZL}, t_{PZH}$	Output Enable Time	0.8	3.8	1.0	5.1	1.5	9.8	ns
$t_{PLZ}, t_{PHZ}$	Output Disable Time	0.8	3.6	1.0	4.0	1.5	7.2	ns
$t_{OSHL}, t_{OSLH}$	Output to Output Skew (Note 9)		0.5		0.5		0.75	ns
<p><b>Note 8:</b> For <math>C_L = 50\text{ pF}</math>, add approximately 300 ps to the AC maximum specification.</p> <p><b>Note 9:</b> Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (<math>t_{OSHL}</math>) or LOW-to-HIGH (<math>t_{OSLH}</math>).</p>								
Dynamic Switching Characteristics								
Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$	Units			
				Typical				
$V_{OLP}$	Quiet Output Dynamic Peak $V_{OL}$	$C_L = 30\text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0V$	1.8	0.15	V			
			2.5	0.25				
			3.3	0.35				
$V_{OLV}$	Quiet Output Dynamic Valley $V_{OL}$	$C_L = 30\text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0V$	1.8	-0.15	V			
			2.5	-0.25				
			3.3	-0.35				
$V_{OHV}$	Quiet Output Dynamic Valley $V_{OH}$	$C_L = 30\text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0V$	1.8	1.55	V			
			2.5	2.05				
			3.3	2.65				
Capacitance								
Symbol	Parameter	Conditions	$T_A = +25^\circ\text{C}$	Units				
			Typical					
$C_{IN}$	Input Capacitance	$V_{CC} = 1.8, 2.5V \text{ or } 3.3V, V_I = 0V \text{ or } V_{CC}$	6	pF				
$C_{OUT}$	Output Capacitance	$V_I = 0V \text{ or } V_{CC}, V_{CC} = 1.8V, 2.5V \text{ or } 3.3V$	7	pF				
$C_{PD}$	Power Dissipation Capacitance	$V_I = 0V \text{ or } V_{CC}, f = 10\text{ MHz}, V_{CC} = 1.8V, 2.5V \text{ or } 3.3V$	20	pF				

### AC Loading and Waveforms



TEST	SWITCH
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3V$ ; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V; 1.8V \pm 0.15V$
$t_{PZH}, t_{PHZ}$	GND

FIGURE 1. AC Test Circuit

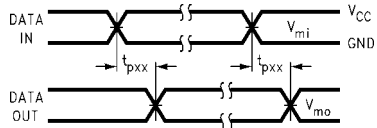


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

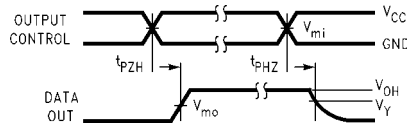


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

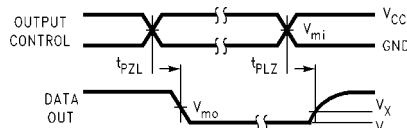
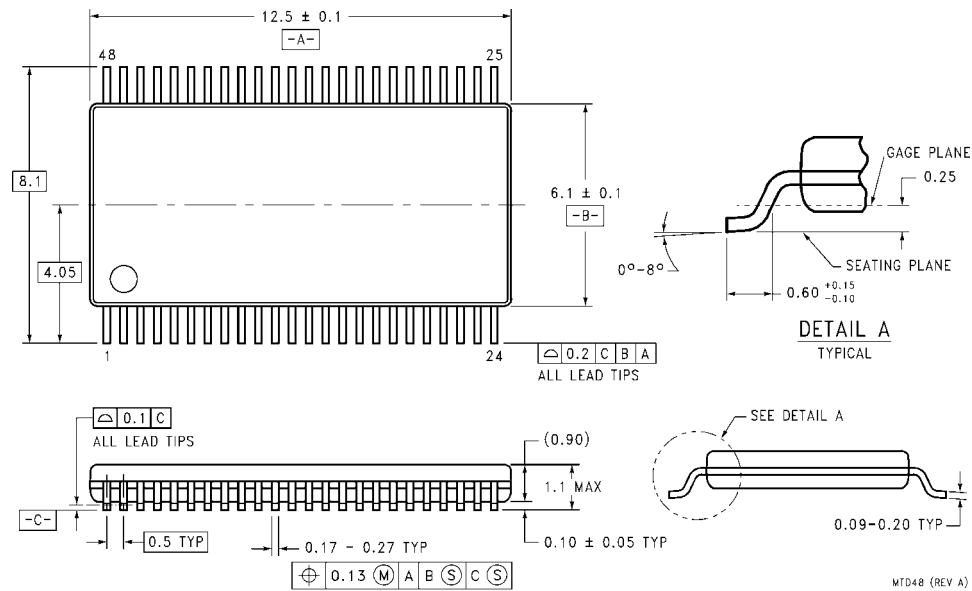


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	$V_{CC}$		
	$3.3V \pm 0.3V$	$2.5V \pm 0.2V$	$1.8V \pm 0.15V$
$V_{mi}$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_{mo}$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_X$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
$V_Y$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

**Physical Dimensions** inches (millimeters) unless otherwise noted



**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide  
Package Number MTD48**

MTD48 (REV A)

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