FAIRCHILD SEMICONDUCTOR™

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74VCX16601
Low Voltage 18-Bit Universal Bus Transceivers with 3.6V Tolerant Inputs and Outputs

General Description

The VCX16601 is an 18-bit universal bus transceiver which combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH-to-LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB. When $\overline{OEAB}$ is LOW, the outputs are active. When $\overline{OEAB}$ is HIGH, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA and $\overline{CLKENBA}$.

The VCX16601 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O capability up to 3.6V.

The VCX16601 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.65V–3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- t_{PD} (A to B, B to A)
  - 2.9 ns max for 3.0V to 3.6V V_{CC}
  - 3.5 ns max for 2.3V to 2.7V V_{CC}
  - 7.0 ns max for 1.65V 1.95V V_{CC}
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- Static Drive (I_{OH}/I_{OL})
  - ±24 mA @ 3.0V V_{CC}
  - ±18 mA @ 2.3V V_{CC}
  - ±6 mA @ 1.65V V_{CC}
- Uses patented noise/EMI reduction circuitry
- Latchup performance exceeds 300 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model >200V

Note 1: To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

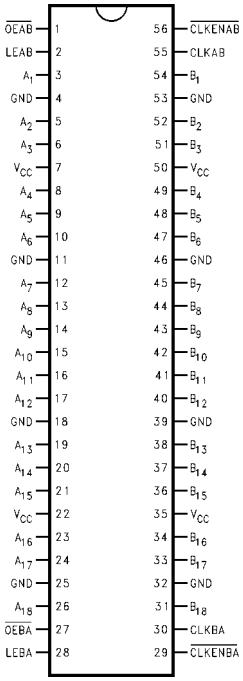
Order Number	Package Number	Package Description
74VCX16601MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Pin Descriptions

Pin Names	Description
$\overline{OEAB}$, $\overline{OEBA}$	Output Enable Inputs (Active LOW)
LEAB, LEBA	Latch Enable Inputs
CLKAB, CLKBA	Clock Inputs
$\overline{CLKENAB}$, $\overline{CLKENBA}$	Clock Enable Inputs
A_1–A_{18}	Side A Inputs or 3-STATE Outputs
B_1–B_{18}	Side B Inputs or 3-STATE Outputs

Connection Diagram



Function Table (Note 2)

Inputs					Outputs
$\overline{CLKENAB}$	$\overline{OEAB}$	LEAB	CLKAB	A_n	B_n
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0 (Note 3)
H	L	L	X	X	B_0 (Note 3)
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B_0 (Note 3)
L	L	L	H	X	B_0 (Note 4)

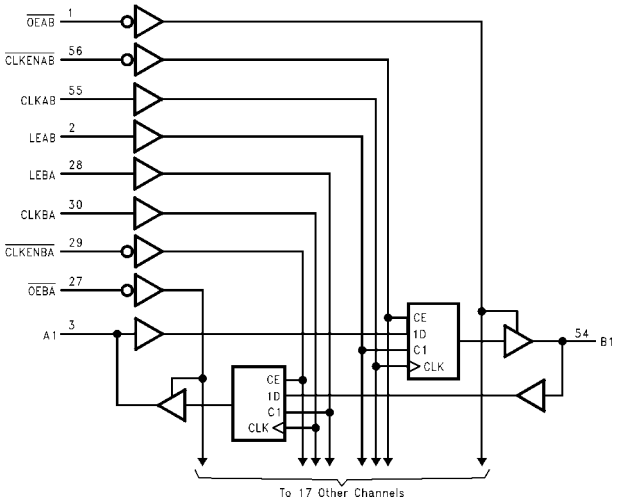
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs may not float)
Z = High Impedance

Note 2: A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CLKENBA}$.

Note 3: Output level before the indicated steady-state input conditions were established.

Note 4: Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.

Logic Diagram



Absolute Maximum Ratings (Note 5)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to +4.6V
Output Voltage (V_O)	
Outputs 3-Stated	−0.5V to +4.6V
Outputs Active (Note 6)	−0.5 to V_{CC} + 0.5V
DC Input Diode Current (I_{IK}) V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
V_O > V_{CC}	+50 mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	±50 mA
DC V_{CC} or Ground Current per Supply Pin (I_{CC} or Ground)	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 7)

Power Supply	
Operating	1.65V to 3.6V
Data Retention Only	1.2V to 3.6V
Input Voltage	−0.3V to 3.6V
Output Voltage (V_O)	
Output in Active States	0V to V_{CC}
Output in 3-STATE	0.0V to 3.6V
Output Current in I_{OH}/I_{OL}	
V_{CC} = 3.0V to 3.6V	±24 mA
V_{CC} = 2.3V to 2.7V	±18 mA
V_{CC} = 1.65V to 2.3V	±6 mA
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

Note 5: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The Recommended Operating Conditions tables will define the conditions for actual device operation.

Note 6: I_O Absolute Maximum Rating must be observed.

Note 7: Floating or unused pin (inputs or I/O's) must be held HIGH or LOW.

DC Electrical Characteristics (2.7V < V_{CC} ≤ 3.6V)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7 – 3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7 – 3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA	2.7 – 3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		
		I_{OH} = −18 mA	3.0	2.4		
		I_{OH} = −24 mA	3.0	2.2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	2.7 – 3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	
		I_{OL} = 18 mA	3.0		0.4	
		I_{OL} = 24 mA	3.0		0.55	
I_I	Input Leakage Current	0V ≤ V_I ≤ 3.6V	2.7 – 3.6		±5.0	µA
I_{OZ}	3-STATE Output Leakage	0V ≤ V_O ≤ 3.6V; V_I = V_{IH} or V_{IL}	2.7 – 3.6		±10	µA
I_{OFF}	Power Off Leakage Current	0V ≤ (V_I, V_O) ≤ 3.6V	0		10	µA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7 – 3.6		20	µA
		V_{CC} ≤ (V_I, V_O) ≤ 3.6V (Note 8)	2.7 – 3.6		±20	
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6V	2.7 – 3.6		750	µA

Note 8: Outputs disabled or 3-STATE only.

DC Electrical Characteristics ($2.3V \le V_{CC} \le 2.7V$)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.6		V
V_{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = –100 µA	2.3 – 2.7	V_{CC} – 0.2		V
		I_{OH} = –6 mA	2.3	2.0		
		I_{OH} = –12 mA	2.3	1.8		
		I_{OH} = –18 mA	2.3	1.7		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	2.3 – 2.7		0.2	V
		I_{OL} = 12 mA	2.3		0.4	
		I_{OL} = 18 mA	2.3		0.6	
I_I	Input Leakage Current	$0 \le V_I \le 3.6V$	2.3 – 2.7		±5.0	µA
I_{OZ}	3-STATE Output Leakage	$0 \le V_O \le 3.6V$	2.3 – 2.7		±10	µA
		$V_I = V_{IH}$ or V_{IL}				
I_{OFF}	Power Off Leakage Current	$0 \le (V_I, V_O) \le 3.6V$	0		10	µA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 – 2.7		20	µA
		$V_{CC} \le (V_I, V_O) \le 3.6V$ (Note 9)	2.3 – 2.7		±20	

Note 9: Outputs disabled or 3-STATE only.

DC Electrical Characteristics ($1.65V \le V_{CC} < 2.3V$)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		1.65 - 2.3	$0.65 \times V_{CC}$		V
V_{IL}	LOW Level Input Voltage		1.65 - 2.3		$0.35 \times V_{CC}$	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = –100 µA	1.65 - 2.3	V_{CC} – 0.2		V
		I_{OH} = –6 mA	1.65	1.25		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	1.65 - 2.3		0.2	V
		I_{OL} = 6 mA	1.65		0.3	
I_I	Input Leakage Current	$0 \le V_I \le 3.6V$	1.65 - 2.3		±5.0	µA
I_{OZ}	3-STATE Output Leakage	$0 \le V_O \le 3.6V$	1.65 - 2.3		±10	µA
		$V_I = V_{IH}$ or V_{IL}				
I_{OFF}	Power Off Leakage Current	$0 \le (V_I, V_O) \le 3.6V$	0		10	µA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	1.65 - 2.3		20	µA
		$V_{CC} \le (V_I, V_O) \le 3.6V$ (Note 10)	1.65 - 2.3		±20	

Note 10: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 11)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 30$ pF, $R_L = 500\Omega$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.5 \pm 0.2V$		$V_{CC} = 1.8V \pm 0.15V$		
		Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	250		200		100		MHz
t_{PHL} t_{PLH}	Propagation Delay Bus to Bus	0.8	2.9	1.0	3.5	1.5	7.0	ns
t_{PHL} t_{PLH}	Propagation Delay Clock to Bus	0.8	3.5	1.0	4.4	1.5	8.8	ns
t_{PHL} t_{PLH}	Propagation Delay LE to Bus	0.8	3.5	1.0	4.4	1.5	8.8	ns
t_{PZL} t_{PZH}	Output Enable Time	0.8	3.8	1.0	4.9	1.5	9.8	ns
t_{PLZ} t_{PHZ}	Output Disable Time	0.8	3.7	1.0	4.2	1.5	7.6	ns
t_S	Setup Time	1.5		1.5		2.5		ns
t_H	Hold Time	1.0		1.0		1.0		ns
t_W	Pulse Width	1.5		1.5		4.0		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 12)		0.5		0.5		0.75	ns

Note 11: For $C_L = 50$pF, add approximately 300ps to the AC maximum specification.

Note 12: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = +25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8 2.5 3.3	0.25 0.6 0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8 2.5 3.3	–0.25 –0.6 –0.8	V
V_{OHV}	Quiet Output Dynamic Valley V_{OH}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8 2.5 3.3	1.5 1.9 2.2	V

Capacitance

Symbol	Parameter	Conditions	$T_A = +25°C$	Units
C_{IN}	Input Capacitance	$V_I = 0V$ or V_{CC} $V_{CC} = 1.8V$, 2.5V, or 3.3V	6	pF
$C_{I/O}$	Output Capacitance	$V_I = 0V$ or V_{CC}, $V_{CC} = 1.8V$, 2.5V or 3.3V	7	pF
C_{PD}	Power Dissipation Capacitance	$V_I = 0V$ or V_{CC}, f = 10 MHz $V_{CC} = 1.8V$, 2.5V or 3.3V	20	pF

AC Loading and Waveforms

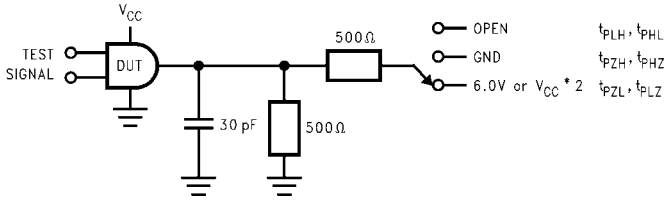


FIGURE 1. AC Test Circuit

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ± 0.3V; V_{CC} x 2 at V_{CC} = 2.5 ± 0.2V; 1.8V ± 0.15V
t_{PZH}, t_{PHZ}	GND

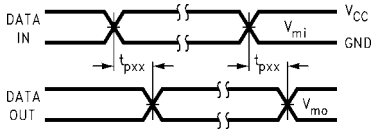


FIGURE 2. Waveform for Inverting and Non-inverting Functions

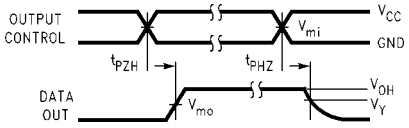


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

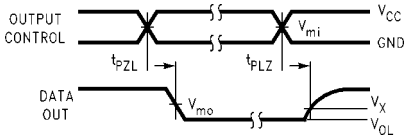


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

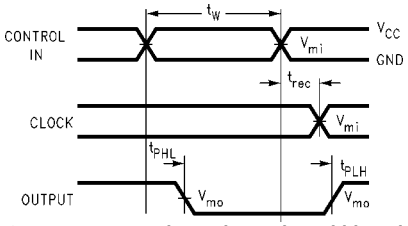


FIGURE 5. Propagation Delay, Pulse Width and t_{rec} Waveforms

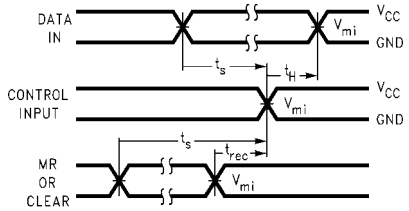
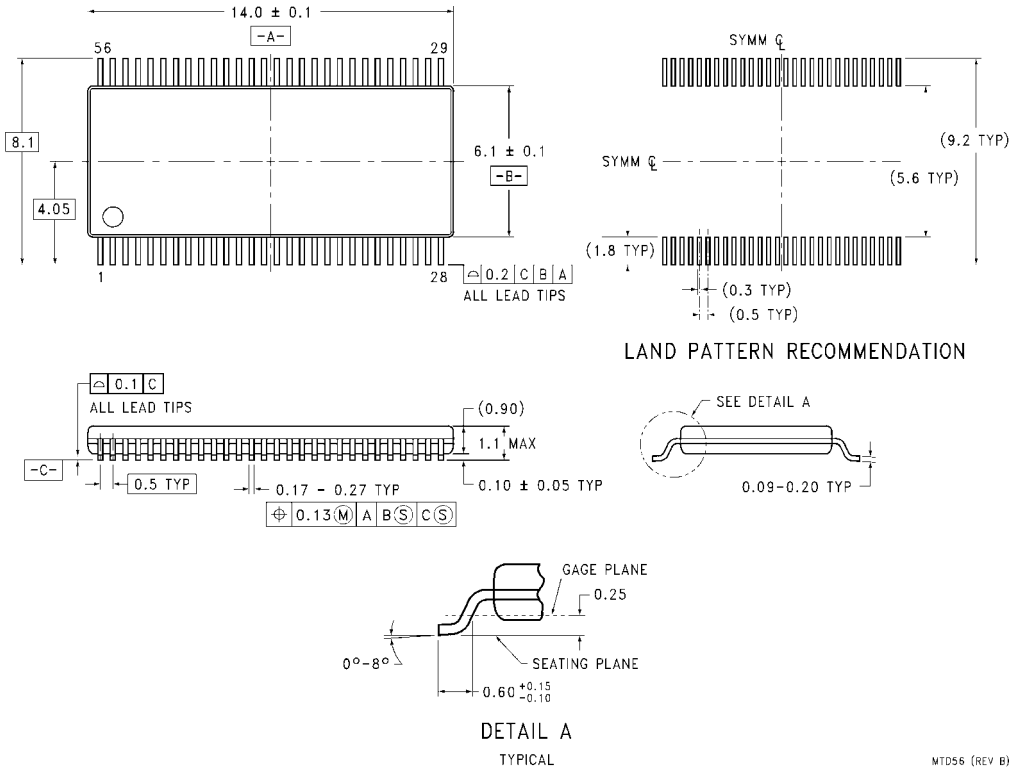


FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

Symbol	V_{CC}		
	3.3V ± 0.3V	2.5V ± 0.2V	1.8V ± 0.15V
V_{mi}	1.5V	V_{CC}/2	V_{CC}/2
V_{mo}	1.5V	V_{CC}/2	V_{CC}/2
V_X	V_{OL} + 0.3V	V_{OL} + 0.15V	V_{OL} + 0.15V
V_Y	V_{OH} − 0.3V	V_{OH} − 0.15V	V_{OH} − 0.15V

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

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