

74VCX2245

Low Voltage Bidirectional Transceiver with 3.6V Tolerant Inputs and Outputs and 26Ω Series Resistors in B Outputs

General Description

The VCX2245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The T/R input determines the direction of data flow. The \overline{OE} input disables both the A and B ports by placing them in a high impedance state.

The 74VCX2245 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V. The VCX2245 is also designed with 26Ω series resistance in the B Port outputs. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers transmitters.

The 74VCX2245 is fabricated with an advanced CMOS technology to achieve high-speed operation while maintaining low CMOS power dissipation.

Features

- 1.65V - 3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- 26Ω series resistors in B Port outputs
- Power-off high impedance inputs and outputs
- Supports Live Insertion and Withdrawal (Note 1)
- t_{PD} (A to B)
 - 4.4 ns max for 3.0V to 3.6V V_{CC}
 - 5.6 ns max for 2.3V to 2.7V V_{CC}
 - 9.8 ns max for 1.65V to 1.95V V_{CC}
- Static Drive (I_{OH}/I_{OL} B outputs):
 - ±12 mA @ 3.0V V_{CC}
 - ±8 mA @ 2.3V V_{CC}
 - ±3 mA @ 1.65V V_{CC}
- Uses patented Quiet Series™ noise/EMI reduction circuitry
- Latchup performance exceeds 300 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V

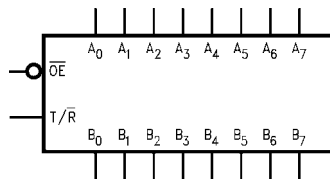
Note 1: To ensure the high impedance state during power up and power down, \overline{OE}_n should be tied to V_{CC} through a pull up resistor. The minimum value of the resistor is determined by the current sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74VCX2245WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74VCX2245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol

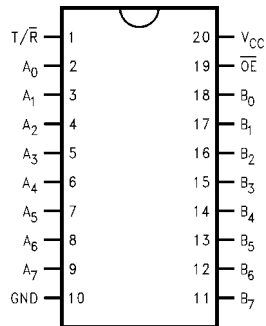


Pin Descriptions

Pin Names	Description
\overline{OE}	Output Enable Input (Active LOW)
T/R	Transmit/Receive Input
A ₀ -A ₇	Side A Inputs or 3-STATE Outputs
B ₀ -B ₇	Side B Inputs or 3-STATE Outputs

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Connection Diagram



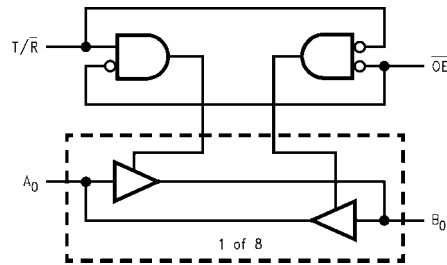
Truth Table

Inputs		Outputs
\overline{OE}	$\overline{T/R}$	
L	L	Bus B ₀ -B ₇ Data to Bus A ₀ -A ₇
L	H	Bus A ₀ -A ₇ Data to Bus B ₀ -B ₇
H	X	HIGH Z State on A ₀ -A ₇ , B ₀ -B ₇ (Note 2)

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

Note 2: Unused bus terminals during HIGH Z State must be held HIGH or LOW.

Logic Diagram



Absolute Maximum Ratings (Note 3)		Input Voltage	-0.3V to 3.6V			
Supply Voltage (V_{CC})	-0.5V to +4.6V	Output Voltage (V_O)	0V to V_{CC}			
DC Input Voltage (V_I)	-0.5V to +4.6V	Output in Active States	0V to 3.6V			
DC Output Voltage (V_O)		Output in 3-STATE	0V to 3.6V			
Outputs 3-STATE	-0.5V to +4.6V	Output Current in I_{OH}/I_{OL} - A Outputs				
Outputs Active (Note 4)	-0.5V to $V_{CC} + 0.5V$	$V_{CC} = 3.0V$ to 3.6V	±24 mA			
DC Input Diode Current (I_{IK}) $V_I < 0V$	-50 mA	$V_{CC} = 2.3V$ to 2.7V	±18 mA			
DC Output Diode Current (I_{OK})		$V_{CC} = 1.65V$ to 2.3V	±6 mA			
$V_O < 0V$	-50 mA	Output Current in I_{OH}/I_{OL} - B Outputs				
$V_O > V_{CC}$	+50 mA	$V_{CC} = 3.0V$ to 3.6V	±12 mA			
DC Output Source/Sink Current	±50 mA	$V_{CC} = 2.3V$ to 2.7V	±8 mA			
(I_{OH}/I_{OL})		$V_{CC} = 1.65V$ to 2.3V	±3 mA			
DC V_{CC} or Ground Current	±100 mA	Free Air Operating Temperature (T_A)	-40°C to +85°C			
Storage Temperature (T_{STG})	-65°C to +150°C	Minimum Input Edge Rate ($\Delta t/\Delta V$)				
		$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V			
Recommended Operating Conditions (Note 5)		Note 3: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.				
Power Supply Voltage (V_{CC})		Note 4: I_O Absolute Maximum Rating must be observed.				
Operating	1.65V to 3.6V	Note 5: Floating or unused inputs must be held HIGH or LOW.				
Data Retention Only	1.2V to 3.6V					
DC Electrical Characteristics (2.7V < V_{CC} ≤ 3.6V)						
Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7-3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7-3.6		0.8	V
V_{OH}	HIGH Level Output Voltage A Outputs	$I_{OH} = -100 \mu A$	2.7-3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -12 mA$	2.7	2.2		
		$I_{OH} = -18 mA$	3.0	2.4		
		$I_{OH} = -24 mA$	3.0	2.2		
V_{OH}	HIGH Level Output Voltage B Outputs	$I_{OH} = -100 \mu A$	2.7-3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -6 mA$	2.7	2.2		
		$I_{OH} = -8 mA$	3.0	2.4		
		$I_{OH} = -12 mA$	3.0	2.2		
V_{OL}	LOW Level Output Voltage A Outputs	$I_{OL} = 100 \mu A$	2.7-3.6		0.2	V
		$I_{OL} = 12 mA$	2.7	0.4		
		$I_{OL} = 18 mA$	3.0	0.4		
		$I_{OL} = 24 mA$	3.0	0.55		
V_{OL}	LOW Level Output Voltage B Outputs	$I_{OL} = 100 \mu A$	2.7-3.6		0.2	V
		$I_{OL} = 6 mA$	2.7	0.4		
		$I_{OL} = 8 mA$	3.0	0.55		
		$I_{OL} = 12 mA$	3.0	0.8		
I_I	Input Leakage Current	$0 \leq V_I \leq 3.6V$	2.7-3.6		±5.0	μA
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ $V_I = V_{IH}$ or V_{IL}	2.7-3.6		±10	μA
I_{OFF}	Power Off Leakage Current	$0 \leq (V_I, V_O) \leq 5.5V$	0		10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.7-3.6		20	μA
		$V_{CC} \leq (V_I, V_O) \leq 3.6V$ (Note 6)	2.7-3.6		±20	
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.7-3.6		750	μA
Note 6: Outputs disabled or 3-STATE only.						

DC Electrical Characteristics (2.3V ≤ V_{CC} ≤ 2.7V)

Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units
V _{IH}	HIGH Level Input Voltage		2.3–2.7	1.6		V
V _{IL}	LOW Level Input Voltage		2.3–2.7		0.7	V
V _{OH}	HIGH Level Output Voltage A Outputs	I _{OH} = -100 μA	2.3–2.7	V _{CC} - 0.2		V
		I _{OH} = -6 mA	2.3	2.0		
		I _{OH} = -12 mA	2.3	1.8		
		I _{OH} = -18 mA	2.3	1.7		
V _{OH}	HIGH Level Output Voltage B Outputs	I _{OH} = -100 μA	2.3–2.7	V _{CC} -2		V
		I _{OH} = -4 mA	2.3	2.0		
		I _{OH} = -6 mA	2.3	1.8		
		I _{OH} = -8mA	2.3	1.7		
V _{OL}	LOW Level Output Voltage A Outputs	I _{OL} = 100 μA	2.3–2.7		0.2	V
		I _{OL} = 12 mA	2.3	0.4		
		I _{OL} = 18 mA	2.3	0.6		
V _{OL}	LOW Level Output Voltage B Outputs	I _{OL} = 100 μA	2.3–2.7		0.2	V
		I _{OL} = 6 mA	2.3	0.4		
		I _{OL} = 8 mA	2.3	0.6		
I _I	Input Leakage Current	0 ≤ V _I ≤ 3.6V	2.3–2.7		±5.0	μA
I _{OZ}	3-STATE Output Leakage	0 ≤ V _O ≤ 3.6V V _I = V _{IH} or V _{IL}	2.3–2.7		±10	μA
I _{OFF}	Power Off Leakage Current	0 ≤ (V _I , V _O) ≤ 3.6V	0		10	μA
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND V _{CC} ≤ (V _I , V _O) ≤ 3.6V (Note 7)	2.3–2.7 2.3–2.7		20 ±20	μA

Note 7: Outputs disabled or 3-STATE only.

DC Electrical Characteristics (1.65V ≤ V_{CC} < 2.3V)

Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units
V _{IH}	HIGH Level Input Voltage		1.65–2.3	0.65 x V _{CC}		V
V _{IL}	LOW Level Input Voltage		1.65–2.3		0.35 x V _{CC}	V
V _{OH}	HIGH Level Output Voltage A Outputs	I _{OH} = -100 μA	1.65–2.3	V _{CC} - 0.2		V
		I _{OH} = -6 mA	1.65	1.25		
V _{OH}	HIGH Level Output Voltage B Outputs	I _{OH} = -100 μA	1.65–2.3	V _{CC} -0.2		V
		I _{OH} = -3 mA	1.65	1.25		
V _{OL}	LOW Level Output Voltage A Outputs	I _{OL} = 100 μA	1.65–2.3		0.2	V
		I _{OL} = 6 mA	1.65	0.3		
V _{OL}	LOW Level Output Voltage B Outputs	I _{OL} = 100μA	1.65–2.3		0.2	V
		I _{OL} = 3 mA	1.65	0.3		
I _I	Input Leakage Current	0 ≤ V _I ≤ 3.6V	1.65–2.3		±5.0	μA
I _{OZ}	3-STATE Output Leakage	0 ≤ V _O ≤ 3.6V V _I = V _{IH} or V _{IL}	1.65-2.3		±10	μA
I _{OFF}	Power Off Leakage Current	0 ≤ (V _I , V _O) ≤ 3.6V	0		10	μA
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND V _{CC} ≤ (V _I , V _O) ≤ 3.6V (Note 8)	1.65–2.3 1.65–2.3		20 ±20	μA

Note 8: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 9)								
Symbol	Parameter	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, C_L = 30 \text{ pF}, R_L = 500\Omega$						Units
		$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$		$V_{CC} = 2.5\text{V} \pm 0.2\text{V}$		$V_{CC} = 1.8\text{V} \pm 0.15\text{V}$		
		Min	Max	Min	Max	Min	Max	
t_{PHL}	Propagation Delay, A to B	0.6	4.4	0.8	5.6	1.5	9.8	ns
t_{PLH}								
t_{PHL}	Propagation Delay, B to A	0.6	3.5	0.8	4.2	1.5	8.4	ns
t_{PLH}								
t_{PZL}	Output Enable Time, A to B	0.6	5.0	0.8	6.6	1.5	9.8	ns
t_{PZH}								
t_{PZL}	Output Enable Time, B to A	0.6	4.5	0.8	5.6	1.5	9.8	ns
t_{PZH}								
t_{PLZ}	Output Disable Time, A to B	0.6	4.2	0.8	4.7	1.5	8.5	ns
t_{PHZ}								
t_{PLZ}	Output Disable Time, B to A	0.6	3.6	0.8	4.0	1.5	7.2	ns
t_{PHZ}								
t_{OSHL}	Output to Output Skew (Note 10)		0.5		0.5		0.75	ns
t_{OSLH}								
<p>Note 9: For $C_L = 50 \text{ pF}$, add approximately 300 ps to the AC maximum specification.</p> <p>Note 10: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).</p>								
Dynamic Switching Characteristics								
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25^{\circ}\text{C}$	Units			
				Typical				
V_{OLP}	Quiet Output Dynamic Peak V_{OL} , B to A	$C_L = 30 \text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	1.8	0.3	V			
			2.5	0.7				
			3.3	1.0				
V_{OLV}	Quiet Output Dynamic Peak V_{OL} , A to B	$C_L = 30 \text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	1.8	0.2	V			
			2.5	0.45				
			3.3	0.65				
V_{OLV}	Quiet Output Dynamic Valley V_{OL} , B to A	$C_L = 30 \text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	1.8	-0.3	V			
			2.5	-0.7				
			3.3	-1.0				
V_{OLV}	Quiet Output Dynamic Valley V_{OL} , A to B	$C_L = 30 \text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	1.8	-0.2	V			
			2.5	-0.45				
			3.3	-0.65				
V_{OHV}	Quiet Output Dynamic Valley V_{OH} , B to A	$C_L = 30 \text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	1.8	1.3	V			
			2.5	1.7				
			3.3	2.0				
V_{OHV}	Quiet Output Dynamic Valley V_{OH} , A to B	$C_L = 30 \text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	1.8	1.5	V			
			2.5	2.0				
			3.3	2.5				
Capacitance								
Symbol	Parameter	Conditions	$T_A = +25^{\circ}\text{C}$	Units				
			Typical					
C_{IN}	Input Capacitance	$V_I = 0\text{V}$ or V_{CC} , $V_{CC} = 1.8\text{V}, 2.5\text{V}$ or 3.3V	6	pF				
C_{IO}	Input/Output Capacitance	$V_I = 0\text{V}$ or V_{CC} , $V_{CC} = 1.8\text{V}, 2.5\text{V}$ or 3.3V	7	pF				
C_{PD}	Power Dissipation Capacitance	$V_I = 0\text{V}$ or V_{CC} , $f = 10 \text{ MHz}$, $V_{CC} = 1.8\text{V}, 2.5\text{V}$ or 3.3V	20	pF				

AC Loading and Waveforms

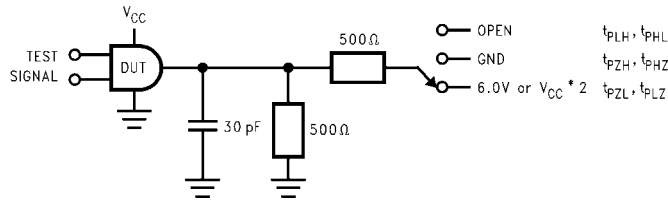


FIGURE 1. AC Test Circuit

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$; $V_{CC} \times 2$ at $V_{CC} = 2.5V \pm 0.2V; 1.8V \pm 0.15V$
t_{PZH}, t_{PHZ}	GND

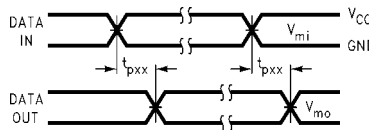


FIGURE 2. Waveform for Inverting and Non-inverting Functions

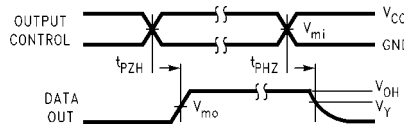


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

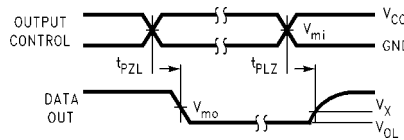
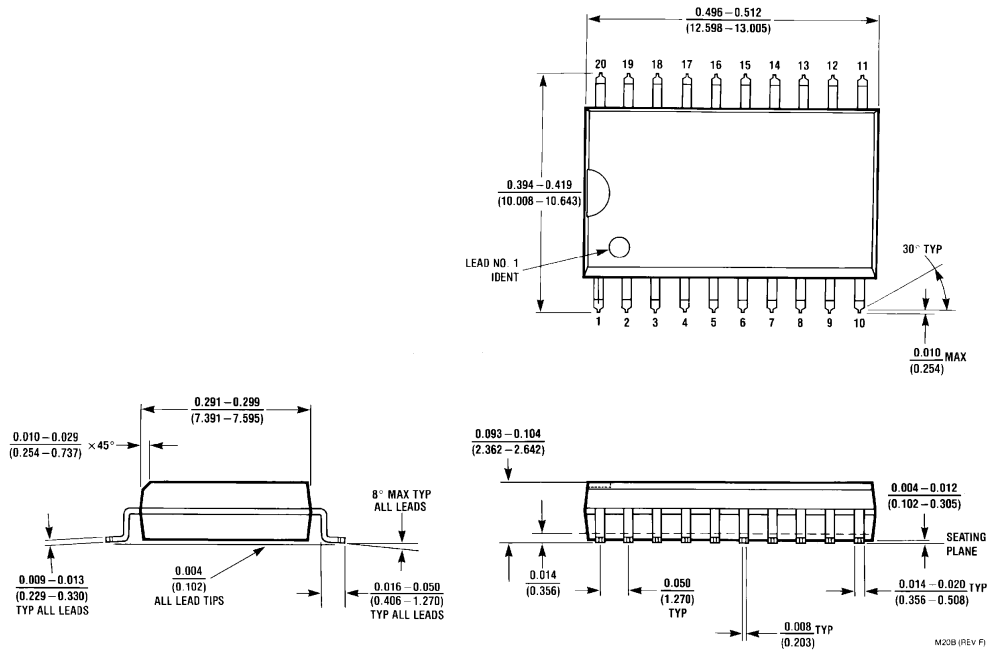


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

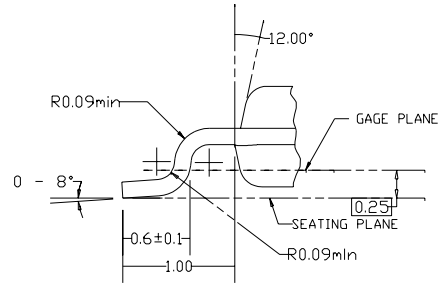
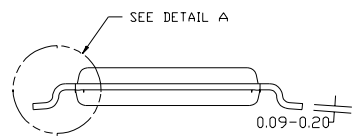
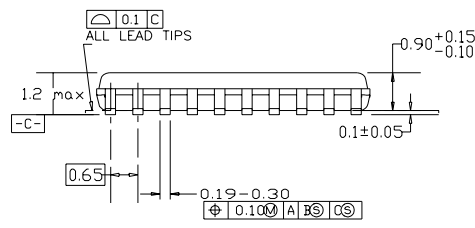
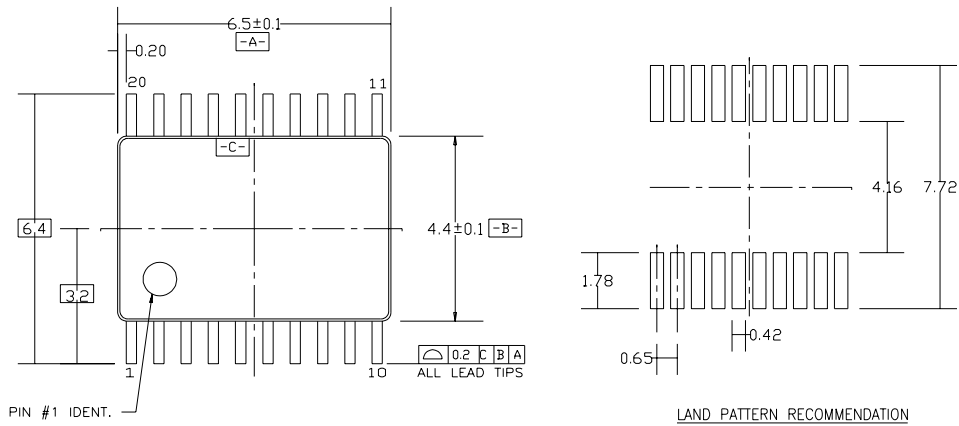
Symbol	V_{CC}		
	$3.3V \pm 0.3V$	$2.5V \pm 0.2V$	$1.8V \pm 0.15V$
V_{mi}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
V_y	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20**

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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