



November 1999
Revised November 1999

74VCXH162244 Low Voltage 16-Bit Buffer/Line Driver with Bushold

74VCXH162244 Low Voltage 16-Bit Buffer/Line Driver with Bushold and 26Ω Series Resistor in Outputs (Preliminary)

General Description

The VCXH162244 contains sixteen non-inverting buffers with 3-STATE outputs to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble (4-bit) controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation. .

The VCXH162244 data inputs include active bushold circuitry, eliminating the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level

The 74VCXH162244 is also designed with 26Ω series resistors in the outputs. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The 74VCXH162244 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with output capability up to 3.6V.

The 74VCXH162244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

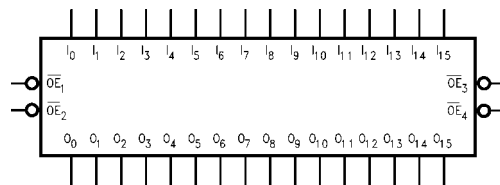
- 1.65V–3.6V V_{CC} supply operation
- 3.6V tolerant control inputs and outputs
- Bushold on data inputs eliminates the need for external pull-up/pull-down resistors
- 26Ω series resistors in outputs
- t_{PD}
 - 3.3 ns max for 3.0V to 3.6V V_{CC}
 - 3.8 ns max for 2.3V to 2.7V V_{CC}
 - 7.6 ns max for 1.65V to 1.95V V_{CC}
- Static Drive (I_{OH}/I_{OL})
 - ±12 mA @ 3.0V V_{CC}
 - ±8 mA @ 2.3V V_{CC}
 - ±3 mA @ 1.65V V_{CC}
- Uses patented noise/EMI reduction circuitry
- Latch-up performance exceeds 300 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V

Ordering Code:

Order Number	Package Number	Package Description
74VCXH162244MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TUBES]
74VCXH162244MTX (Note 1)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TAPE and REEL]

Note 1: Use this Order Number to receive devices in Tape and Reel.

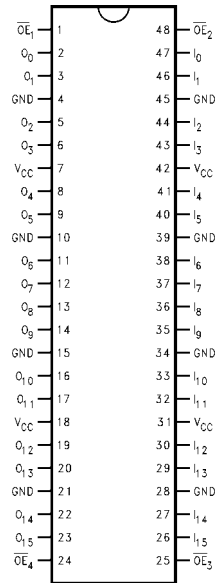
Logic Symbol



Pin Descriptions

Pin Names	Description
\overline{OE}_n	Output Enable Input (Active LOW)
I ₀ –I ₁₅	Bushold Inputs
O ₀ –O ₁₅	Outputs

Connection Diagram



Truth Tables

Inputs		Outputs
\overline{OE}_1	I_0-I_3	O_0-O_3
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
\overline{OE}_2	I_4-I_7	O_4-O_7
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
\overline{OE}_3	I_8-I_{11}	O_8-O_{11}
L	L	L
L	H	H
H	X	Z

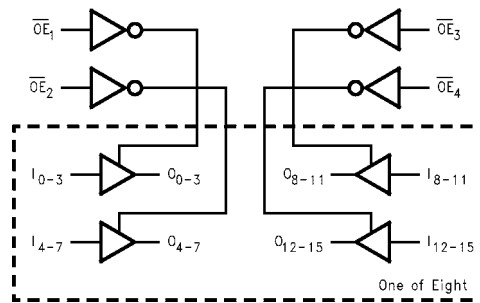
Inputs		Outputs
\overline{OE}_4	$I_{12}-I_{15}$	$O_{12}-O_{15}$
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial (HIGH or LOW, inputs may not float)
 Z = High Impedance

Functional Description

The 74VCXH162244 contains sixteen non-inverting buffers with 3-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of each other. The control pins may be shorted together to obtain full 16-bit operation. The 3-STATE outputs are controlled by an Output Enable (\overline{OE}_n) input. When \overline{OE}_n is LOW, the outputs are in the 2-state mode. When \overline{OE}_n is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the inputs.

Logic Diagram



Absolute Maximum Ratings (Note 2)		Recommended Operating Conditions (Note 4)	
Supply Voltage (V_{CC})	-0.5V to +4.6V	Power Supply	
DC Input Voltage (V_I)		Operating	1.65V to 3.6V
\overline{OE}_n	-0.5V to 4.6V	Data Retention Only	1.2V to 3.6V
$I_0 - I_{15}$	-0.5V to $V_{CC} + 0.5V$	Input Voltage	-0.3V to V_{CC}
Output Voltage (V_O)		Output Voltage (V_O)	
Outputs 3-STATE	-0.5V to +4.6V	Output in Active States	0V to V_{CC}
Outputs Active (Note 3)	-0.5V to $V_{CC} + 0.5V$	Output in 3-STATE	0.0V to 3.6V
DC Input Diode Current (I_{IK})		Output Current in I_{OH}/I_{OL}	
$V_I < 0V$	-50 mA	$V_{CC} = 3.0V$ to 3.6V	± 12 mA
DC Output Diode Current (I_{OK})		$V_{CC} = 2.3V$ to 2.7V	± 8 mA
$V_O < 0V$	-50 mA	$V_{CC} = 1.65V$ to 2.3V	± 3 mA
$V_O > V_{CC}$	+50 mA	Free Air Operating Temperature (T_A)	-40°C to +85°C
DC Output Source/Sink Current (I_{OH}/I_{OL})	± 50 mA	Minimum Input Edge Rate ($\Delta t/\Delta V$)	
DC V_{CC} or GND Current per Supply Pin (I_{CC} or GND)	± 100 mA	$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V
Storage Temperature Range (T_{STG})	-65°C to +150°C	<p>Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.</p> <p>Note 3: I_0 Absolute Maximum Rating must be observed.</p> <p>Note 4: Floating or unused control inputs must be held HIGH or LOW.</p>	

DC Electrical Characteristics (2.7V < V_{CC} ≤ 3.6V)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units	
V_{IH}	HIGH Level Input Voltage		2.7-3.6	2.0		V	
V_{IL}	LOW Level Input Voltage		2.7-3.6		0.8	V	
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.7-3.6	$V_{CC} - 0.2$		V	
		$I_{OH} = -6$ mA	2.7	2.2		V	
		$I_{OH} = -8$ mA	3.0	2.4		V	
		$I_{OH} = -12$ mA	3.0	2.2		V	
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.7-3.6		0.2	V	
		$I_{OL} = 6$ mA	2.7		0.4	V	
		$I_{OL} = 8$ mA	3.0		0.55	V	
		$I_{OL} = 12$ mA	3.0		0.8	V	
I_I	Input Leakage Current	Control Pins	$0 \leq V_I \leq 3.6V$	2.7-3.6		± 5.0	μA
		Data Pins	$0 \leq V_I \leq V_{CC}$	2.7-3.6		± 5.0	μA
$I_{IH(HOLD)}$	Bushold Input Minimum Drive Hold Current		$V_{IN} = 0.8V$	3.0	75		μA
			$V_{IN} = 2.0V$	3.0	-75		μA
$I_{I(OD)}$	Bushold Input Over-Drive Current to Change State		(Note 5)	3.6	450		μA
			(Note 6)	3.6	-450		μA
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ $V_I = V_{IH}$ or V_{IL}	2.7-3.6		± 10	μA	
I_{OFF}	Power-OFF Leakage Current	$0 \leq (V_O) \leq 3.6V$	0		10	μA	
I_{CC}	Quiescent Supply Current		$V_I = V_{CC}$ or GND	2.7-3.6	20		μA
			$V_{CC} \leq (V_O) \leq 3.6V$ (Note 7)	2.7-3.6		± 20	μA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.7-3.6		750	μA	

Note 5: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 6: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 7: Outputs disabled or 3-STATE only.

DC Electrical Characteristics (2.3V ≤ V_{CC} ≤ 2.7V)

Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units
V _{IH}	HIGH Level Input Voltage		2.3-2.7	1.6		V
V _{IL}	LOW Level Input Voltage		2.3-2.7		0.7	V
V _{OH}	HIGH Level Output Voltage	I _{OH} = -100 μA	2.3-2.7	V _{CC} - 0.2		V
		I _{OH} = -4 mA	2.3	2.0		V
		I _{OH} = -6 mA	2.3	1.8		V
		I _{OH} = -8 mA	2.3	1.7		V
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	2.3-2.7		0.2	V
		I _{OL} = 6 mA	2.3		0.4	V
		I _{OL} = 8 mA	2.3		0.6	V
I _I	Input Leakage Current	Control Pins 0 ≤ V _I ≤ 3.6V	2.3-2.7		±5.0	μA
		Data Pins 0 ≤ V _I ≤ V _{CC}	2.3-2.7		±5.0	μA
I _{I(HOLD)}	Bushold Input Minimum	V _{IN} = 0.7V	2.3	45		μA
	Drive Hold Current	V _{IN} = 1.6V	2.3	-45		
I _{I(OD)}	Bushold Input Over-Drive Current to Change State	(Note 8)	2.7	300		μA
		(Note 9)	2.7	-300		
I _{OZ}	3-STATE Output Leakage	0 ≤ V _O ≤ 3.6V V _I = V _{IH} or V _{IL}	2.3-2.7		±10	μA
I _{OFF}	Power-OFF Leakage Current	0 ≤ (V _O) ≤ 3.6V	0		10	μA
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	2.3-2.7		20	μA
		V _{CC} ≤ (V _O) ≤ 3.6V (Note 10)	2.3-2.7		±20	μA

Note 8: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 9: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 10: Outputs disabled or 3-STATE only.

DC Electrical Characteristics (1.65V ≤ V_{CC} < 2.3V)

Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units
V _{IH}	HIGH Level Input Voltage		1.65-2.3	0.65 × V _{CC}		V
V _{IL}	LOW Level Input Voltage		1.65-2.3		0.35 × V _{CC}	V
V _{OH}	HIGH Level Output Voltage	I _{OH} = -100 μA	1.65-2.3	V _{CC} - 0.2		V
		I _{OH} = -3 mA	1.65	1.25		V
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	1.65-2.3		0.2	V
		I _{OL} = 3mA	1.65		0.3	V
I _I	Input Leakage Current	Control Pins 0 ≤ V _I ≤ 3.6V	1.65-2.3		±5.0	μA
		Data Pins 0 ≤ V _I ≤ V _{CC}	1.65-2.3		±5.0	μA
I _{I(HOLD)}	Bushold Input Minimum	V _{IN} = 0.57V	1.65	25		μA
	Drive Hold Current	V _{IN} = 1.07V	1.65	-25		
I _{I(OD)}	Bushold Input Over-Drive Current to Change State	(Note 11)	1.95	200		μA
		(Note 12)	1.95	-200		
I _{OZ}	3-STATE Output Leakage	0 ≤ V _O ≤ 3.6V V _I = V _{IH} or V _{IL}	1.65-2.3		±10	μA
I _{OFF}	Power-OFF Leakage Current	0 ≤ (V _O) ≤ 3.6V	0		10	μA
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	1.65-2.3		20	μA
		V _{CC} ≤ (V _O) ≤ 3.6V (Note 13)	1.65-2.3		±20	μA

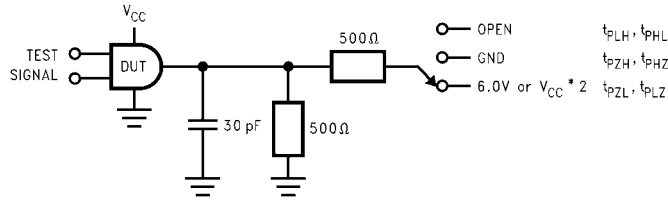
Note 11: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 12: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 13: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 14)								
Symbol	Parameter	T _A = -40°C to +85°C, C _L = 30 pF, R _L = 500Ω						Units
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.5V ± 0.2V		V _{CC} = 1.8V ± 0.15V		
		Min	Max	Min	Max	Min	Max	
t _{PHL} , t _{PLH}	Prop Delay	0.8	3.3	1.0	3.8	1.5	7.6	ns
t _{PZL} , t _{PZH}	Output Enable Time	0.8	3.8	1.0	5.1	1.5	9.8	ns
t _{PLZ} , t _{PHZ}	Output Disable Time	0.8	3.6	1.0	4.0	1.5	7.2	ns
t _{OSSL} t _{OSLH}	Output to Output Skew (Note 15)		0.5		0.5		0.75	ns
<p>Note 14: For C_L = 50pF, add approximately 300 ps to the AC maximum specification.</p> <p>Note 15: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSLH}).</p>								
Dynamic Switching Characteristics								
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = +25°C	Units			
				Typical				
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	0.15	V			
			2.5	0.25				
			3.3	0.35				
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	-0.15	V			
			2.5	-0.25				
			3.3	-0.35				
V _{OHV}	Quiet Output Dynamic Valley V _{OH}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	1.55	V			
			2.5	2.05				
			3.3	2.65				
Capacitance								
Symbol	Parameter	Conditions	T _A = +25°C		Units			
			Typical					
C _{IN}	Input Capacitance	V _{CC} = 1.8, 2.5V or 3.3V, V _I = 0V or V _{CC}	6		pF			
C _{OUT}	Output Capacitance	V _I = 0V or V _{CC} , V _{CC} = 1.8V, 2.5V or 3.3V	7		pF			
C _{PD}	Power Dissipation Capacitance	V _I = 0V or V _{CC} , f = 10 MHz, V _{CC} = 1.8V, 2.5V or 3.3V	20		pF			

AC Loading and Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V; 1.8 \pm 0.15V$
t_{PZH}, t_{PHZ}	GND

FIGURE 1. AC Test Circuit

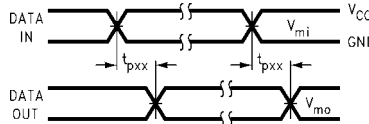


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

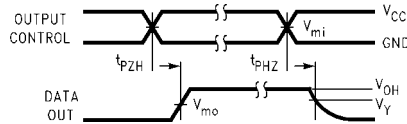


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

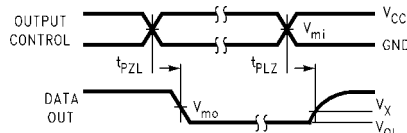
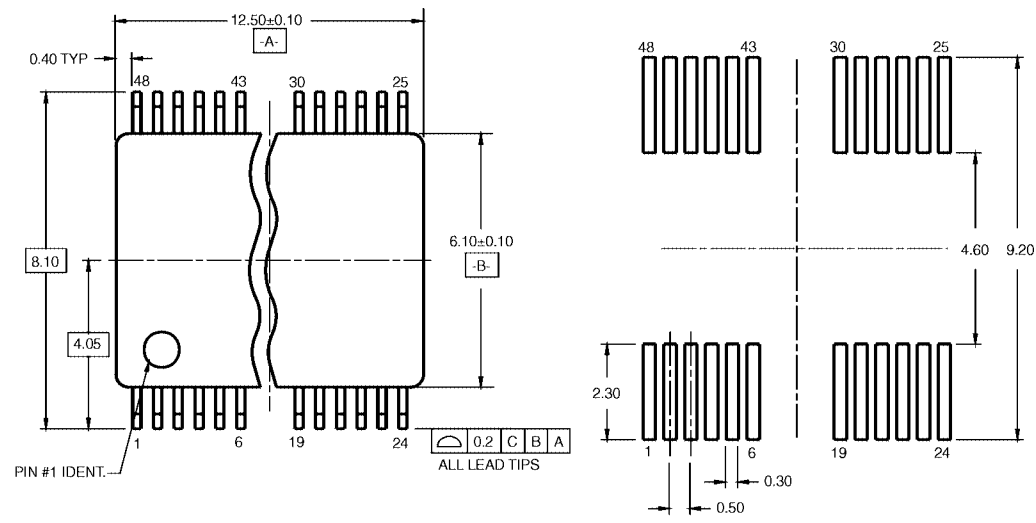


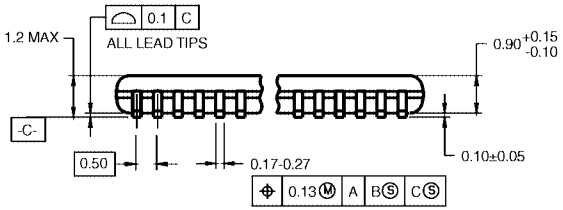
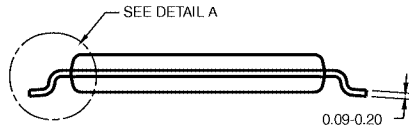
FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	V_{CC}		
	$3.3V \pm 0.3V$	$2.5V \pm 0.2V$	$1.8V \pm 0.15V$
V_{mi}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
V_Y	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

Physical Dimensions inches (millimeters) unless otherwise noted



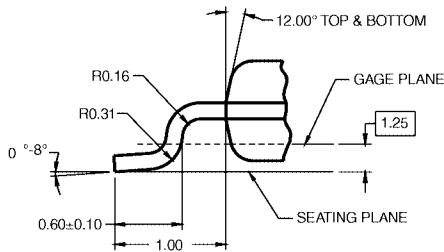
LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
 - D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48RevB1



DETAIL A

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-, 6.1mm Wide Package Number MTD48

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com