

74VHCT240A Octal Buffer/Line Driver with 3-STATE Outputs

General Description

The VHCT240A is an advanced high speed CMOS octal bus transceiver fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The VHCT240A is an inverting 3-STATE buffer having two active-LOW output enables. This device is designed to be used as 3-STATE memory address drivers, clock drivers, and bus oriented transmitter/receivers.

Protection circuits ensure that 0V to 7V can be applied to the input and output (Note 1) pins without regard to the supply voltage. These circuits prevent device destruction

due to mismatched supply and input/output voltages. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up.

Note 1: Outputs in OFF-State

Features

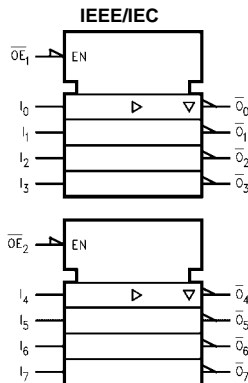
- High Speed: $t_{PD} = 5.6$ ns (typ) at $V_{CC} = 5$ V
- Power down protection is provided on inputs and outputs
- Low power dissipation: $I_{CC} = 4$ μ A (max) @ $T_A = 25^\circ$ C
- Pin and function compatible with 74HCT240

Ordering Code:

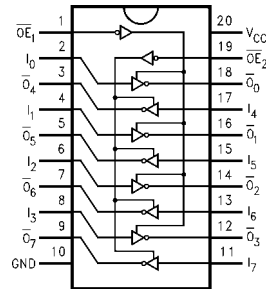
| Order Number | Package Number | Package Description |
|---------------|----------------|---|
| 74VHCT240AM | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide |
| 74VHCT240ASJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74VHCT240AMTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74VHCT240AN | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

| Pin Names | Description |
|-------------------------------------|-------------------------|
| $\overline{OE}_1, \overline{OE}_2$ | 3-STATE Output Enable |
| I_0 - I_7 | Inputs |
| \overline{O}_0 - \overline{O}_7 | Outputs 3-STATE Outputs |

Truth Tables

| Inputs | | Outputs (Pins 12, 14, 16, 18) |
|-------------------|-------|----------------------------------|
| \overline{OE}_1 | I_n | |
| L | L | H |
| L | H | L |
| H | X | Z |

| Inputs | | Outputs (Pins 3, 5, 7, 9) |
|-------------------|-------|------------------------------|
| \overline{OE}_1 | I_n | |
| L | L | H |
| L | H | L |
| H | X | Z |

H - HIGH Voltage Level
L - LOW Voltage Level
X - Immaterial
Z - High Impedance

| Absolute Maximum Ratings (Note 2) | | | Recommended Operating Conditions (Note 6) | | |
|--|--|--------------------------|--|--|--|
| Supply Voltage (V_{CC}) | | -0.5V to +7.0V | Supply Voltage (V_{CC}) | | 4.5V to +5.5V |
| DC Input Voltage (V_{IN}) | | -0.5V to +7.0V | Input Voltage (V_{IN}) | | 0V to +5.5V |
| DC Output Voltage (V_{OUT}) | | -0.5V to $V_{CC} + 0.5V$ | Output Voltage (V_{OUT}) | | 0V to V_{CC} |
| (Note 3) | | -0.5V to $V_{CC} + 0.5V$ | (Note 3) | | 0V to +5.5V |
| (Note 4) | | -0.5V to +7.0V | (Note 4) | | 0V to +5.5V |
| Input Diode Current (I_{IK}) | | -20 mA | Operating Temperature (T_{OPR}) | | -40°C to +85°C |
| Output Diode Current (I_{OK}) (Note 5) | | ± 20 mA | Input Rise and Fall Time (t_r, t_f) | | $V_{CC} = 5.0V \pm 0.5V$ 0 ns/V ~ 20 ns/V |
| DC Output Current (I_{OUT}) | | ± 25 mA | Note 2: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications. | | |
| DC V_{CC} /GND Current (I_{CC}) | | ± 75 mA | Note 3: HIGH or LOW state. I_{OUT} absolute maximum rating must be observed. | | |
| Storage Temperature (T_{STG}) | | -65°C to +150°C | Note 4: When outputs are in OFF-State or when $V_{CC} = 0V$. | | |
| Lead Temperature (T_L) | | 260°C | Note 5: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$ (Outputs Active). | | |
| (Soldering, 10 seconds) | | 260°C | Note 6: Unused inputs must be held HIGH or LOW. They may not float. | | |

| DC Electrical Characteristics | | | | | | | | | | |
|-------------------------------|---|--------------|--------------------|------|------------|--------------------------------------|-----------|---------|--|--|
| Symbol | Parameter | V_{CC} (V) | $T_A = 25^\circ C$ | | | $T_A = -40^\circ C$ to $+85^\circ C$ | | Units | Conditions | |
| | | | Min | Typ | Max | Min | Max | | | |
| V_{IH} | HIGH Level | 4.5 | 2.0 | | | 2.0 | | V | | |
| | Input Voltage | 5.5 | 2.0 | | | 2.0 | | | | |
| V_{IL} | LOW Level | 4.5 | | | 0.8 | | 0.8 | V | | |
| | Input Voltage | 5.5 | | | 0.8 | | 0.8 | | | |
| V_{OH} | HIGH Level | 4.5 | 4.40 | 4.50 | | 4.40 | | V | $V_{IN} = V_{IH}$ or V_{IL} | $I_{OH} = -50 \mu A$ $I_{OH} = -8 mA$ |
| | Output Voltage | | 3.94 | | | 3.80 | | | | |
| V_{OL} | LOW Level | 4.5 | | 0.0 | 0.1 | | 0.1 | V | $V_{IN} = V_{IH}$ or V_{IL} | $I_{OL} = 50 \mu A$ $I_{OL} = 8 mA$ |
| | Output Voltage | | | | 0.36 | | 0.44 | | | |
| I_{OZ} | 3-STATE Output Off-State Current | 5.5 | | | ± 0.25 | | ± 2.5 | μA | $V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND | |
| I_{IN} | Input Leakage Current | 0-5.5 | | | ± 0.1 | | ± 1.0 | μA | $V_{IN} = 5.5V$ or GND | |
| I_{CC} | Quiescent Supply Current | 5.5 | | | 4.0 | | 40.0 | μA | $V_{IN} = V_{CC}$ or GND | |
| I_{CCT} | Maximum I_{CC} /Input | 5.5 | | | 1.35 | | 1.50 | mA | $V_{IN} = 3.4V$ Other Input = V_{CC} or GND | |
| I_{OFF} | Output Leakage Current (Power Down State) | 0.0 | | | 0.5 | | 5.0 | μA | $V_{OUT} = 5.5V$ | |

| Noise Characteristics | | | | | | |
|-----------------------|--|--------------|--------------------|--------|-------|---------------|
| Symbol | Parameter | V_{CC} (V) | $T_A = 25^\circ C$ | | Units | Conditions |
| | | | Typ | Limits | | |
| V_{OLP} (Note 7) | Quiet Output Maximum Dynamic V_{OL} | 5.0 | 0.9 | 1.1 | V | $C_L = 50 pF$ |
| V_{OLV} (Note 7) | Quiet Output Minimum Dynamic V_{OL} | 5.0 | -0.9 | -1.1 | V | $C_L = 50 pF$ |
| V_{IHD} (Note 7) | Minimum HIGH Level Dynamic Input Voltage | 5.0 | | 2.0 | V | $C_L = 50 pF$ |
| V_{ILD} (Note 7) | Maximum LOW Level Dynamic Input Voltage | 5.0 | | 0.8 | V | $C_L = 50 pF$ |

Note 7: Parameter guaranteed by design.

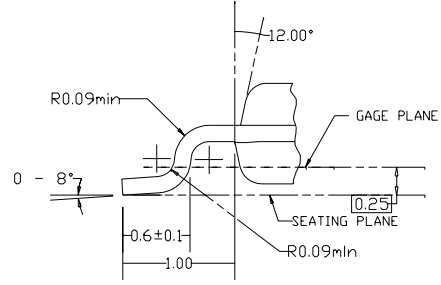
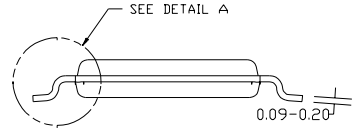
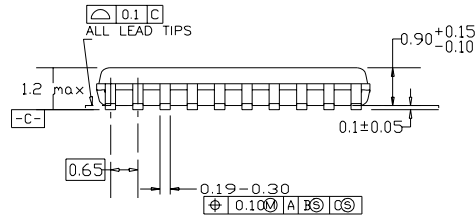
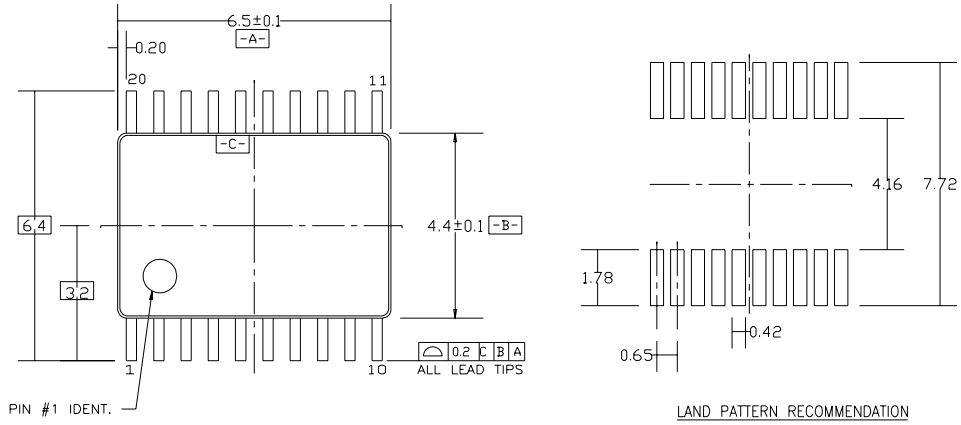
AC Electrical Characteristics

| Symbol | Parameter | V _{CC} (V) | T _A = 25°C | | | T _A = -40°C to +85°C | | Units | Conditions |
|-------------------|----------------------------------|------------------------|-----------------------|------|-----|---------------------------------|-----|---|------------|
| | | | Min | Typ | Max | Min | Max | | |
| t _{PLH} | Propagation Delay Time | 5.0 ± 0.5 | 5.6 | 7.8 | 1.0 | 9.0 | ns | C _L = 15 pF | |
| t _{PHL} | | | 6.1 | 8.8 | 1.0 | 10.0 | | C _L = 50 pF | |
| t _{PZL} | 3-STATE Output Enable Time | 5.0 ± 0.5 | 6.5 | 10.4 | 1.0 | 12.5 | ns | R _L = 1 kΩ C _L = 15 pF | |
| t _{PZH} | | | 7.3 | 11.4 | 1.0 | 13.5 | | C _L = 50 pF | |
| t _{PLZ} | 3-STATE Output Disable Time | 5.0 ± 0.5 | 7.0 | 11.4 | 1.0 | 13.0 | ns | R _L = 1 kΩ C _L = 50 pF | |
| t _{PHZ} | | | | | | | | | |
| t _{OSLH} | Output to | 5.0 ± 0.5 | | 1.0 | | 1.0 | ns | (Note 8) | |
| t _{OSHL} | Output Skew | | | | | | | | |
| C _{IN} | Input Capacitance | | 4 | 10 | | 10 | pF | V _{CC} = Open | |
| C _{OUT} | Output Capacitance | | 9 | | | | pF | V _{CC} = 5.0V | |
| C _{PD} | Power Dissipation Capacitance | | 19 | | | | pF | (Note 9) | |

Note 8: Parameter guaranteed by design. $t_{OSLH} = |t_{PLH\ max} - t_{PLH\ min}|$; $t_{OSHL} = |t_{PHL\ max} - t_{PHL\ min}|$

Note 9: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC\ (opr.)} = C_{PD} * V_{CC} * f_{IN} + I_{CC}/8$ (per F/F). The total C_{PD} when n pcs. of the Octal D Flip-Flop operates can be calculated by the equation: C_{PD} (total) = 20 + 12n.

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



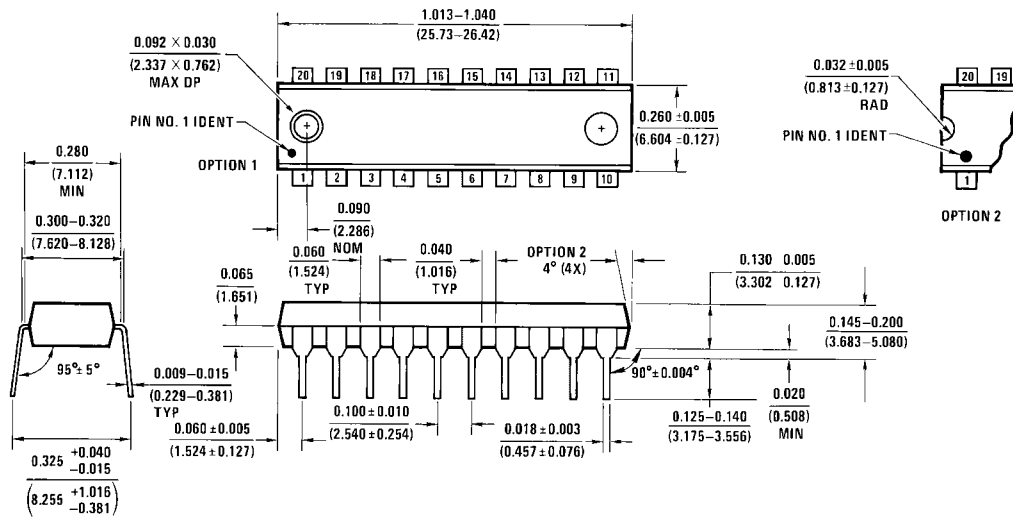
DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N20A (REV G)

**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A**

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