

## CD4724BC 8-Bit Addressable Latch

### General Description

The CD4724BC is an 8-bit addressable latch with three address inputs (A0–A2), an active low enable input ( $\bar{E}$ ), active high clear input (CL), a data input (D) and eight outputs (Q0–Q7).

Data is entered into a particular bit in the latch when that is addressed by the address inputs and the enable ( $\bar{E}$ ) is LOW. Data entry is inhibited when enable ( $\bar{E}$ ) is HIGH.

When clear (CL) and enable ( $\bar{E}$ ) are HIGH, all outputs are LOW. When clear (CL) is HIGH and enable ( $\bar{E}$ ) is LOW, the channel demultiplexing occurs. The bit that is addressed has an active output which follows the data input while all unaddressed bits are held LOW. When operating in the addressable latch mode ( $\bar{E} = \text{CL} = \text{LOW}$ ), changing more than one bit of the address could impose a transient wrong

address. Therefore, this should only be done while in the memory mode ( $\bar{E} = \text{HIGH}$ ,  $\text{CL} = \text{LOW}$ ).

### Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45  $V_{DD}$  (typ.)
- Low power TTL compatibility: fan out of 2 driving 74L or 1 driving 74LS
- Serial to parallel capability
- Storage register capability
- Random (addressable) data entry
- Active high demultiplexing capability
- Common active high clear

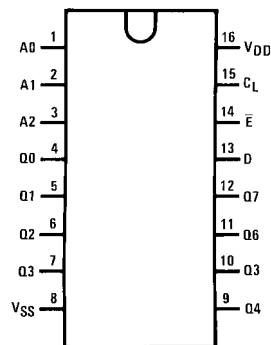
### Ordering Code:

Order Number	Package Number	Package Description
CD4724BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
CD4724BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram

Pin Assignments for DIP and SOIC

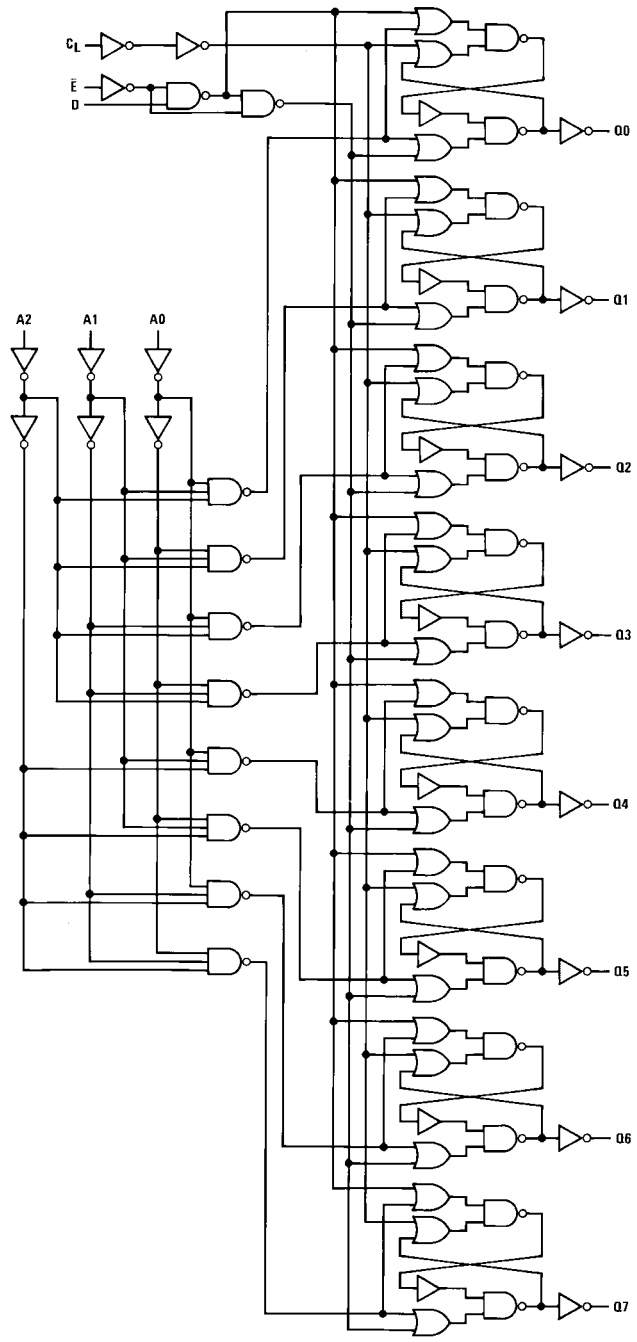


Top View

### Truth Table

Mode Selection				
$\bar{E}$	CL	Addressed Latch	Unaddressed Latch	Mode
L	L	Follows Data	Holds Previous Data	Addressable Latch
H	L	Hold Previous Data	Holds Previous Data	Memory
L	H	Follows Data	Reset to "0"	Demultiplexer
H	H	Reset to "0"	Reset to "0"	Clear

Logic Diagram



<b>Absolute Maximum Ratings</b> (Note 1)		<b>Recommended Operating Conditions</b> (Note 2)	
(Note 2)			
DC Supply Voltage ( $V_{DD}$ )	-0.5V to +18 $V_{DC}$	DC Supply Voltage ( $V_{DD}$ )	3.0V to 15 $V_{DC}$
Input Voltage ( $V_{IN}$ )	-0.5V to $V_{DD} + 0.5 V_{DC}$	Input Voltage ( $V_{IN}$ )	0V to $V_{DD} V_{DC}$
Storage Temperature ( $T_S$ )	-65°C to +150°C	Operating Temperature Range ( $T_A$ )	-40°C to +85°C
Power Dissipation ( $P_D$ )		<b>Note 1:</b> "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.	
Dual-In-Line	700 mW	<b>Note 2:</b> $V_{SS} = 0V$ unless otherwise specified.	
Small Outline	500 mW		
Lead Temperature ( $T_L$ )			
(Soldering, 10 seconds)	260°C		

**DC Electrical Characteristics** (Note 2)

Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	$V_{DD} = 5V$		20		0.02	20	150	$\mu A$	
		$V_{DD} = 10V$		40		0.02	40	300	$\mu A$	
		$V_{DD} = 15V$		80		0.02	80	600	$\mu A$	
$V_{OL}$	LOW Level Output Voltage	$ I_O  \leq 1 \mu A$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
$V_{OH}$	HIGH Level Output Voltage	$ I_O  \leq 1 \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
$V_{IL}$	LOW Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1V$ or 9V		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or 13.5V		4.0		6.75	4.0		4.0	V
$V_{IH}$	HIGH Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V, V_O = 1V$ or 9V	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or 13.5V	11.0		11.0	8.25		11.0		V
$I_{OL}$	LOW Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
$I_{OH}$	HIGH Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	-0.52		-0.44	-0.88		-0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	-1.3		-1.1	-2.25		-0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	-3.6		-3.0	-8.8		-2.4		mA
$I_{IN}$	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.30		$-10^{-5}$	-0.30		-1.0	$\mu A$
		$V_{DD} = 15V, V_{IN} = 15V$		0.30		$10^{-5}$	0.30		1.0	$\mu A$

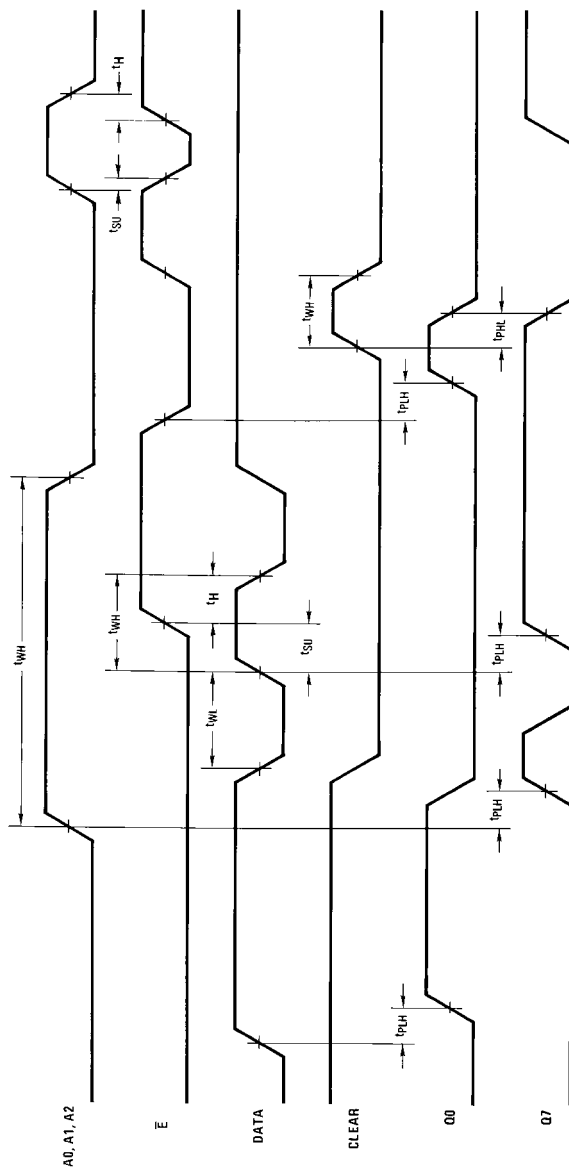
**Note 3:**  $I_{OL}$  and  $I_{OH}$  are tested one output at a time.

<b>AC Electrical Characteristics</b> (Note 4)						
T <sub>A</sub> = 25°C, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 200k, Input t <sub>r</sub> = t <sub>f</sub> = 20 ns, unless otherwise noted						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Data to Output	V <sub>DD</sub> = 5V		200	400	ns
		V <sub>DD</sub> = 10V		75	150	ns
		V <sub>DD</sub> = 15V		50	100	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Enable to Output	V <sub>DD</sub> = 5V		200	400	ns
		V <sub>DD</sub> = 10V		80	160	ns
		V <sub>DD</sub> = 15V		60	120	ns
t <sub>PHL</sub>	Propagation Delay Clear to Output	V <sub>DD</sub> = 5V		175	350	ns
		V <sub>DD</sub> = 10V		80	160	ns
		V <sub>DD</sub> = 15V		65	130	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Address to Output	V <sub>DD</sub> = 5V		225	450	ns
		V <sub>DD</sub> = 10V		100	200	ns
		V <sub>DD</sub> = 15V		75	150	ns
t <sub>THL</sub> , t <sub>TLH</sub>	Transition Time (Any Output)	V <sub>DD</sub> = 5V		100	200	ns
		V <sub>DD</sub> = 10V		50	100	ns
		V <sub>DD</sub> = 15V		40	80	ns
T <sub>WH</sub> , T <sub>WL</sub>	Minimum Data Pulse Width	V <sub>DD</sub> = 5V		100	200	ns
		V <sub>DD</sub> = 10V		50	100	ns
		V <sub>DD</sub> = 15V		40	80	ns
t <sub>WH</sub> , t <sub>WL</sub>	Minimum Address Pulse Width	V <sub>DD</sub> = 5V		200	400	ns
		V <sub>DD</sub> = 10V		100	200	ns
		V <sub>DD</sub> = 15V		65	125	ns
t <sub>WH</sub>	Minimum Clear Pulse Width	V <sub>DD</sub> = 5V		75	150	ns
		V <sub>DD</sub> = 10V		40	75	ns
		V <sub>DD</sub> = 15V		25	50	ns
t <sub>SU</sub>	Minimum Setup Time Data to E	V <sub>DD</sub> = 5V		40	80	ns
		V <sub>DD</sub> = 10V		20	40	ns
		V <sub>DD</sub> = 15V		15	30	ns
t <sub>H</sub>	Minimum Hold Time Data to E	V <sub>DD</sub> = 5V		60	120	ns
		V <sub>DD</sub> = 10V		30	60	ns
		V <sub>DD</sub> = 15V		25	50	ns
t <sub>SU</sub>	Minimum Setup Time Address to E	V <sub>DD</sub> = 5V		-15	50	ns
		V <sub>DD</sub> = 10V		0	30	ns
		V <sub>DD</sub> = 15V		0	20	ns
t <sub>H</sub>	Minimum Hold Time Address to E	V <sub>DD</sub> = 5V		-50	15	ns
		V <sub>DD</sub> = 10V		-20	10	ns
		V <sub>DD</sub> = 15V		-15	5	ns
C <sub>PD</sub>	Power Dissipation Capacitance	Per Package (Note 5)		100		pF
C <sub>IN</sub>	Input Capacitance	Any Input		5.0	7.5	pF

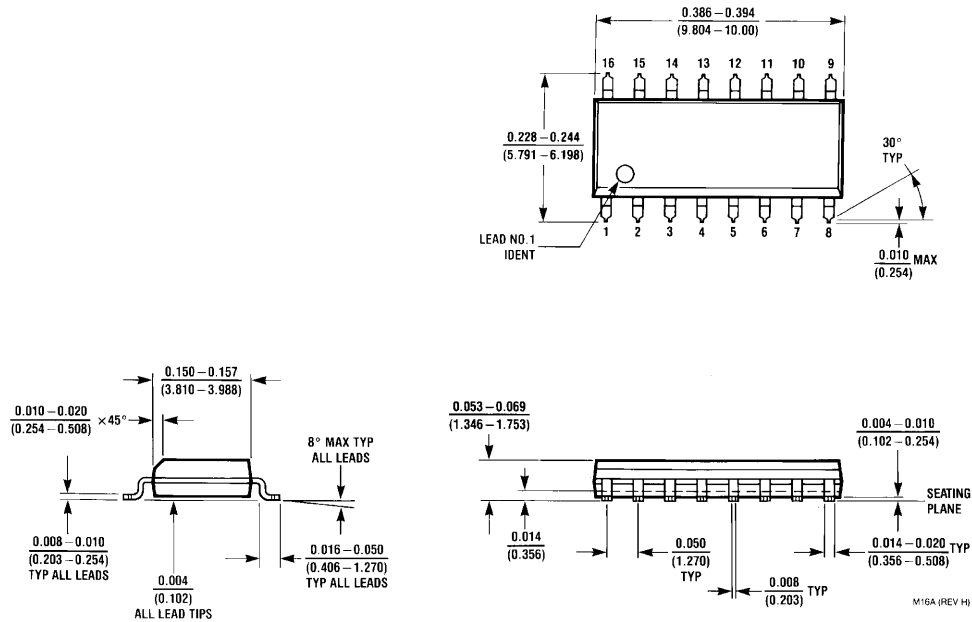
**Note 4:** AC Parameters are guaranteed by DC correlated testing.

**Note 5:** Dynamic power dissipation (P<sub>D</sub>) is given by: P<sub>D</sub> = (C<sub>PD</sub> + C<sub>L</sub>) V<sub>CC</sub><sup>2</sup>f + P<sub>Q</sub>; where C<sub>L</sub> = load capacitance; f = frequency of operation; for further details, see Application Note AN-90, "Family Characteristics".

Switching Time Waveforms

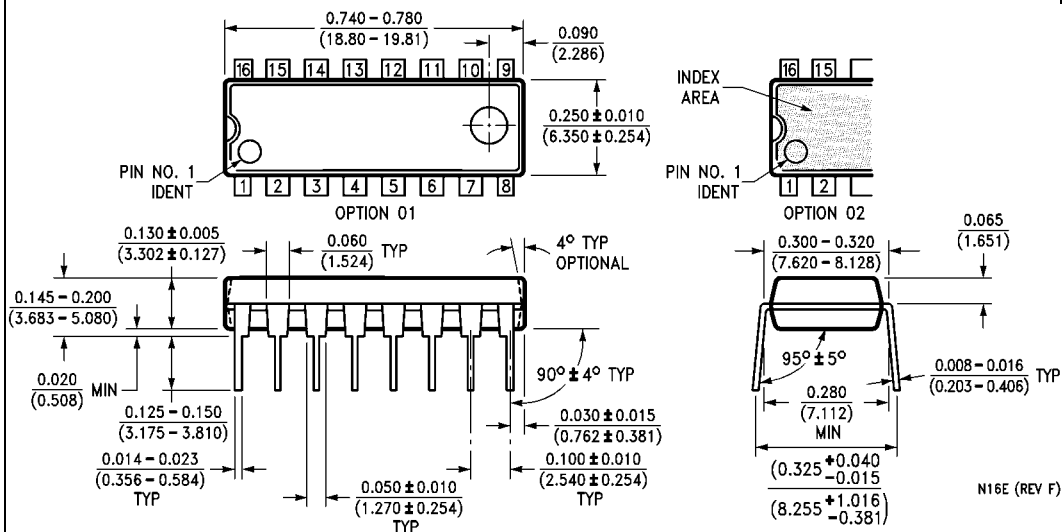


**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body  
Package Number M16A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N16E**

N16E (REV F)

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