SONY

CXA1276K

8-bit 500 MSPS Flash A/D Converter

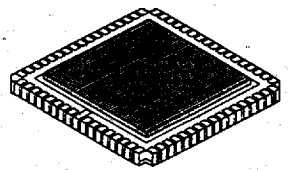
Preliminary

SONY CORP/COMPONENT PRODS T-51-10-08

Description

The CXA1276K is a 8-bit ultrahigh-speed flash A/D converter IC capable of Digitizing analog signals at a maximum rate of 500 MSPS. The digital I/O levels of these A/D converters are compatible with the ECL 100K/10KH/10K.

68 pin LCC (Ceramic)



Features

- Differential linearity error: ± 1/2 LSB or less
- Integral linearity error: ± 1/2 LSB or less
- Built-in integral linearity compensation circuit
- Ultrahigh-speed operation with maximum conversion rate of 500 MSPS (Min.)
- Low input capacitance: 16pF (Typ.)
- Wide analog input bandwidth: 250MHz (Typ. for full-scale input)
- Single power supply: –5.2V
- Low power consumption: 2.2W (Typ.)
- Low error rate
- Good temperature characteristics
- Capable of driving 50 Ω loads

Structure

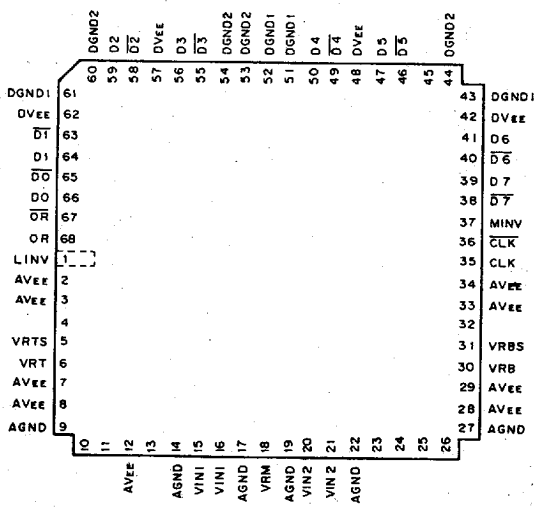
Bipolar silicon monolithic IC

Applications

- Digital oscilloscopes
- Radar
- Other apparatus requiring ultrahigh-speed A/D conversion

Pin Configuration

Pins without name are NC pins (not connected internally).



PE90618 – ST

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	AV_{EE}, DV_{EE}	−7 to +0.5	V
• Analog input voltage	V_{IN}	−2.7 to +0.5	V
• Reference input voltage	V_{RT}, V_{RB}, V_{RM}	AV_{EE} to +0.5	V
	$\lvert V_{RT}-V_{RB}\rvert$	2.5	V
• Digital input voltage	MINV, LINV	−4 to +0.5	V
	CLK, $\overline{CLK}$	DV_{EE} to +0.5	V
	$\lvert CLK-\overline{CLK}\rvert$	2.7	V
• V_{RM} pin input current	I_{VRM}	−3 to +3	mA
• Digital output current	ID_0 to ID_7, IOR, $\overline{ID_0}$ to $\overline{ID_7}$, $\overline{IOR}$	−30 to 0	mA
• Operating temperature	Ta	−25 to +100	°C
	Tc	−25 to +125	°C
• Storage temperature	Tstg	−65 to +150	°C

Operating Conditions

		Min.	Typ.	Max.	Unit
• Supply voltage	AV_{EE}, DV_{EE}	−5.5	−5.2	−4.95	V
	AV_{EE}–DV_{EE}	−0.05	0	0.05	V
	AGND–DGND	−0.05	0	0.05	V
• Reference input voltage	V_{RT}	−0.1	0	0.1	V
	V_{RB}	−2.2	−2.0	−1.8	V
• Analog input voltage	V_{IN}	V_{RB}		V_{RT}	

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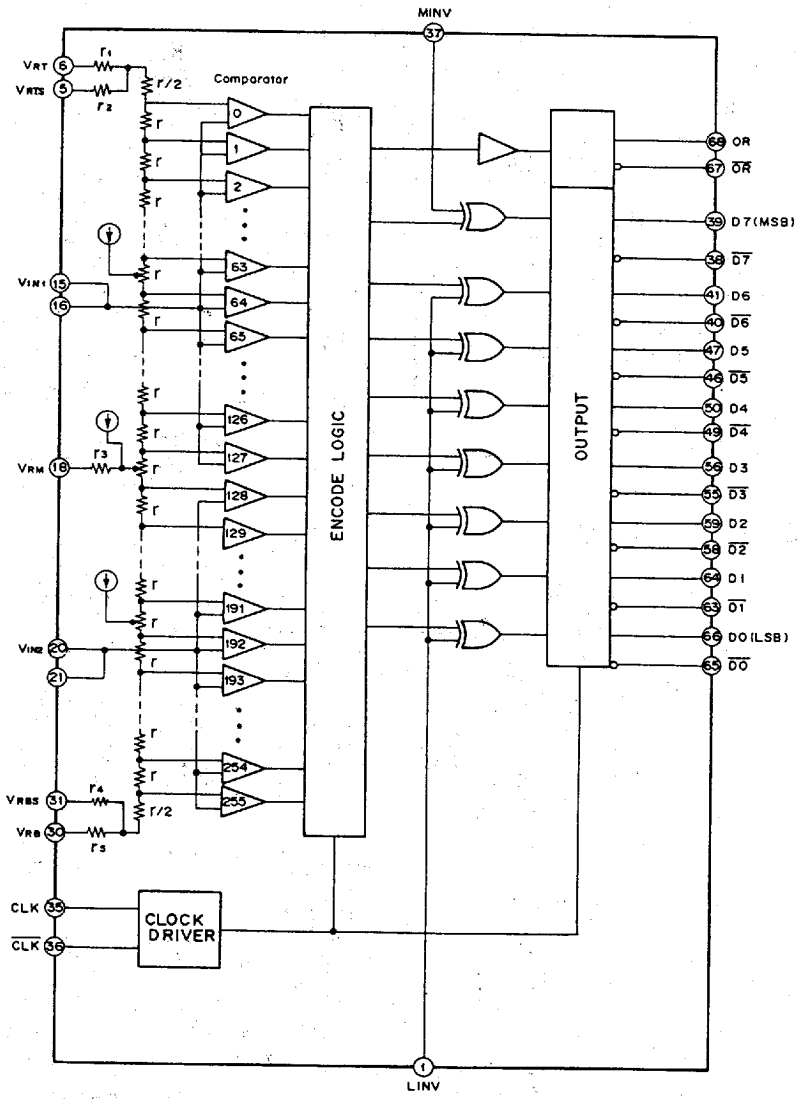
Block Diagram



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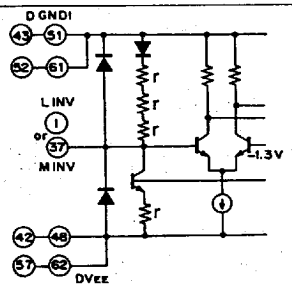
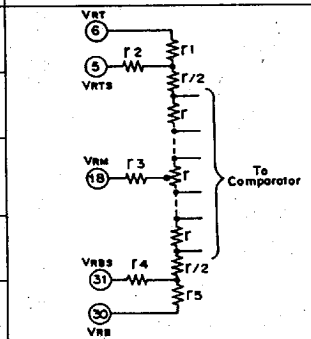
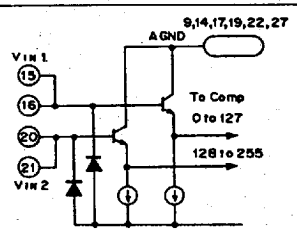
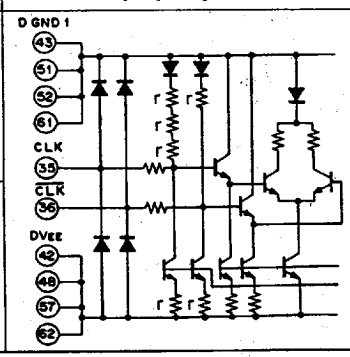
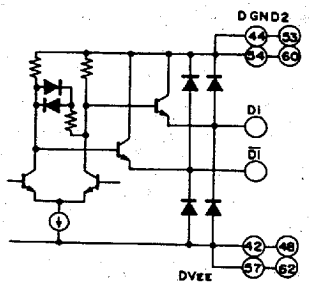
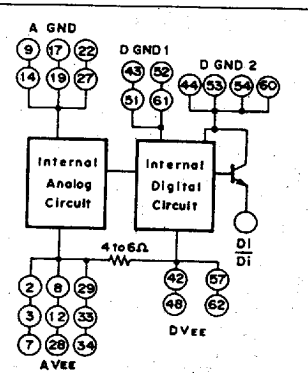
Pin Description

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
1	LINV	I	ECL		Polarity selection for LSBs. (Refer to the table of Input voltage vs. Digital output) L level is maintained with left open.
37	MINV	I	ECL		Polarity selection for MSB (Refer to the table of Input voltage vs. Digital output) L level is maintained with left open.
6	V_{RT}	I	0V		Analog reference voltage (Top) (0V Typ.)
5	V_{RTS}	O	0V		Reference voltage sense (Top)
18	V_{RM}	I	V_{RB}/2		Reference voltage mid-point It can be used for linearity compensation.
31	V_{RBS}	O	–2V		Reference voltage sense (Bottom)
30	V_{RB}	I	–2V		Analog reference voltage (Bottom)
15 16	V_{IN1}	I	V_{RTS} to V_{RBS}		Analog input All of the pins must be wired externally.
20 21	V_{IN2}				
35	CLK	I	ECL		CLK input
36	$\overline{CLK}$	I	ECL		Complementary CLK input V_{BB} (–1.3V) is maintained with left open.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
39 38	$\frac{D_7}{D_7}$	O	ECL		MSB and complementary MSB output
41 40	$\frac{D_6}{D_6}$	O	ECL		
47 46	$\frac{D_5}{D_5}$	O	ECL		
50 49	$\frac{D_4}{D_4}$	O	ECL		
56 55	$\frac{D_3}{D_3}$	O	ECL		
59 58	$\frac{D_2}{D_2}$	O	ECL		
64 63	$\frac{D_1}{D_1}$	O	ECL		D_1 to D_6: Output $\overline{D_1}$ to $\overline{D_6}$: Complementary output
66 65	$\frac{D_0}{D_0}$	O	ECL		LSB and complementary LSB output
68 67	$\frac{OR}{OR}$	O	ECL		Overrange and complementary Overrange output
2, 3, 7, 8, 12, 28, 29, 33, 34	AV_{EE} *		–5.2V		Analog supply Internally connected with DV_{EE} (resistance : 4 to 6 Ω).
9, 14, 17, 19, 22, 27	AGND *		0V		Analog ground
42, 48, 57, 62	DV_{EE} *		–5.2V		Digital supply Internally connected with AV_{EE} (resistance : 4 to 6 Ω).
43, 51, 52, 61	DGND1 *		0V		Digital ground
44, 53, 54, 60	DGND2 *		0V		Digital ground for output drive
4, 10, 11, 13, 23, 24, 25, 26, 32	NC		——		No connect pins It is recommended to wire these pins to AGND.
45	NC		——		No connect pins It is recommended to wire these pins to DGND.

* All of these pins must be wired to the respective external circiut.

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Electrical Characteristics

(AVEE=DVEE=–5.2V, VRT, VRTS=0V, VRB, VRBS=–2V)

Item	Symbol	Condition	Test level *1	Min.	Typ.	Max.	Unit
Resolution					8		bits
DC characteristics							
Integral linearity error	EIL	Fc=500MHz	II		±0.3	±0.5	LSB
Differential linearity error	EDL	Fc=500MHz	II		±0.3	±0.5	LSB
Analog input							
Analog input capacitance	CIN	VIN=–1V+0.07Vrms	IV		16		pF
Analog input resistance	RIN		IV		100		kΩ
Input bias current	IIN	VIN=–1V	IV			620	μA
Reference inputs							
Reference resistance	RREF		II		110		Ω
Frequency characteristic of reference resistance	FREF		IV		10		MHz
Residual resistance *2 r1	r1		IV		0.6		Ω
r2	r2		IV		500		Ω
r3	r3		IV		2.0		Ω
r4	r4		IV		500		Ω
r5	r5		IV		0.6		Ω
Digital inputs							
Logic H level	VIH		IV	–1.165			V
Logic L level	VIL		IV			–1.475	V
Logic H current	IIH	Input connected to GND	IV			100	μA
Logic L current	IIL	Input connected to –2V	IV	–100			μA
Input capacitance			IV		7		pF
Switching characteristics							
Maximum conversion rate	Fc		II	400			MSPS
Aperture jitter	Taj		IV		5		ps
Sampling delay	Tds		IV		1.0		ns
Output delay	Tdo		IV		2.0		ns
H pulse width of clock	TPW1		IV	1.2			ns
L pulse width of clock	TPW0		IV	1.2			ns
Digital outputs							
Logic H level	VOH	RL=50 Ω	II	–1.025			V
Logic L level	VOL	RL=50 Ω	II			–1.620	V
Output rising time	Tr	RL=50 Ω	IV		1.0		ns
Output falling time	Tf	RL=50 Ω	IV		1.0		ns

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Item	Symbol	Condition	Test level *1	Min.	Typ.	Max.	Unit
Dynamic characteristics							
Full scale input bandwidth		V_{IN}=2Vp-p	IV		300		MHz
Small-signal input bandwidth		V_{IN}=0.6Vp-p	IV		500		MHz
S/N ratio		Input=1kHz, FS, Clock=500MHz	IV		46		dB
		Input=99.999MHz, FS, Clock=500MHz	IV		40		dB
Error rate		Input=1kHz, FS, Error>16LSB, Clock=99.999MHz	IV			10^{-12}	TPS *3
		Input=62.499MHz, FS, Error>16LSB, Clock=500MHz	II			10^{-9}	TPS *3
Differential gain error	DG	NTSC 40 IRE mod. ramp, Fc=500MSPS	IV			1.0	%
Differential phase error	DP		IV			0.5	deg
Overrange recovery time			IV		1.0		ns
Power supply							
Analog supply current	I_{EEA}		II		320		mA
Digital supply current	I_{EED}		II		100		mA
Power consumption *4	Pd		II		2200		mW

*1 Test levels
I····· All-quantity test over full operating temperature range (Tc=–25 to +125 °C)
II····· All-quantity test at Tc=+25 °C
III····· Sampling test only
IV····· Design specifications
V····· Typical values only

*2 See Block Diagram
*3 TPS: times per sample
*4 $Pd=I_{EEA} \cdot AV_{EE+} I_{EED} \cdot DV_{EE+} \frac{(V_{RT}-V_{RB})^2}{R_{REF}}$

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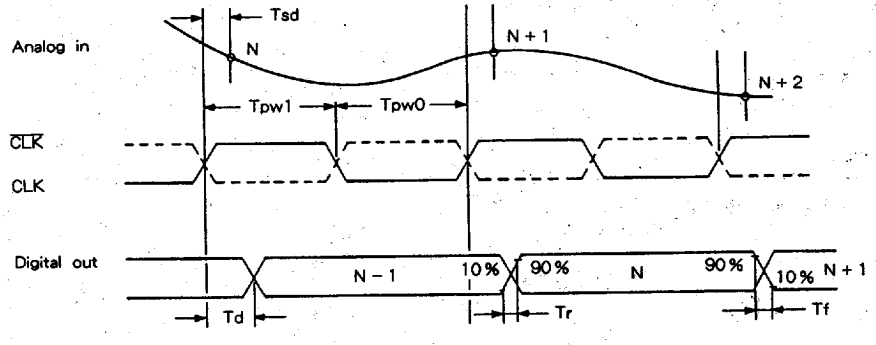
Input Voltage vs. Digital Output

V_{IN} *	Step	MINV 1 LINV 1			0 1			1 0			0 0		
		OR	D7	D0	OR	D7	D0	OR	D7	D0	OR	D0	D7
0V		0	000·····00		0	100·····00		0	011·····11		0	111·····11	
	0	1	000·····00		1	100·····00		1	011·····11		1	111·····11	
	1	1	000·····01		1	100·····01		1	011·····10		1	111·····10	
			⋮			⋮			⋮			⋮	
−1V	127	1	011·····11		1	111·····11		1	000·····00		1	100·····00	
	128	1	100·····00		1	000·····00		1	111·····11		1	011·····11	
			⋮			⋮			⋮			⋮	
	254	1	111·····10		1	011·····10		1	100·····01		1	000·····01	
	255	1	111·····11		1	011·····11		1	100·····00		1	000·····00	
−2V		1	111·····11		1	011·····11		1	100·····00		1	000·····00	

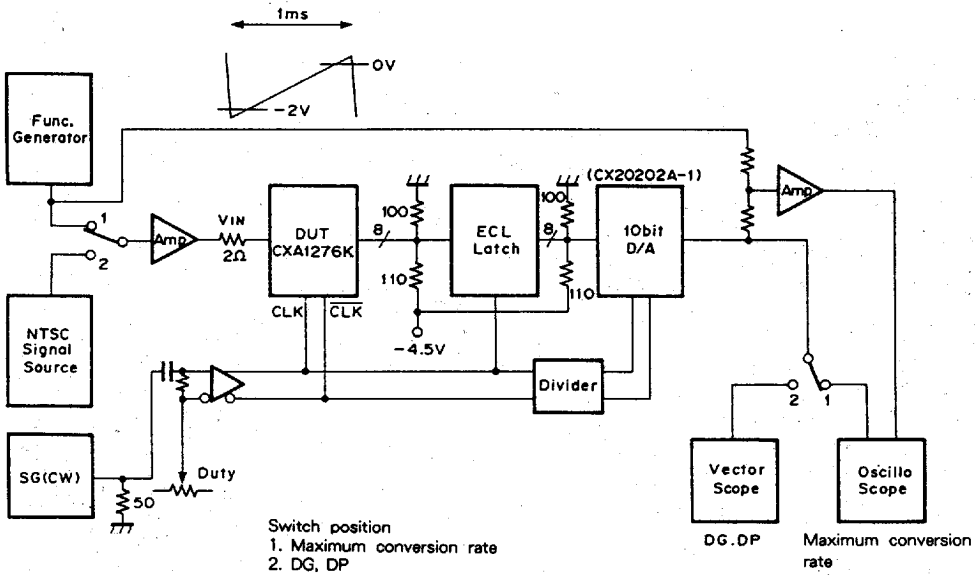
* V_{RT}=V_{RTS}=0V, V_{RM}=−1V or Open, V_{RB}=V_{RBS}=−2V

Timing Diagram

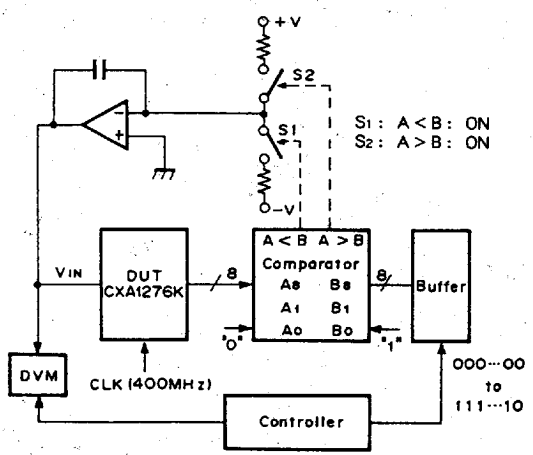


Electrical Characteristics Test Circuit

Maximum conversion rate test circuit
Differential gain error test circuit
Differential phase error test circuit



Integral linearity error test circuit
Differential linearity error test circuit



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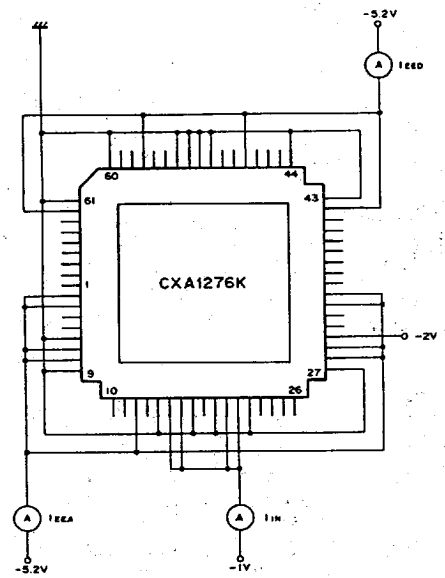
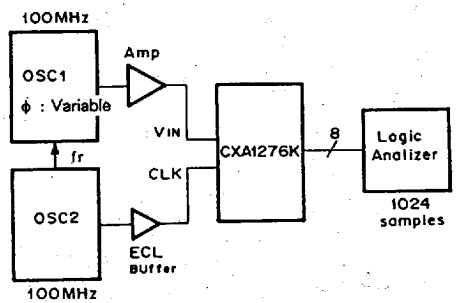
Power Supply Current Test Circuit

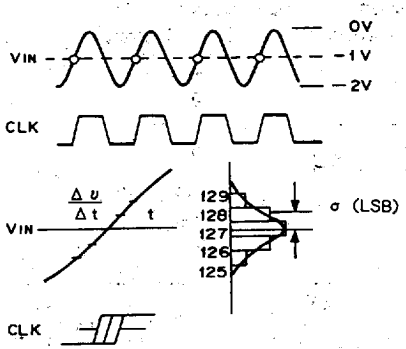
Analog Input bias current test circuit



Sampling delay test circuit
Aperture jitter test circuit



Aperture jitter test method



Aperture jitter

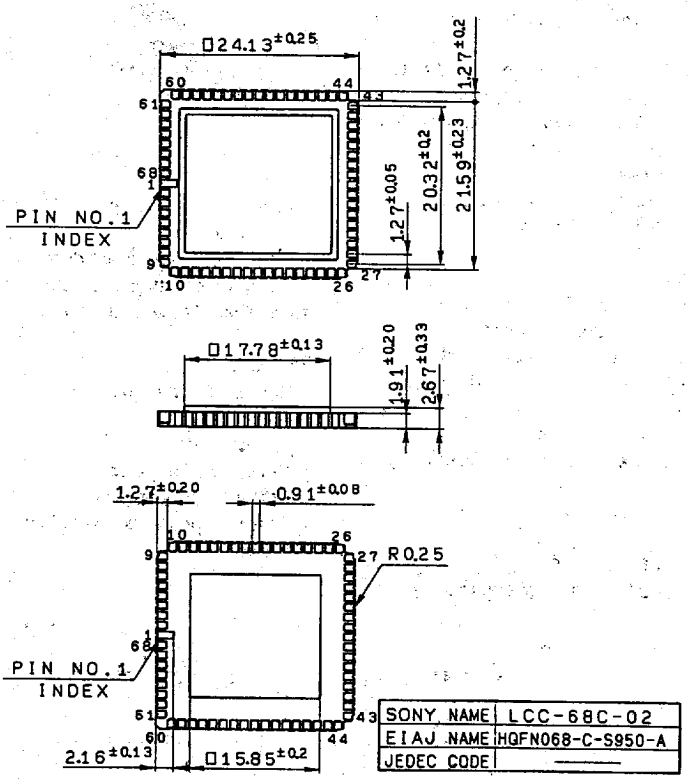
Aperture jitter is defined as follows :

$$Taj = \sigma / \frac{\Delta v}{\Delta t} = \sigma / \left(\frac{256}{2} \times 2\pi f\right),$$

Where σ (unit : LSB) is the deviation of the output codes when the input frequency is exactly the same as the clock and is sampled at the largest slew rate point.

Package Outline Unit : mm

68pin LCC (Ceramic)



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