



# M2114A

## 1024 x 4 BIT STATIC RAM

Military

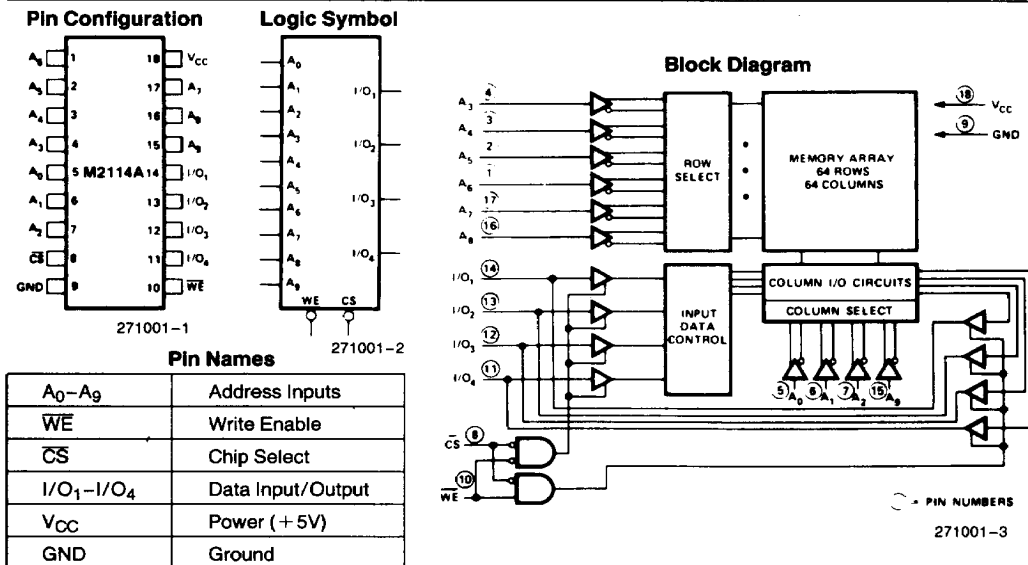
|                       | M2114AL-3 | M2114AL-4 | M2114A-4 | M2114AL-5 |
|-----------------------|-----------|-----------|----------|-----------|
| Max. Access Time (ns) | 150       | 200       | 200      | 250       |
| Max. Current (mA)     | 50        | 50        | 70       | 70        |

- **HMOS Technology**
- **Low Power, High Speed**
- **Identical Cycle and Access Times**
- **Single +5V Supply  $\pm 10\%$**
- **High Density 18-Pin Package**
- **Completely Static Memory—No Clock or Timing Strobe Required**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**
- **M2114 Upgrade**
- **Military Temperature Range**  
–55°C to +125°C (T<sub>C</sub>)
- **Not Recommended for New Designs**

The Intel M2114A is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using HMOS, a high performance MOS technology. It uses fully DC stable (static) circuitry throughout, in both the array and the decoding, therefore it requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The M2114A is designed for memory applications where the high performance and high reliability of HMOS, low cost, large bit storage, and simple interfacing are important design objectives. The M2114A is placed in an 18-pin package for the highest possible density.

It is directly TTL compatible in all respects: inputs, outputs, and a signal +5V supply. A separate Chip Select (CS) lead allows easy selection of an individual package when outputs are or-tied.



# ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias ..... -65°C to +135°C  
 Storage Temperature ..... -65°C to +150°C  
 Voltage on any Pin  
     With Respect to Ground ..... -3.5V to +7V  
 Power Dissipation ..... 1.0W  
 D.C. Output Current ..... 5 mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

*\*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

# Operating Conditions

| Symbol          | Parameter                     | Min  | Max  | Units |
|-----------------|-------------------------------|------|------|-------|
| T <sub>C</sub>  | Case Temperature (Instant On) | -55  | +125 | °C    |
| V <sub>CC</sub> | Digital Supply Voltage        | 4.50 | 5.50 | V     |

# D.C. AND OPERATING CHARACTERISTICS (Over Specified Operating Conditions)

| Symbol              | Parameter                              | M2114AL-3/L-4 |        |     | M2114A-4/-5 |        |     | Units | Comments                                                                  |
|---------------------|----------------------------------------|---------------|--------|-----|-------------|--------|-----|-------|---------------------------------------------------------------------------|
|                     |                                        | Min           | Typ(2) | Max | Min         | Typ(2) | Max |       |                                                                           |
| I <sub>LI</sub>     | Input Load Current<br>(All Input Pins) |               |        | 10  |             |        | 10  | μA    | V <sub>IN</sub> = 0 to 5.5V                                               |
| I <sub>LO</sub>     | I/O Leakage Current                    |               | 10     |     |             |        | 10  | μA    | $\overline{CS} = V_{IN}$<br>V <sub>I/O</sub> = GND to V <sub>CC</sub>     |
| I <sub>CC</sub>     | Power Supply Current                   |               | 25     | 50  |             | 50     | 70  | mA    | V <sub>CC</sub> = max, I <sub>I/O</sub> = 0 mA,<br>T <sub>C</sub> = -55°C |
| V <sub>IL</sub>     | Input Low Voltage                      | -3.0          |        | 0.8 | -3.0        |        | 0.8 | V     |                                                                           |
| V <sub>IH</sub>     | Input High Voltage                     | 2.0           |        | 6.0 | 2.0         |        | 6.0 | V     |                                                                           |
| I <sub>OL</sub>     | Output Low Current                     | 2.1           | 9.0    |     | 2.1         | 9.0    |     | mA    | V <sub>OL</sub> = 0.4V                                                    |
| I <sub>OH</sub>     | Output High Current                    | -1.0          | -2.5   |     | -1.0        | -2.5   |     | mA    | V <sub>OH</sub> = 2.4V                                                    |
| I <sub>OS</sub> (2) | Output Short Circuit                   |               |        | 40  |             |        | 40  | mA    | V <sub>OUT</sub> = GND                                                    |

## NOTES:

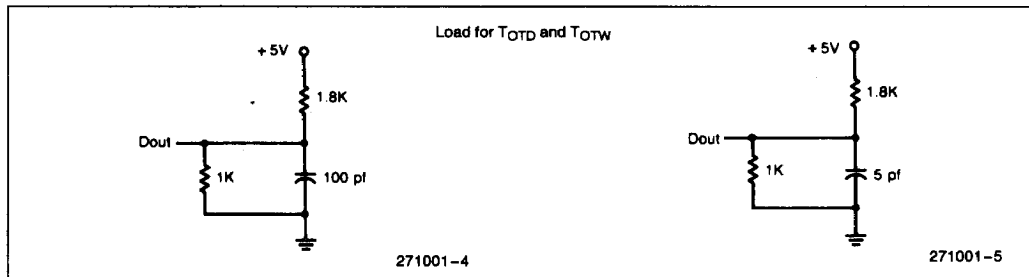
- Typical values are for T<sub>C</sub> = 25°C and V<sub>CC</sub> = 5.0V.
- Duration not to exceed 30 seconds.

**CAPACITANCE**  $T_C = 25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$

| Symbol    | Test                     | Max | Units | Conditions            |
|-----------|--------------------------|-----|-------|-----------------------|
| $C_{I/O}$ | Input/Output Capacitance | 5   | pF    | $V_{I/O} = 0\text{V}$ |
| $C_{IN}$  | Input Capacitance        | 5   | pF    | $V_{IN} = 0\text{V}$  |

**A.C. CONDITIONS OF TEST**

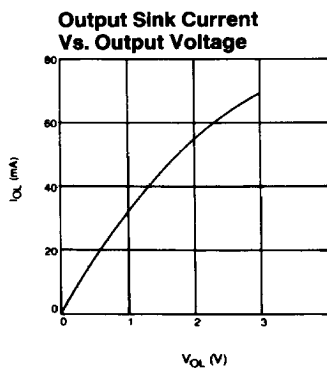
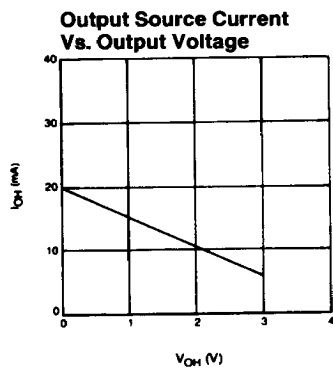
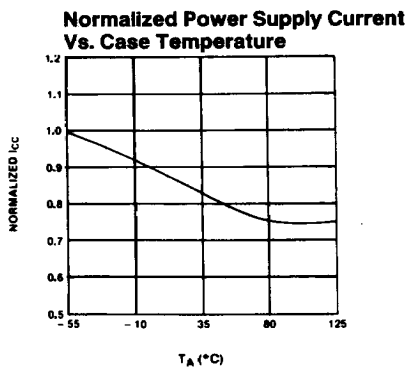
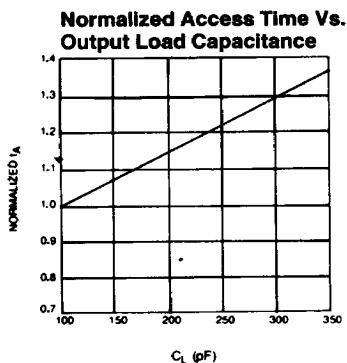
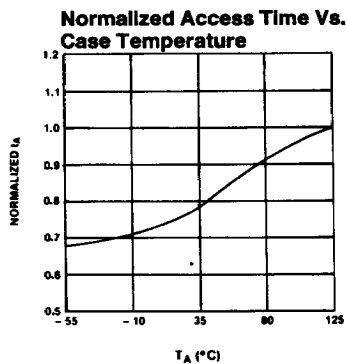
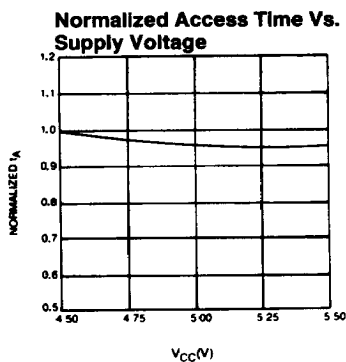
Input Pulse Levels ..... 0.8V to 2.0V  
 Input Rise and Fall Times ..... 10 ns  
 Input and Output Timing Levels ..... 1.5V  
 Output Load ..... 1 TTL Gate and  $C_L = 100\text{ pF}$



**Figure 1**

**Figure 2**

# TYPICAL D.C. AND A.C. CHARACTERISTICS



271001-6

## A.C. CHARACTERISTICS (Over Specified Operating Conditions)

### READ CYCLE<sup>(1)</sup>

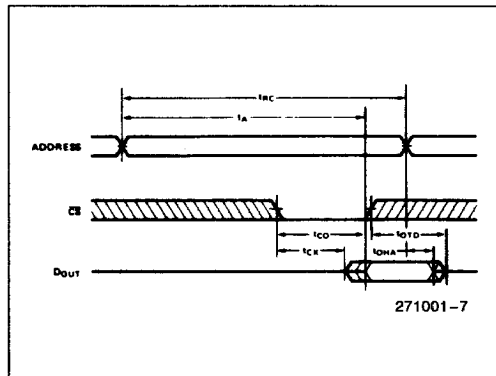
| Symbol         | Parameter                       | M2114AL-3 |     | M2114A-4/L-4 |     | M2114A-5 |     | Units |
|----------------|---------------------------------|-----------|-----|--------------|-----|----------|-----|-------|
|                |                                 | Min       | Max | Min          | Max | Min      | Max |       |
| $t_{RC}$       | Read Cycle Time                 | 150       |     | 200          |     | 250      |     | ns    |
| $t_A$          | Access Time                     |           | 150 |              | 200 |          | 250 | ns    |
| $t_{CO}$       | Chip Selection to Output Valid  |           | 70  |              | 70  |          | 85  | ns    |
| $t_{CX}^{(2)}$ | Chip Selection to Output Active | 10        |     | 10           |     | 10       |     | ns    |
| $t_{OD}^{(2)}$ | Output 3-State from Deselection |           | 40  |              | 50  |          | 60  | ns    |
| $t_{OHA}$      | Output Hold from Address Change | 15        |     | 15           |     | 15       |     | ns    |

### WRITE CYCLE<sup>(3)</sup>

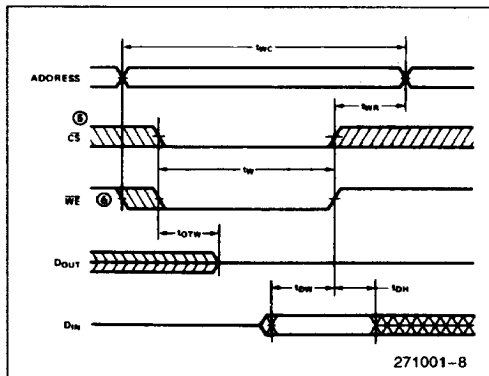
| Symbol          | Parameter                  | M2114AL-3 |     | M2114A-4/L-4 |     | M2114A-5 |     | Units |
|-----------------|----------------------------|-----------|-----|--------------|-----|----------|-----|-------|
|                 |                            | Min       | Max | Min          | Max | Min      | Max |       |
| $t_{WC}$        | Write Cycle Time           | 150       |     | 200          |     | 250      |     | ns    |
| $t_{W}^{(3)}$   | Write Time                 | 90        |     | 120          |     | 135      |     | ns    |
| $t_{WR}$        | Write Release Time         | 0         |     | 0            |     | 0        |     | ns    |
| $t_{OTW}^{(2)}$ | Output 3-State from Write  |           | 40  |              | 50  |          | 60  | ns    |
| $t_{DPW}$       | Data to Write Time Overlap | 90        |     | 120          |     | 135      |     | ns    |
| $t_{DPH}$       | Data Hold from Write Time  | 0         |     | 0            |     | 0        |     | ns    |

## WAVEFORMS

### READ CYCLE<sup>(4)</sup>



### WRITE CYCLE



#### NOTES:

1. A Read occurs during the overlap of a low  $\overline{CS}$  and a high  $\overline{WE}$ .
2. Measured at  $\pm 500$  mV with 1 TTL Gate and  $C_L = 5$  pf. Using Figure 2.
3. A Write occurs during the overlap of a low  $\overline{CS}$  and a low  $\overline{WE}$ .  $t_W$  is measured from the latter of  $\overline{CS}$  or  $\overline{WE}$  going low to the earlier of  $\overline{CS}$  or  $\overline{WE}$  going high.
4.  $\overline{WE}$  is high for a Read Cycle.
5. If the  $\overline{CS}$  low transition occurs simultaneously with the  $\overline{WE}$  low transition, the output buffers remain in a high impedance state.
6.  $\overline{WE}$  must be high during all address transitions.