FAIRCHILD SEMICONDUCTOR™

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# DM7476
# Dual Master-Slave J-K Flip-Flops with Clear, Preset, and Complementary Outputs

## General Description

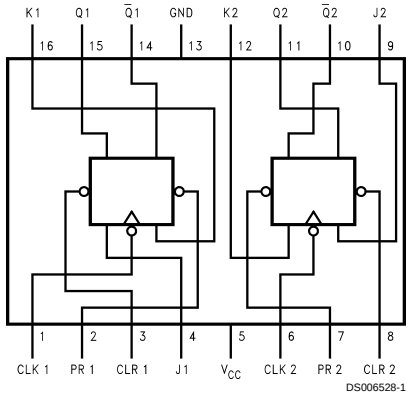
This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flop after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is high the J and K inputs are disabled. On the negative transition of the clock, the data from the master is transferred to the slave. The logic state of J and K inputs must not be allowed to change while the clock is high. The data is transfered to the outputs on the falling edge of the clock pulse. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

## Features

- Alternate Military/Aerospace device (5476) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

## Connection Diagram

**Dual-In-Line Package**




**Order Number 5476DMQB, 5476FMQB, DM5476J, DM5476W or DM7476N**
**See Package Number J16A, N16E or W16A**

## Function Table

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| **PR** | **CLR** | **CLK** | **J** | **K** | **Q** | **$\overline{Q}$** |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H (Note 1) | H (Note 1) |
| H | H | ⎍ | L | L | $Q_0$ | $\overline{Q}_0$ |
| H | H | ⎍ | H | L | H | L |
| H | H | ⎍ | L | H | L | H |
| H | H | ⎍ | H | H | Toggle | |

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
⎍ = Positive pulse data. The J and K inputs must be held constant while the clock is high. Data is transfered to the outputs on the falling edge of the clock pulse.
$Q_0$ = The output logic level before the indicated input conditions were established.
Toggle = Each output changes to the complement of its previous level on each complete active high level clock pulse.

**Note 1:** This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs return to their inactive (high) level.

## Absolute Maximum Ratings (Note 2)

| | |
|---|---|
| Supply Voltage | 7V |
| Input Voltage | 5.5V |
| Operating Free Air Temperature Range | |
| DM54 and 54 | −55˚C to +125˚C |
| DM74 | 0˚C to +70˚C |
| Storage Temperature Range | −65˚C to +150˚C |

## Recommended Operating Conditions

| Symbol | Parameter | | DM5476 | | | DM7476 | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply Voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High Level Input Voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | 0.8 | | | 0.8 | V |
| $I_{OH}$ | High Level Output Current | | | | −0.4 | | | −0.4 | mA |
| $I_{OL}$ | Low Level Output Current | | | | 16 | | | 16 | mA |
| $f_{CLK}$ | Clock Frequency (Note 8) | | 0 | | 15 | 0 | | 15 | MHz |
| $t_W$ | Pulse Width (Note 8) | Clock High | 20 | | | 20 | | | ns |
| | | Clock Low | 47 | | | 47 | | | |
| | | Preset Low | 25 | | | 25 | | | |
| | | Clear Low | 25 | | | 25 | | | |
| $t_{SU}$ | Input Setup Time (Notes 3, 8) | | 0↑ | | | 0↑ | | | ns |
| $t_H$ | Input Hold Time (Notes 3, 8) | | 0↓ | | | 0↓ | | | ns |
| $T_A$ | Free Air Operating Temperature | | −55 | | 125 | 0 | | 70 | ˚C |

**Note 2:** *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

## Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | | Min | Typ (Note 4) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | V |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $I_{OH}$ = Max<br>$V_{IL}$ = Max, $V_{IH}$ = Min | | 2.4 | 3.4 | | V |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $I_{OL}$ = Max<br>$V_{IH}$ = Min, $V_{IL}$ = Max | | | 0.2 | 0.4 | V |
| $I_I$ | Input Current @ Max Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5V | | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max<br>$V_I$ = 2.4V | J, K | | | 40 | µA |
| | | | Clock | | | 80 | |
| | | | Clear | | | 80 | |
| | | | Preset | | | 80 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max<br>$V_I$ = 0.4V<br>(Note 7) | J, K | | | −1.6 | mA |
| | | | Clock | | | −3.2 | |
| | | | Clear | | | −3.2 | |
| | | | Preset | | | −3.2 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max<br>(Note 5) | DM54 | −20 | | −55 | mA |
| | | | DM74 | −18 | | −55 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (Note 6) | | | 18 | 34 | mA |

**Note 3:** The symbol (↑, ↓) indicates the edge of the clock pulse is used for reference (↑) for rising edge, (↓) for falling edge.

**Note 4:** All typicals are at $V_{CC}$ = 5V, $T_A$ = 25˚C.

**Note 5:** Not more than one output should be shorted at a time.

**Note 6:** With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock input is grounded.

**Note 7:** Clear is measured with preset high and preset is measured with clear high.

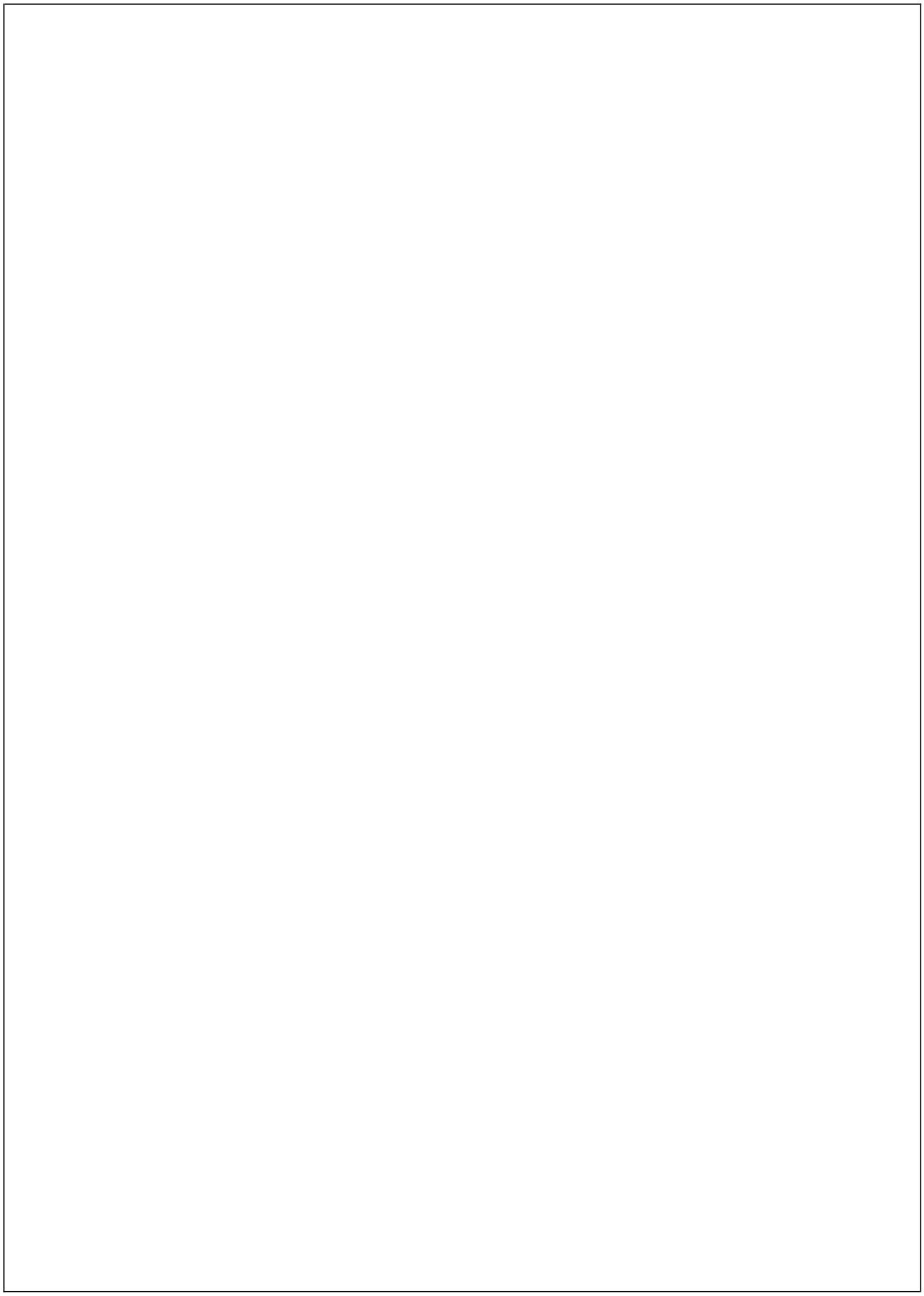
## Electrical Characteristics (Continued)

**Note 8:** $T_A = 25^\circ C$ and $V_{CC} = 5V$.

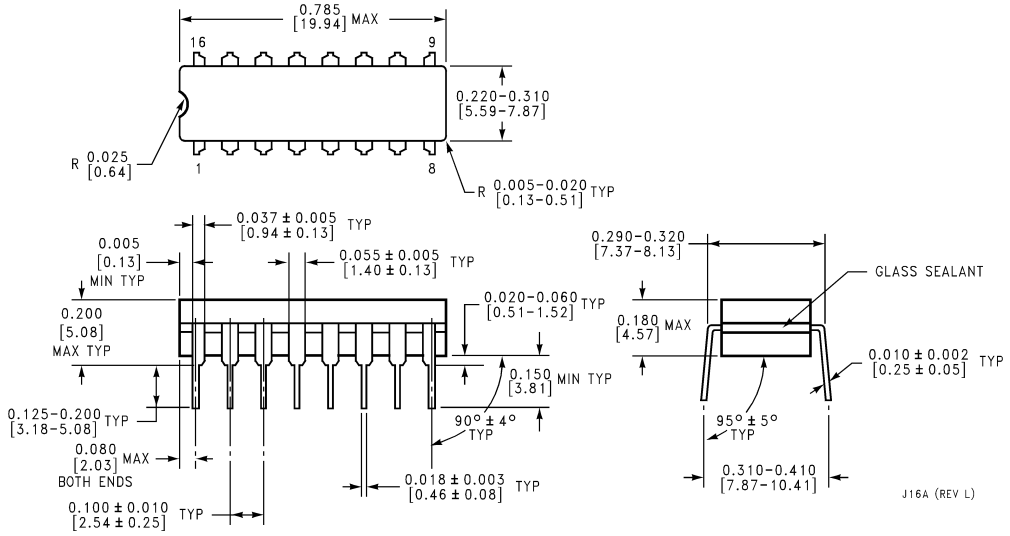
## Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25^\circ C$

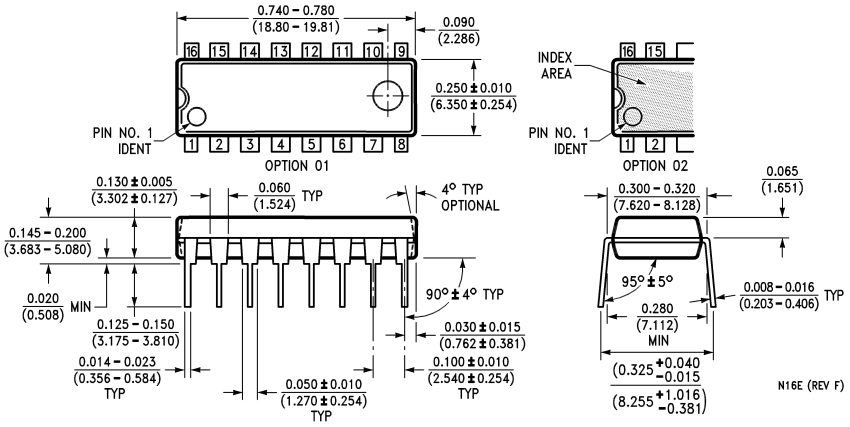
| Symbol | Parameter | From (Input) To (Output) | $R_L = 400\Omega$ $C_L = 15$ pF | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | | 15 | | MHz |
| $t_{PHL}$ | Propagation Delay Time High to Low Level Output | Preset to $\overline{Q}$ | | 40 | ns |
| $t_{PLH}$ | Propagation Delay Time Low to High Level Output | Preset to Q | | 25 | ns |
| $t_{PHL}$ | Propagation Delay Time High to Low Level Output | Clear to Q | | 40 | ns |
| $t_{PLH}$ | Propagation Delay Time Low to High Level Output | Clear to $\overline{Q}$ | | 25 | ns |
| $t_{PHL}$ | Propagation Delay Time High to Low Level Output | Clock to Q or $\overline{Q}$ | | 40 | ns |
| $t_{PLH}$ | Propagation Delay Time Low to High Level Output | Clock to Q or $\overline{Q}$ | | 25 | ns |



## Physical Dimensions inches (millimeters) unless otherwise noted

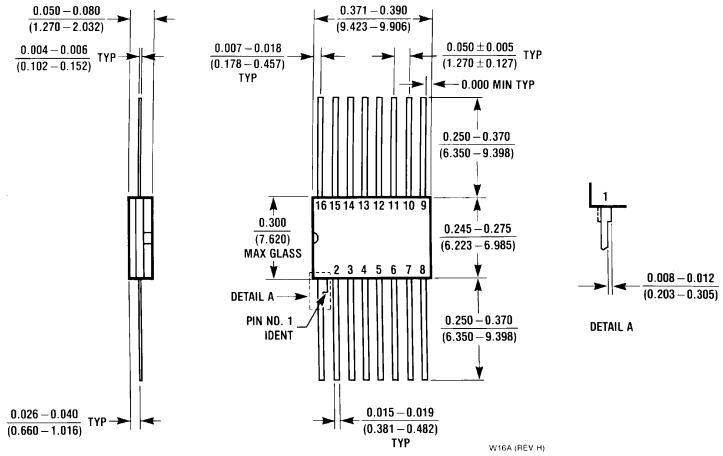



**16-Lead Ceramic Dual-In-Line Package (J)**
**Order Number 5476DMQB or DM5476J**
**Package Number J16A**




**16-Lead Molded Dual-In-Line Package (N)**
**Order Number DM7476N**
**Package Number N16E**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**16-Lead Ceramic Flat Package (W)**
**Order Number 5476FMQB or DM7476W**
**Package Number W16A**

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