FAIRCHILD SEMICONDUCTOR™

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DM74ALS109A
Dual J-$\overline{K}$ Positive-Edge-Triggered Flip-Flop with Preset and Clear

General Description

The DM54ALS109A is a dual edge-triggered flip-flop. Each flip-flop has individual J, $\overline{K}$, clock, clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input J or $\overline{K}$ is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the J, $\overline{K}$ input signal has no effect.

Asynchronous preset and clear inputs will set or clear Q output respectively upon the application of low level signal.

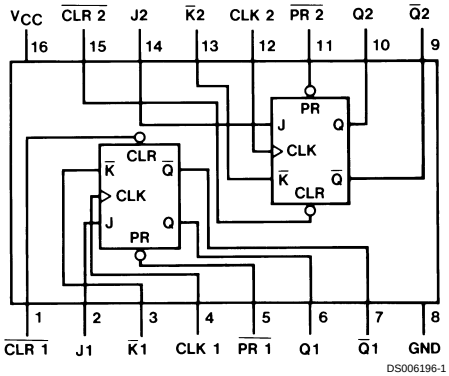
The J-$\overline{K}$ design allows operation as a D flip-flop by tying the J and $\overline{K}$ inputs together.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and LS TTL counterpart
- Improved AC performance over LS109 at approximately half the power

Connection Diagram

Dual-In-Line Package



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Order Number DM74ALS109AM or DM74ALS109AN
See Package Number M16A or N16A

Function Table

Inputs					Outputs	
$\overline{PR}$	$\overline{CLR}$	CK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H (Note 1)	H (Note 1)
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition, Q_0 = Previous Condition of Q

Note 1: This condition is nonstable; it will not persist when present and clear inputs return to their inactive (high) level. The output levels in this condition are not guaranteed to meet the V_{OH} specification.

Absolute Maximum Ratings (Note 2)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74ALS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C
Typical θ_{JA}	
N Package	82.5˚C/W
M Package	111.5˚C/W

Recommended Operating Conditions

Symbol	Parameter		DM74ALS109A			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
f_{CLK}	Clock Frequency		0		34	MHz
$t_{W(CLK)}$	Pulse Width	Clock High	14.5			ns
		Clock Low	14.5			ns
t_W	Pulse Width (Note 3)	$\overline{\text{Preset}}$ and $\overline{\text{Clear}}$	15			ns
t_{SU}	Data Setup Time	J or $\overline{K}$	15↑			ns
	(Note 3)	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	10↑			
t_H	Data Hold Time		0↑			ns
T_A	Free Air Operating Temperature		0		70	˚C

Note 2: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 3: The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free-air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25˚C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −400 µA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V	Clock, J, $\overline{K}$			0.1	mA
			$\overline{\text{Preset}}$, $\overline{\text{Clear}}$			0.2	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V	Clock, J, $\overline{K}$			20	µA
			$\overline{\text{Preset}}$, $\overline{\text{Clear}}$			40	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V	Clock, J, $\overline{K}$			−0.2	mA
			$\overline{\text{Preset}}$, $\overline{\text{Clear}}$			−0.4	
I_O (Note 5)	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V (Note 4)			2.4	4	mA

Note 4: I_{CC} is measured with J, $\overline{K}$, CLK and $\overline{\text{PRESET}}$ grounded, then with J, $\overline{K}$, CLK and $\overline{\text{CLEAR}}$ grounded.

Note 5: The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}.

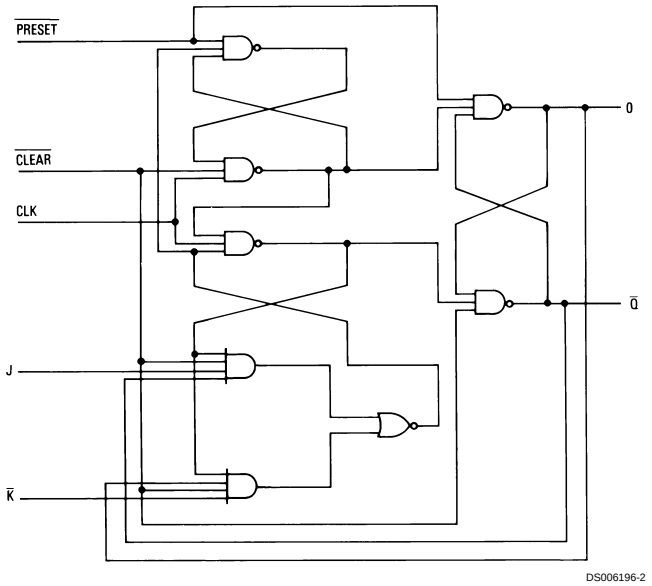
Switching Characteristics

over recommended operating free air temperature range (Note 6)

Symbol	Parameter	Conditions	From	To	DM74ALS109A		Units
					Min	Max	
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V			34		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	R_L = 500Ω C_L = 50 pF	$\overline{\text{Preset}}$ or $\overline{\text{Clear}}$	Q or $\overline{Q}$	3	13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		$\overline{\text{Preset}}$ or $\overline{\text{Clear}}$	Q or $\overline{Q}$	5	15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Q or $\overline{Q}$	5	16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Q or $\overline{Q}$	5	18	ns

Note 6: See Section 1 for test waveforms and output load.

Logic Diagram



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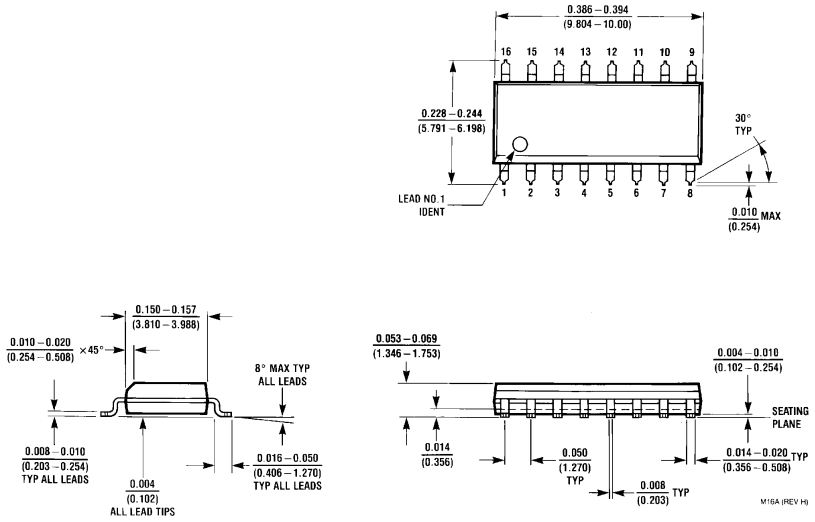
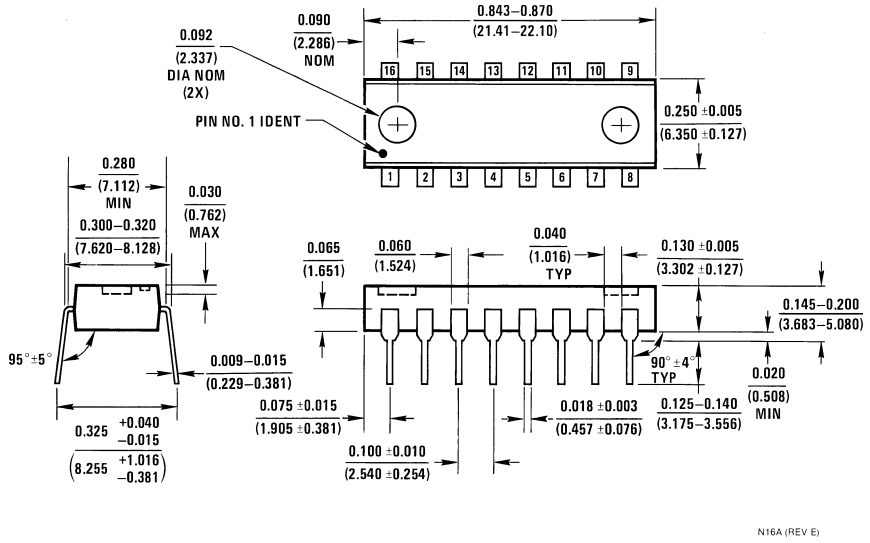
Physical Dimensions inches (millimeters) unless otherwise noted



S.O. Package (M)
Order Number DM74ALS109AM
Package Number M16A



Molded Dual-In-Line Package (N)
Order Number DM74ALS109AN
Package Number N16A

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