

DM74AS651/DM74AS652 Octal Bus Transceiver and Register

General Description

These devices incorporate an octal transceiver and an octal D-type register configured to enable transmission of data from bus to bus or internal register to bus. The 'AS651 offers 64-Industrial grade product guaranteeing performance from -40°C to $+85^{\circ}\text{C}$.

These bus transceivers feature totem-pole 3-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these devices with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The registers in the 'AS651/652 are edge-triggered D-type flip-flops. On the positive transition of the clock (CAB or CBA), the input data is stored.

The SAB and SBA control pins are provided to select whether real-time data or stored data is transferred. A low in-

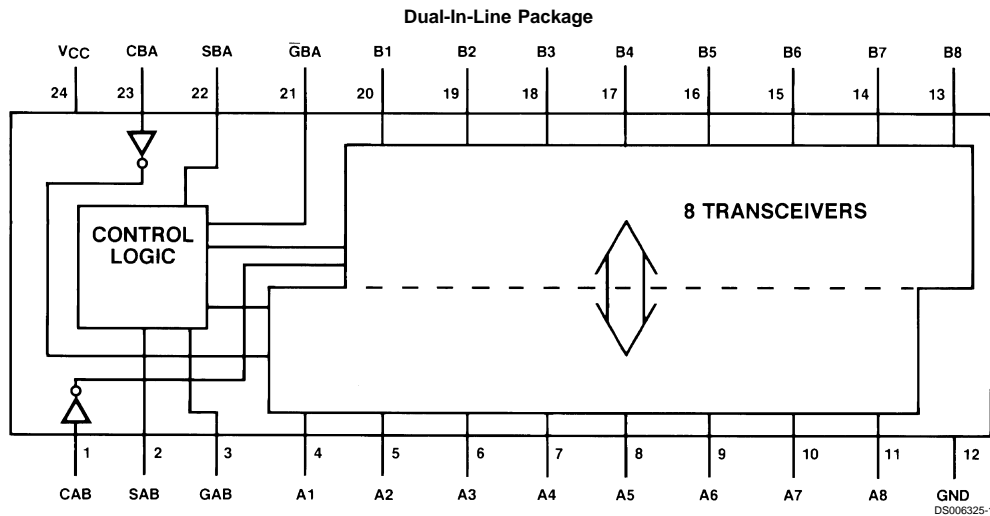
put level selects real-time data and a high level selects stored data. The select controls have a "make before break" configuration to eliminate a glitch which would normally occur in a typical multiplexer during the transition between stored and real-time data.

The Enable (GAB and $\bar{\text{G}}\text{BA}$) control pins provide four modes of operation; real-time data transfer from bus A to B, real-time data transfer from bus B to A, real-time bus A and/or B data transfer to internal storage, or internal stored data transfer to bus A and/or B.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- 3-STATE buffer-type outputs drive bus lines directly
- Guaranteed performance over industrial temperature range (-40°C to $+85^{\circ}\text{C}$) in 64-grade products

Connection Diagram



Order Number DM74AS651NT, DM74AS651WM,
DM74AS652NT or DM74AS652WM
See Package Number N24C or M24B

Absolute Maximum Ratings (Note 2)

Parameter	Value	Range	Temperature
Supply Voltage	7V	DM74AS	0°C to +70°C
Input Voltage		Storage Temperature Range	-65°C to +150°C
Control Inputs	7V	Typical θ_{JA}	
I/O Ports	5.5V	N Package	41.1°C/W
Operating Free Air Temperature		M Package	81.5°C/W

Recommended Operating Conditions

Symbol	Parameter	DM74AS651/DM74AS652			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			-15	mA
I_{OL}	Low Level Output Current			48	mA
f_{CLK}	Clock Frequency	0		90	MHz
t_{WCLK}	Width of Enable Pulse	High	5		ns
		Low	6		
t_{SU}	Data Setup Time	6			ns
t_H	Data Hold Time	0			ns
T_A	Operating Free Air Temperature	0		70	°C

Note 1: This product meets application requirements of 500 temperature cycles from -65°C to +150°C.

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at $V_{CC} = 5V$, $T_A = 25^\circ C$.

Symbol	Parameter	Conditions	DM74AS651/DM74AS652			Units		
			Min	Typ	Max			
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18 mA$			-1.2	V		
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$	$I_{OH} = \text{Max}$	2		V		
		$V_{CC} = 4.5V \text{ to } 5.5V$	$I_{OH} = -3 mA$	2.4	3.2			
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$, $I_{OL} = \text{Max}$		$V_{CC} - 2$	0.35	0.5	V	
I_I	Input Current at Max Input Voltage	$V_{CC} = 5.5V$	$V_I = 7V$	Control Inputs		0.1	mA	
			$V_I = 5.5V$	A or B Ports		0.1		
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$	Control Inputs		20	μA		
			A or B Ports		70			
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$	Control Inputs		-0.5	mA		
			A or B Ports		-0.75			
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$		-30		-112	mA	
I_{CC}	Supply Current	$V_{CC} = 5.5V$	'AS651	Outputs High		110	185	mA
				Outputs Low		120	195	
				Outputs Disabled		130	195	
			'AS652	Outputs High		120	195	
				Outputs Low		130	211	
				Outputs Disabled		130	211	

DM74AS651 Switching Characteristics

over recommended operating free air temperature range (Note 3)

Symbol	Parameter	Conditions	From	To	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 4.5V$ to $5.5V$			90		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	$R_1 = R_2 = 500\Omega$ $C_L = 50$ pF	CBA or CAB	A or B	2	8.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				2	9	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		A or B	B or A	2	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				1	7	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		SBA or SAB (Note 4)	A or B	2	11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				2	9	ns
t_{PZH}	Output Enable Time to High Level Output		Enable $\overline{G}BA$	A	2	10	ns
t_{PZL}	Output Enable Time to Low Level Output				3	16	ns
t_{PHZ}	Output Disable Time from High Level Output				2	9	ns
t_{PLZ}	Output Disable Time from Low Level Output				2	9	ns
t_{PZH}	Output Disable Time to High Level Output		Enable GAB	B	3	11	ns
t_{PZL}	Output Disable Time to Low Level Output				3	16	ns
t_{PHZ}	Output Disable Time from High Level Output				2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output				2	11	ns

Note 3: See Section 5 for test waveforms and output load.

Note 4: These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

DM74AS652 Switching Characteristics

over recommended operating free air temperature range (Note 5)

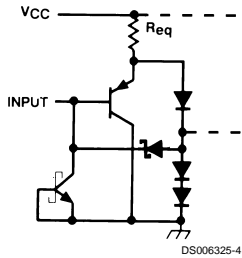
Symbol	Parameter	Conditions	From	To	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 4.5V$ to $5.5V$			90		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	$R_1 = R_2 = 500\Omega$ $C_L = 50$ pF	CBA or CAB	A or B	2	8.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				2	9	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		A or B	B or A	2	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				1	7	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		SBA or SAB (Note 6)	A or B	2	11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				2	9	ns
t_{PZH}	Output Enable Time to High Level Output		Enable $\overline{G}BA$	A	2	10	ns
t_{PZL}	Output Enable Time to Low Level Output				3	16	ns
t_{PHZ}	Output Disable Time from High Level Output				2	9	ns
t_{PLZ}	Output Disable Time from Low Level Output				2	9	ns
t_{PZH}	Output Disable Time to High Level Output		Enable GAB	B	3	11	ns
t_{PZL}	Output Disable Time to Low Level Output				3	16	ns
t_{PHZ}	Output Disable Time from High Level Output				2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output				2	11	ns

Note 5: See Section 1 for test waveforms and output load.

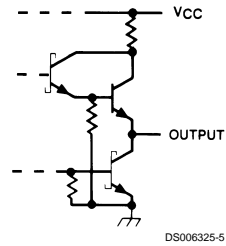
Note 6: These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

Schematics of Inputs and Outputs

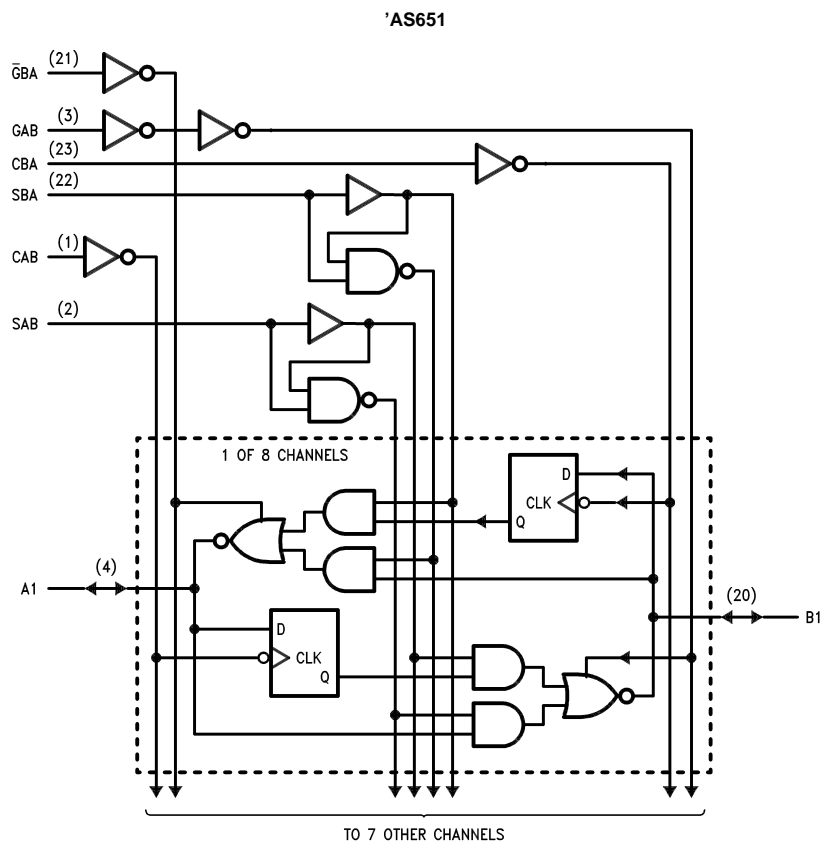
Equivalent of All Other Inputs



Typical of All 'AS651, 'AS652 Outputs

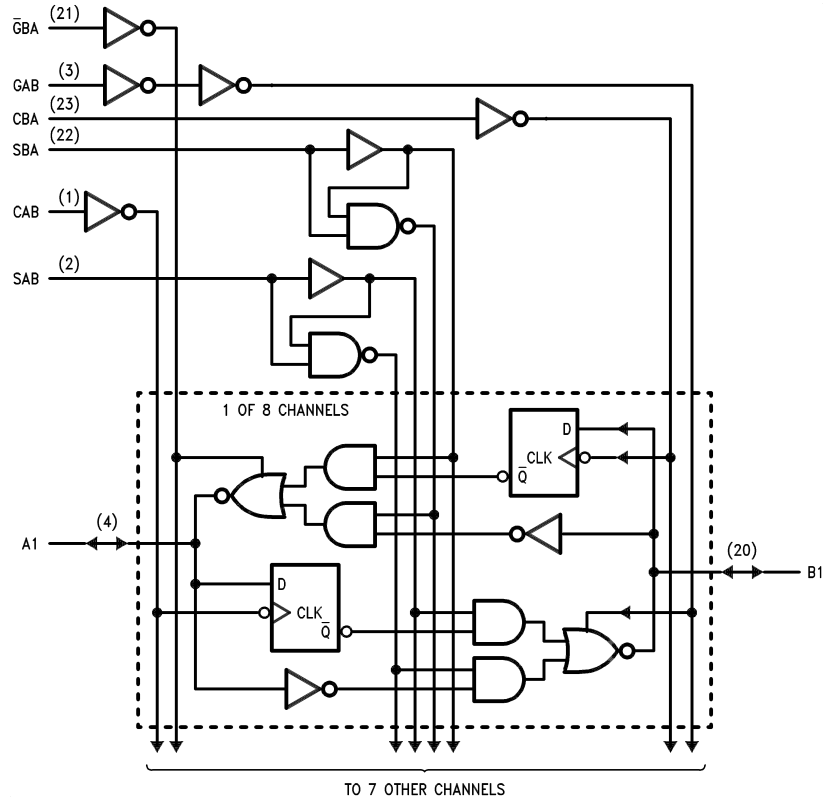


Block Diagram



Block Diagram (Continued)

'AS652



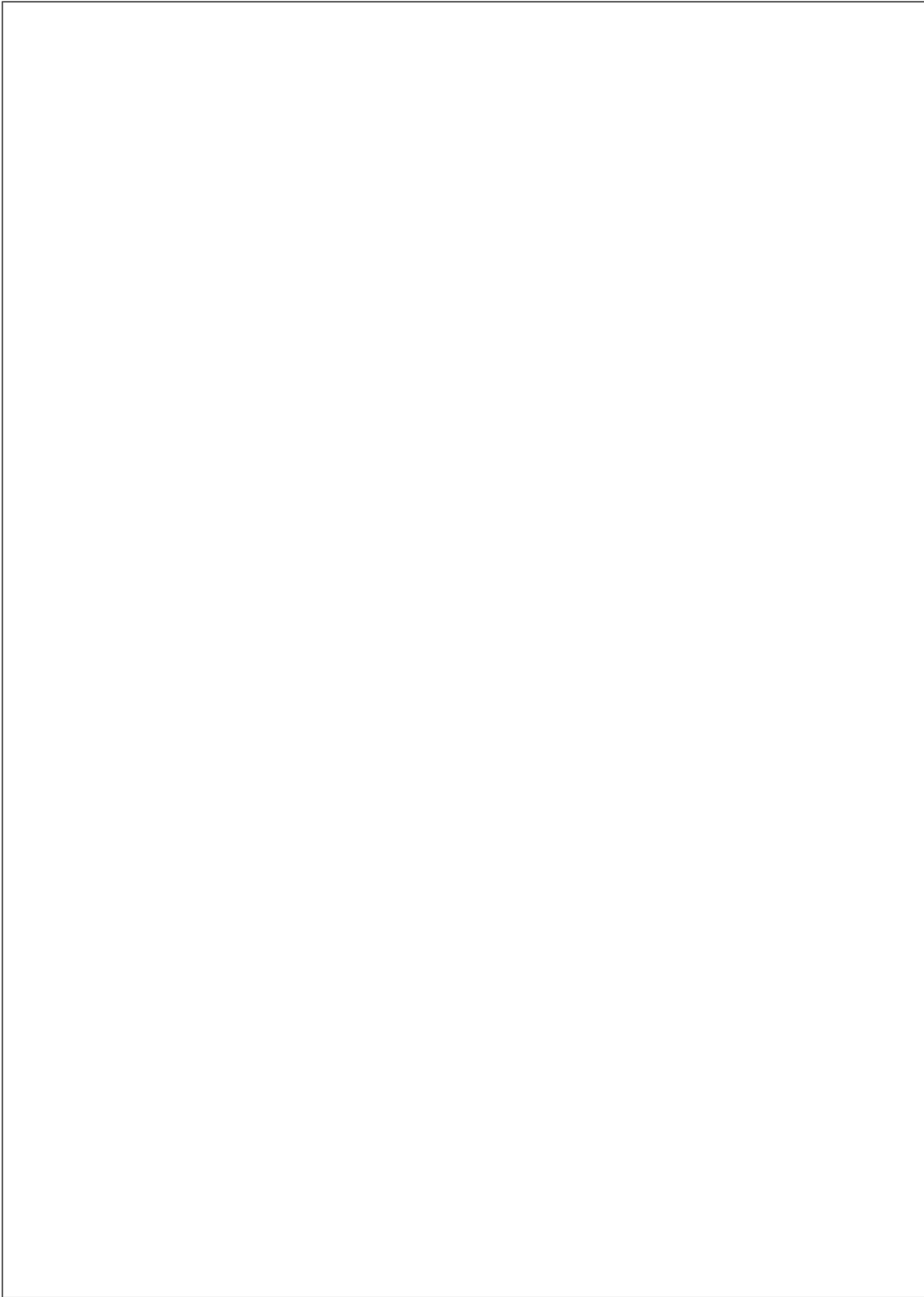
DS006325-3

Function Table

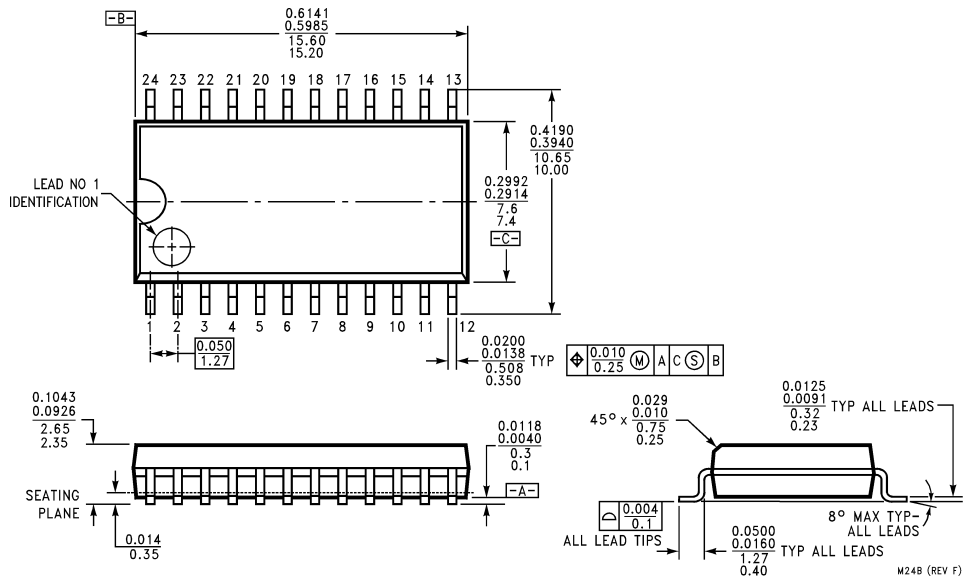
INPUTS					DATA I/O (Note 8)		OPERATION OR FUNCTION		
GAB	$\overline{\text{GBA}}$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'AS651	'AS652
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time $\overline{\text{B}}$ Data to A Bus	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{\text{B}}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real Time $\overline{\text{A}}$ Data to B Bus	Real Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{\text{A}}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{\text{A}}$ Data to B Bus & Stored $\overline{\text{B}}$ Data to A Bus	Stored A Data to B Bus & Stored B Data to A Bus
X	H	↑	H or L	X	X	Input	Unspecified (Note 8) Output	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X ⁽¹⁾	X	Input		Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified (Note 8) Output	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X ⁽¹⁾			Store B in both registers	Store B in both registers

Note 7: If the select control is low, the clocks can occur simultaneously. If the select control is high, the clocks must be staggered in order to load both registers.
H—high level L—low level X—irrelevant ↑—low-to-high transition

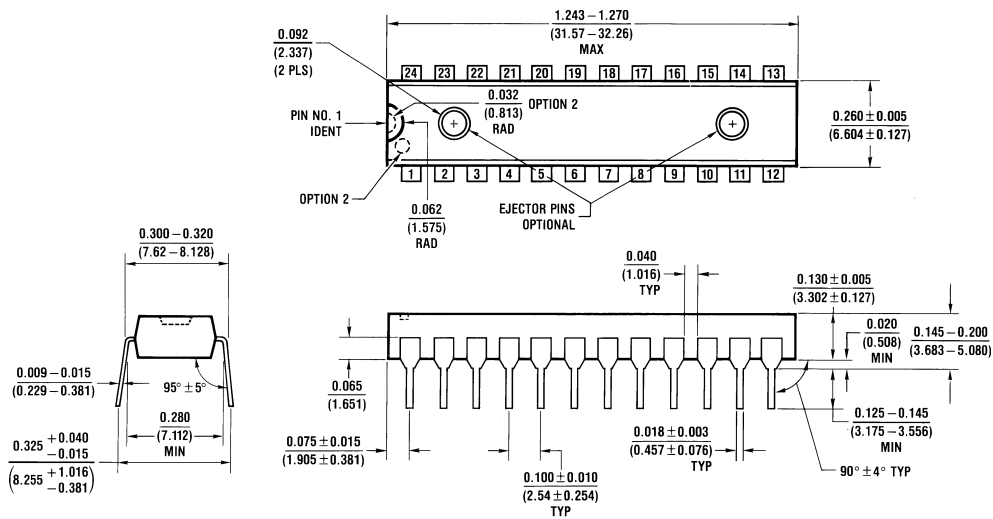
Note 8: The data output functions may be enabled or disabled by various signals at the GAB and $\overline{\text{GBA}}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.



Physical Dimensions inches (millimeters) unless otherwise noted



Wide Body S.O. Package (WM)
Order Number DM74AS651WM or DM74AS652WM
Package Number M24B



Molded Dual-In-Line Package (N)
Order Number DM74AS651NT or DM74AS652NT
Package Number N24C

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Fairchild Semiconductor Corporation Americas
Customer Response Center
Tel: 1-888-522-5372

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: +852 2737-7200
Fax: +852 2314-0061

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179

www.fairchildsemi.com