

## DM74S182 Look-Ahead Carry Generators

### General Description

These circuits are high-speed, look-ahead carry generators, capable of anticipating a carry across four binary adders or groups of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjunction with the 181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each S182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALU's are in their true form, and the carry propagate (P) and carry generate (G) are in ne-

gated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions, as explained on the 181 data sheet are also applicable to and compatible with the look-ahead generator. Positive logic equations for the S182 are:

$$C_{n+x} = \overline{G_0} + \overline{P_0} C_n$$

$$C_{n+y} = \overline{G_1} + \overline{P_1} \overline{G_0} + \overline{P_1} \overline{P_0} C_n$$

$$C_{n+z} = \overline{G_2} + \overline{P_2} \overline{G_1} + \overline{P_2} \overline{P_1} \overline{G_0} + \overline{P_2} \overline{P_1} \overline{P_0} C_n$$

$$\overline{G} = \overline{G_3} (\overline{P_3} + \overline{G_2}) (\overline{P_3} + \overline{P_2} + \overline{G_1})$$

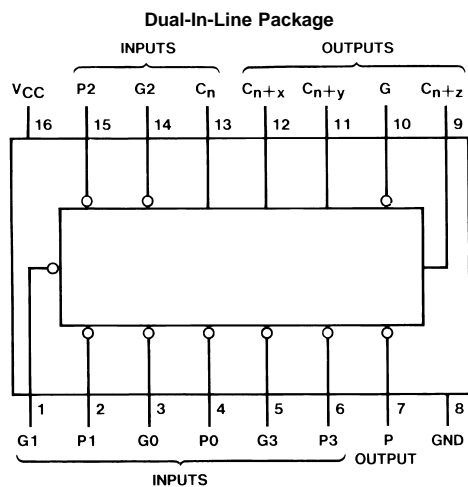
$$(\overline{P_3} + \overline{P_2} + \overline{P_1} + \overline{G_0})$$

$$\overline{P} = \overline{P_3} \overline{P_2} \overline{P_1} \overline{P_0}$$

### Features

- Typical propagation delay time 7 ns
- Typical power dissipation 260 mW

### Connection Diagram



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Order Number DM54S182J or DM74S182N  
See Package Number J16A or N16E

### Pin Designations

Designation	Pin Nos.	Function
G0, G1, G2, G3	3, 1, 14, 5	Active Low Carry Generate Inputs
P0, P1, P2, P3	4, 2, 15, 6	Active Low Carry Propagate Inputs
C <sub>n</sub>	13	Carry Input
C <sub>n+x</sub> , C <sub>n+y</sub> , C <sub>n+z</sub>	12, 11, 9	Carry Outputs
G	10	Active Low Carry Generate Output
P	7	Active Low Carry Propagate Output
V <sub>CC</sub>	16	Supply Voltage
GND	8	Ground

## Absolute Maximum Ratings (Note 1)

Supply Voltage	7V	DM54S	-55°C to +125°C
Input Voltage	5.5V	DM74S	0°C to +70°C
Operating Free Air Temperature Range		Storage Temperature Range	-65°C to +150°C

## Recommended Operating Conditions

Symbol	Parameter	DM54S182			DM74S182			Units
		Min	Nom	Max	Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High Level Input Voltage	2			2			V
V <sub>IL</sub>	Low Level Input Voltage			0.8			0.8	V
I <sub>OH</sub>	High Level Output Current			-1			-1	mA
I <sub>OL</sub>	Low Level Output Current			20			20	mA
T <sub>A</sub>	Free Air Operating Temperature	-55		125	0		70	°C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = -18 mA			-1.2	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max	DM54	2.5	3.4	
		V <sub>IL</sub> = Max, V <sub>IH</sub> = Min	DM74	2.7	3.4	
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max V <sub>IH</sub> = Min, V <sub>IL</sub> = Max			0.5	V
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 5.5V			1	mA
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max V <sub>I</sub> = 2.7V	P0, P1 or G3		200	μA
			P3		100	
			P2		150	
			C <sub>n</sub>		50	
			G0, G2		350	
			G1		400	
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max V <sub>I</sub> = 0.5V	P0, P1 or G3		-8	mA
			P3		-4	
			P2		-6	
			C <sub>n</sub>		-2	
			G0, G2		-14	
			G1		-16	
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 3)	DM54	-40	-100	mA
			DM74	-40	-100	
I <sub>CCH</sub>	Supply Current with Outputs High	V <sub>CC</sub> = Max (Note 4)	DM54	39	55	mA
			DM74	39	55	
I <sub>CCL</sub>	Supply Currents with Outputs Low	V <sub>CC</sub> = Max (Note 5)	DM54	69	99	mA
			DM74	69	109	

**Note 2:** All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

**Note 3:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

**Note 4:** I<sub>CCH</sub> is measured with all outputs open, inputs P3 and G3 at 4.5V, and all other inputs grounded.

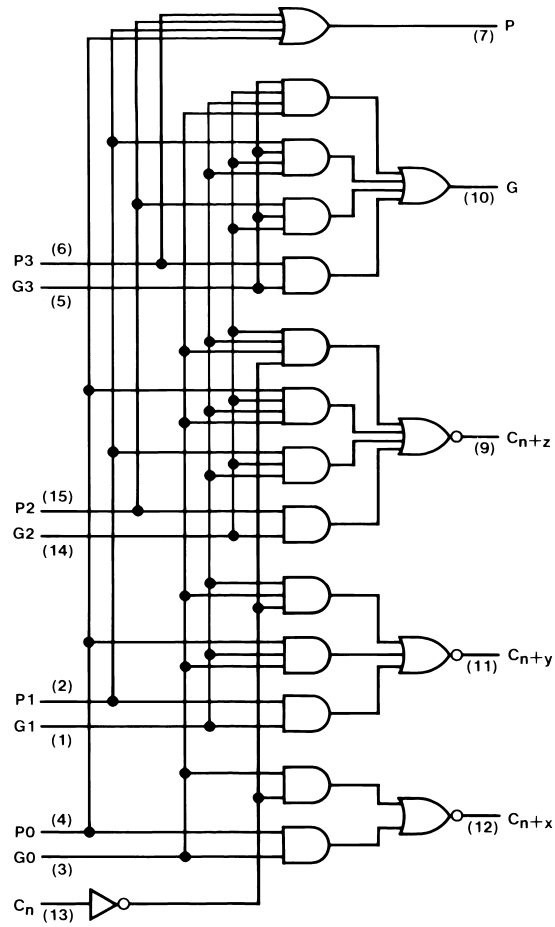
**Note 5:** I<sub>CCL</sub> is measured with all outputs open, inputs G0, G1, and G2 at 4.5V, and all other inputs grounded.

## Switching Characteristics

at  $V_{CC} = 5V$  and  $T_A = 25^\circ C$  (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 280\Omega$				Units
			$C_L = 15\text{ pF}$		$C_L = 50\text{ pF}$		
			Min	Max	Min	Min	
$t_{PLH}$	Propagation Delay Time Low to High Level Output	GN or PN to $C_{n+x, y, z}$		7		10	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	GN or PN to $C_{n+x, y, z}$		7		11	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	GN or PN to G		7.5		11	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	GN or PN to G		10.5		14	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	PN to P		6.5		10	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	PN to P		10		14	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	$C_n$ to to $C_{n+x, y, z}$		10		13	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	$C_n$ to to $C_{n+x, y, z}$		10.5		14	ns

## Logic Diagram

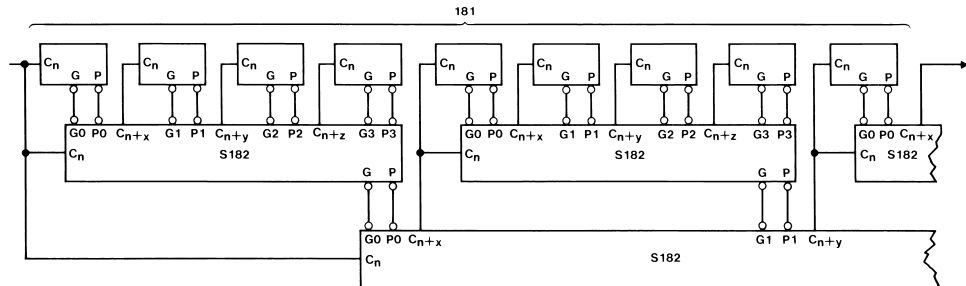


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V<sub>CC</sub> = PIN 16  
GND = PIN 8

## Typical Application

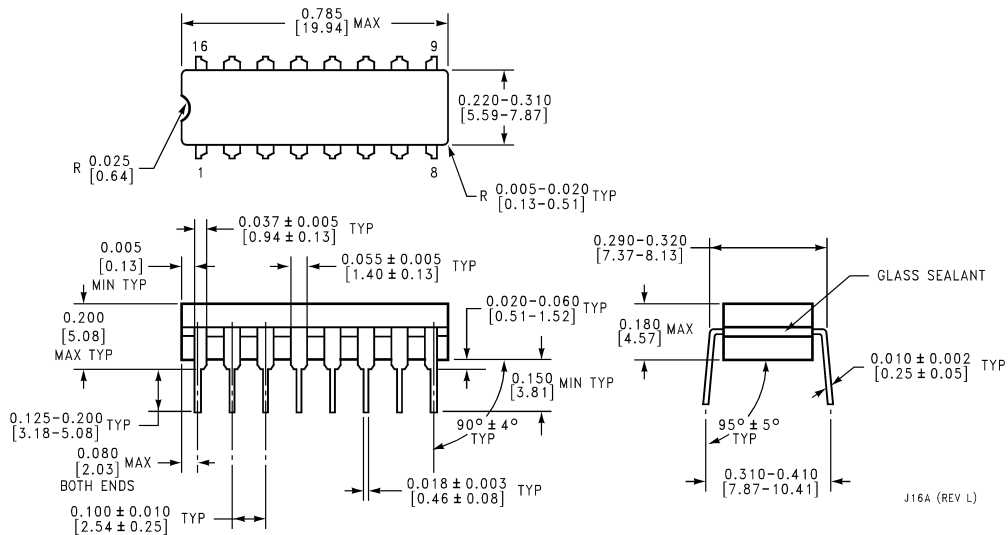
### 64-Bit ALU, Full-Carry Look Ahead in Three Levels



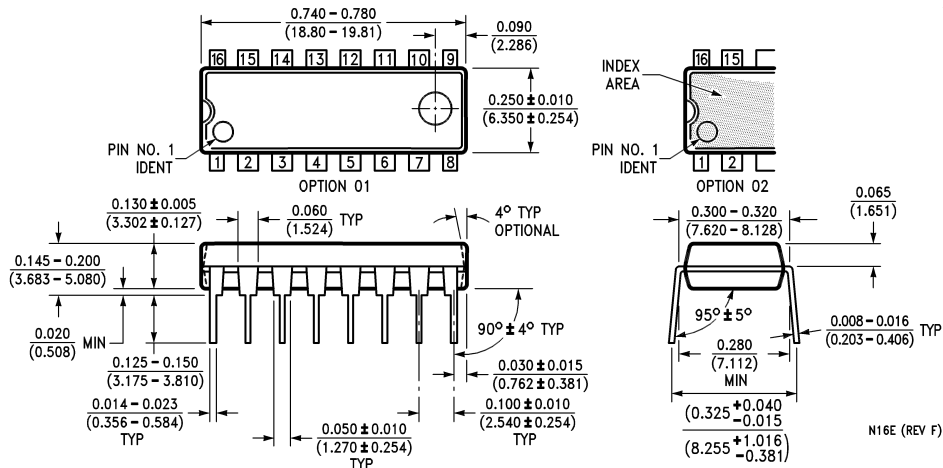
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A and B inputs, and F outputs of 181 are not shown.

**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Ceramic Dual-In-Line Package (J)**  
**Order Number DM54S182J**  
**Package Number J16A**



**16-Lead Molded Dual-In-Line Package (N)**  
**Order Number DM74S182N**  
**Package Number N16E**

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