

# DM9368

## 7-Segment Decoder/Driver/Latch with Constant Current Source Outputs

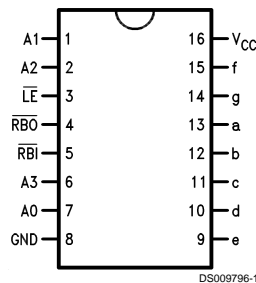
### General Description

mon cathode type LED displays directly.

The DM9368 is a 7-segment decoder driver incorporating input latches and constant current output circuits to drive com-

### Connection Diagram

Dual-In-Line Package



DS009796-1

Order Number **DM9368N**  
See Package Number **N16E**

Pin Name	Description
A0–A3	Address (Data) Inputs
$\overline{RBO}$	Ripple Blanking Output (Active Low)
$\overline{RBI}$	Ripple Blanking Input (Active Low)
a–g	Segment Drivers-Outputs
$\overline{LE}$	Latch Enable Input (Active Low)

DM9368 7-Segment Decoder/Driver/Latch with Constant Current Source Outputs

## Absolute Maximum Ratings (Note 1)

Supply Voltage  
Input Voltage

7V  
5.5V

Operating Free Air Temperature  
Range  
Storage Temperature Range

0°C to +70°C  
-65°C to +150°C

## Recommended Operating Conditions

Symbol	Parameter	DM9368			Units
		Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage	4.75	5	5.25	V
V <sub>IH</sub>	High Level Input Voltage	2			V
V <sub>IL</sub>	Low Level Input Voltage			0.8	V
I <sub>OH</sub>	High Level Output Current		-80		μA
I <sub>OL</sub>	Low Level Output Current $\overline{\text{RBO}}$			3.2	mA
T <sub>A</sub>	Free Air Operating Temperature	0		70	°C
t <sub>s</sub> (H)	Setup Time High A <sub>n</sub> to $\overline{\text{LE}}$	30			ns
t <sub>h</sub> (H)	Hold Time HIGH A <sub>n</sub> to $\overline{\text{LE}}$	0			ns
t <sub>s</sub> (L)	Setup Time LOW A <sub>n</sub> to $\overline{\text{LE}}$	20			ns
t <sub>h</sub> (L)	Hold Time LOW A <sub>n</sub> to $\overline{\text{LE}}$	0			ns
t <sub>w</sub> (L)	$\overline{\text{LE}}$ Pulse Width LOW	45			ns
I <sub>OH</sub>	Segment Output HIGH Current	-16		-22	mA
I <sub>OL</sub>	Segment Output LOW Current	-250		250	μA

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = -12 mA			-1.5	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max, V <sub>IL</sub> = Max	2.4	3.4		V
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max, V <sub>IH</sub> = Min		0.2	0.4	V
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 5.5V			1	mA
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.4V			40	μA
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V			-1.6	mA
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 2)	-18		-57	mA
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max, Outputs Open, Data & Latch Inputs = 0V			67	mA

**Note 2:** All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

**Note 3:** Not more than one output should be shorted at a time.

## Switching Characteristics

$V_{CC} = 5.0V$ ,  $T_A = 25^\circ C$  (See Section 1 for Waveforms and Load Configurations)

Symbol	Parameter	$C_L = 15\text{ pF}$ $R_L = 100\Omega$		Units
		Min	Max	
$t_{PLH}$	Propagation Delay		50	ns
$t_{PHL}$	$A_n$ to a-g		75	
$t_{PLH}$	Propagation Delay		70	ns
$t_{PHL}$	$\overline{LE}$ to a-g		90	

## Functional Description

The '68 is a 7-segment decoder driver designed to drive 7-segment common cathode LED displays. The '68 drives any common cathode LED display rated at a nominal 20 mA at 1.7V per segment without need for current limiting resistors.

This device accepts a 4-bit binary code and produces output drive to the appropriate segments of the 7-segment display. It has a hexadecimal decode format which produces numeric codes "0" thru "9" and alpha codes "A" through "F" using upper and lower case fonts.

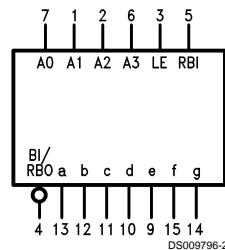
Latches on the four data inputs are controlled by an active LOW latch enable  $\overline{LE}$ . When the  $\overline{LE}$  is LOW, the state of the outputs is determined by the input data. When the  $\overline{LE}$  goes HIGH, the last data present at the inputs is stored in the latches and the outputs remain stable. The  $\overline{LE}$  pulse width necessary to accept and store data is typically 30 ns which allows data to be strobed into the '68 at normal TTL speeds. This feature means that data can be routed directly from high speed counters and frequency dividers into the display without slowing down the system clock or providing intermediate data storage.

Another feature of the '68 is that the unit loading on the data inputs is very low ( $-100\ \mu A$  Max) when the latch enable is

HIGH. This allows '68s to be driven from an MOS device in multiplex mode without the need for drivers on the data lines.

The '68 also has provision for automatic blanking of the leading and/or trailing edge zeros in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an eight digit mixed integer fraction decimal representation, using the automatic blanking capability, 0060.0300 would be displayed as 60.03. Leading edge zero suppression is obtained by connecting the Ripple Blanking Output ( $\overline{RBO}$ ) of a decoder to the Ripple Blanking Input ( $\overline{RBI}$ ) of the next lower stage device. The most significant decoder stage should have the  $\overline{RBI}$  input grounded; and since suppression of the least significant integer zero in a number is not usually desired, the  $\overline{RBI}$  input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing edge zeros. The  $\overline{RBO}$  terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of TTL or DTL gates.

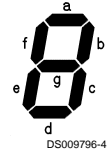
## Logic Symbol



$V_{CC} = \text{Pin } 16$   
 $GND = \text{PIN } 8$

## Truth Table

BINARY STATE	INPUTS					OUTPUTS							DISPLAY		
	$\overline{LE}$	$\overline{RBI}$	A3	A2	A1	A0	a	b	c	d	e	f		g	$\overline{RBO}$
—	H	*	X	X	X	X	← STABLE →							H	STABLE
0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	BLANK
0	L	H	L	L	L	L	H	H	H	H	H	H	L	H	0
1	L	X	L	L	L	H	L	H	H	L	L	L	L	H	1
2	L	X	L	L	H	L	H	H	L	H	H	L	H	H	2
3	L	X	L	L	H	H	H	H	H	L	L	H	H	H	3
4	L	X	L	H	L	L	L	H	H	L	L	H	H	H	4
5	L	X	L	H	L	H	H	L	H	H	L	H	H	H	5
6	L	X	L	H	H	L	H	L	H	H	H	H	H	H	6
7	L	X	L	H	H	H	H	H	L	L	L	L	H	H	7
8	L	X	H	L	L	L	H	H	H	H	H	H	H	H	8
9	L	X	H	L	L	H	H	H	L	L	H	H	H	H	9
10	L	X	H	L	H	L	H	H	L	H	H	H	H	H	0
11	L	X	H	L	H	H	L	L	H	H	H	H	H	H	1
12	L	X	H	H	L	L	H	L	L	H	H	H	L	H	2
13	L	X	H	H	L	H	L	H	H	H	L	H	H	H	3
14	L	X	H	H	H	L	H	L	L	H	H	H	H	H	4
15	L	X	H	H	H	H	H	L	L	L	H	H	H	H	5
X	X	X	X	X	X	X	L	L	L	L	L	L	L	L**	BLANK



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\*The  $\overline{RBI}$  will blank the display only if a binary zero is stored in the latches.

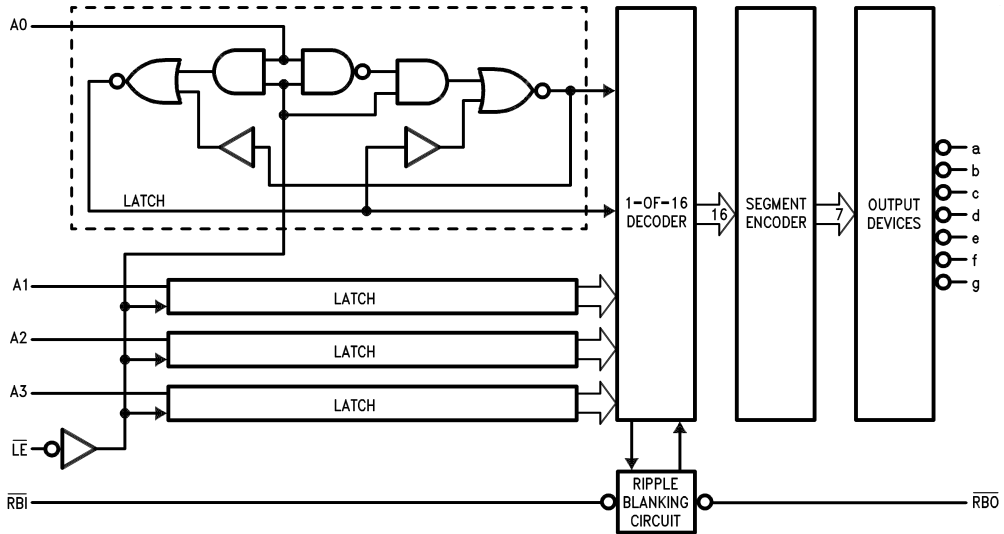
\*The  $\overline{RBO}$  used as an input overrides all other input conditions.

H = HIGH Voltage Level

L = LOW Voltage Level

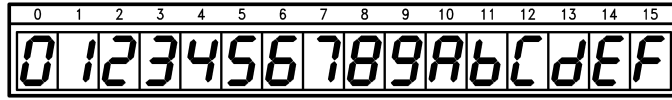
X = Immaterial

## Logic Diagram



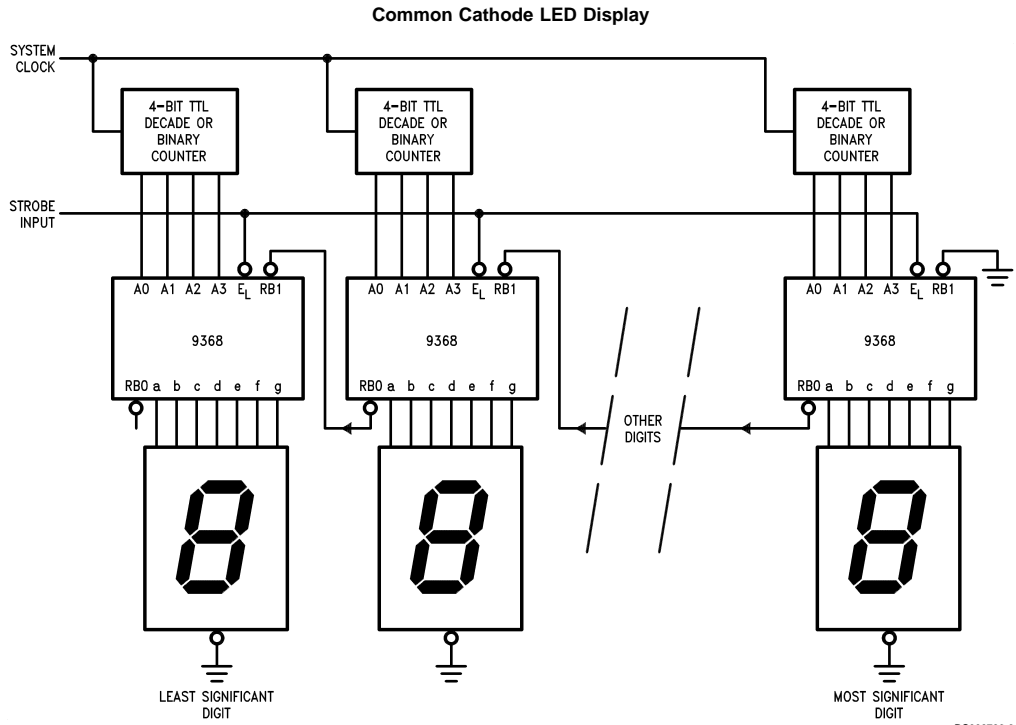
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## Numerical Designations



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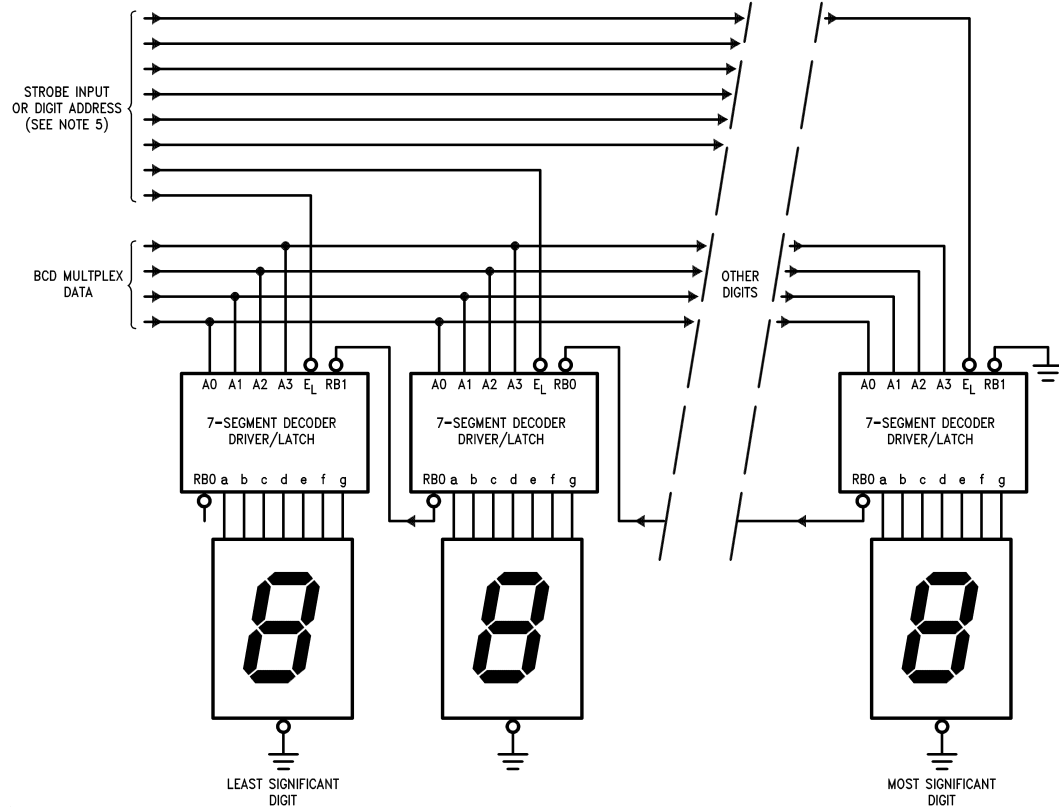
## Parallel Data Display System with Ripply Blanking



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## Display Demultiplexing System with Ripple Blanking

Common Cathode LED Display

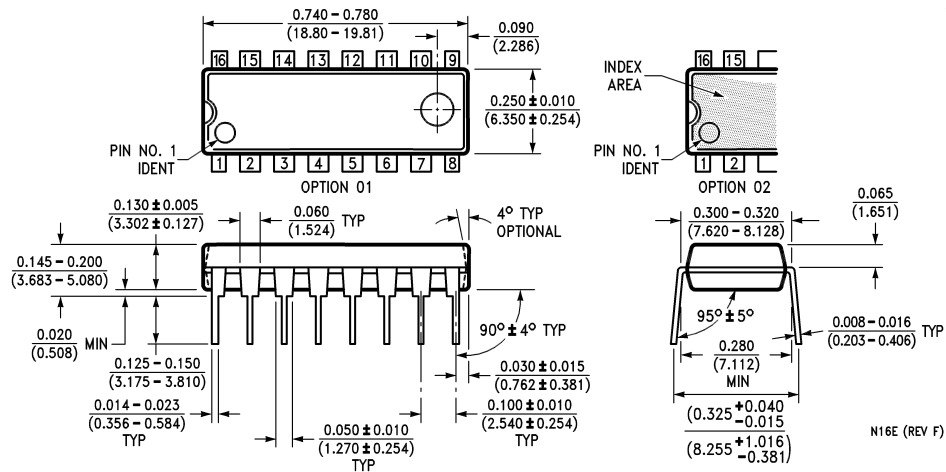


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**Note:** Digit address data must be non-overlapping. Standard TTL decoders like the 9301, 9311, 7442 or 74155 must be strobed, since the address decoding glitches could cause erroneous data to be strobed into the latches.



**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Molded Dual-In-Line Package (N)**  
**Order Number DM9368N**  
**Package Number N16E**

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