FAN5230

System Electronics Regulator for Mobile PCs

Advanced Information

Features

- Synchronous rectification
- ±1% internal reference precision
- >90% efficiency
- Input and output voltage feedback
- 5.6V to 24V input voltage range
- Internally set 300kHz frequency
- 5V and 3.3V Main outputs switch out of phase
- 5V-ALWAYS and 3.3V-ALWAYS outputs
- Stable with almost any output cap
- Adjustable boost converter for 12V
- Boost converter slaved to 5V Main
- Input UVLO
- Output OVP of Buck Converters
- Precision current limit option for 5V, 3.3V Main
- Charge pump works at all loads
- No shoot-through current
- Power Good Voltage Monitor

Applications

- Notebook PCs and PDAs
- Hand-held portable instruments

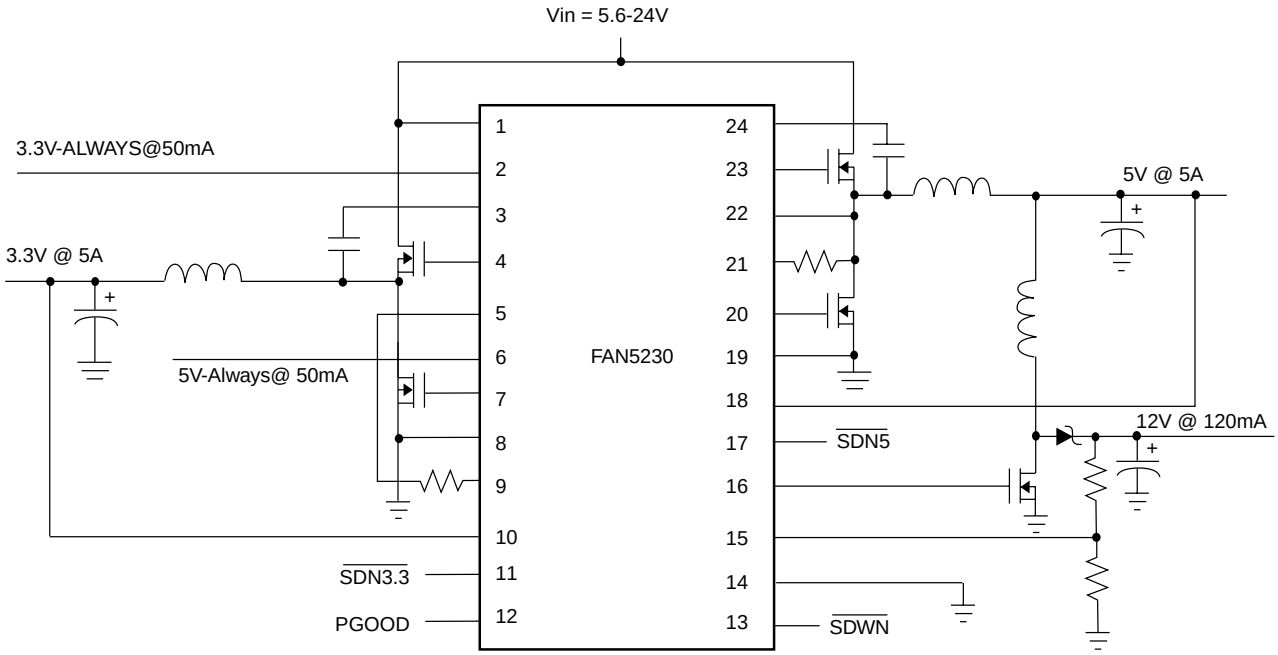
Description

The FAN5230 is a high efficiency and high precision DC/DC controller for notebook converters. Utilization of both input and output voltage feedback in a current-mode control allows for fast and stable loop response over a wide range of input and output variations. A forced-ON control loop assures a transient response of 200nsec. PWM control in normal operation and hysteretic control under light load provides best efficiency over a wide range of loads. The two main regulators switch out of phase to minimize input ripple current.

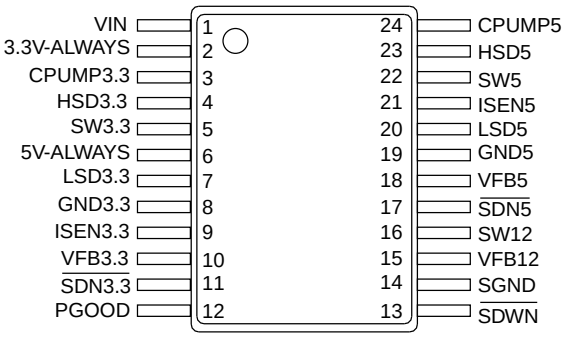
Current sense based on MOSFET R_{dson} gives maximum efficiency, while also permitting use of a sense resistor for high accuracy. An externally adjustable boost converter can be set to generate 12V.

The FAN5230 is available in a 24 pin QSOP package.

Block Diagram



Pin Assignments



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Pin Description

Pin Name	Pin Number	Pin Function Description
VIN	1	**Input Power.**
3.3V-ALWAYS	2	**3.3V ALWAYS Linear Regulator.** Load current on pins 2 and 3 must not exceed 50mA total sum.
CPUMP3.3	3	**Charge Pump 3.3V.** Gate drive voltage for 3.3V.
HSD3.3	4	**High Side FET Driver for 3.3V.** Connect this pin through a resistor to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should be <0.5".
SW3.3	5	**High Side Driver Source and Low Side Driver Drain Switching Node.** Switching node for 3.3V.
5V-ALWAYS	6	**5V ALWAYS Linear Regulator.**
LSD3.3	7	**Low Side FET Driver for 3.3V.** Connect this pin through a resistor to the gate of an N-channel MOSFET. The trace from this pin to the MOFET gate should be <0.5".
GND3.3	8	**Ground for 3.3V MOSFET.**
ISEN3.3	9	**Current Sense for 3.3V.** Together with GND pin allows low-side FET sensing of current.
VFB3.3	10	**Voltage Feedback for 3.3V.**
$\overline{\text{SDN3.3}}$	11	**Soft Start and ON/OFF for 3.3V.** OFF=0. ON=1 with $\overline{\text{SDWN}}$=1.
PGOOD	12	**Power Good Flag.** An open collector ouput that will be logic LOW if any output voltage is not within ±12% of the nominal output voltage setpoint.
$\overline{\text{SDWN}}$	13	**Master Shutdown.** Shutdown for all power =0. When =1 then 5V/3.3V-ALWAYS are ON while 5V/3.3V-Main are ready to turn on if $\overline{\text{SDN5}}$, $\overline{\text{SDN3.3}}$ go high respectively.
SGND	14	**Signal Ground.**
VFB12	15	**Voltage Feedback for 12V.**
SW12	16	**FET Driver for 12V Boost.**
$\overline{\text{SDN5}}$	17	**Enable/Soft Start for 5V and 12V.** Soft start and ON/OFF for 5V & 12V. OFF=0. ON=1 with $\overline{\text{SDWN}}$=1.
VFB5	18	**Voltage Feedback for 5V.**
GND5	19	**Ground for 5V MOSFET.**

Pin Description (Continued)

Pin Name	Pin Number	Pin Function Description
LSD5	20	**Low Side FET Driver for 5V.** Connect this pin through a resistor to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should be <0.5".
ISEN5	21	**Current Sense for 5V.** Together with GND pin allows low-side FET sensing of current.
SW5	22	**High Side Driver Source and Low Side Driver Drain Switching Node.** Switching node for 5V.
HSD5	23	**High Side FET Driver for 5V.** Connect this pin through a resistor to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should be <0.5".
CPUMP5	24	**Charge Pump 5V.** Gate drive voltage for 5V.

Absolute Maximum Ratings[1]

Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IN}				30	V
SW, ISEN Pins				30	V
CPUMP, HSD Pins				35	V
$\overline{SDWN}$ Pin				30	V
$\overline{SDN}$ Pins				7	V
Ambient Temperature, T_A		0		70	°C
Thermal Resistance, R_Θ	JA JC		88 28.5		°C/W °C/W

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

(V_{IN} = 16V, T_A = 0-70°C, circuit of Figure 8 unless otherwise specified.)

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply					
V_{IN} Input Supply Voltage		5.6		24	V
Input Quiescent Current	H/LSD Open			2	mA
	Stand-by			200	µA
	Shut-down			10	µA
Input UVLO Threshold	Rising Vbat	4.4	4.5	4.6	V
	Falling Vbat	3.9	4.0	4.1	V
5V and 3.3V Main Regulators					
Output Voltage Precision	0.1 to 5.5A, 5.6 to 24V	-2		+2	%
Oscillator Frequency, f_{osc}		255	300	345	kHz
Gate Drive On-Resistance for all Sources and HSD Sinks			4	7	Ω
Gate Drive On Resistance for LSD Sinks			2	4	Ω
HSD On Output, V_{CPUMP}-V_{GS}	I = 10µA			100	mV

Advanced Information

Operating Conditions (Continued)

(V_{IN} = 16V, T_A = 0-70°C, circuit of Figure 8 unless otherwise specified.)

Parameter	Conditions	Min.	Typ.	Max.	Units
HSD Off Output, V_{GS}	I = 10µA			100	mV
LSD On Output, $V_{5V\text{-}Always}$-V_{GS}	I = 10µA			100	mV
LSD Off Output, V_{GS}	I = 10µA			100	mV
Ramp Amplitude, pk-pk	V_{IN} = 16V		2		V
Ramp Offset			0.5		V
Ramp Gain from V_{IN}			125		mV/V
Error Amplifier GBW			3		MHz
Current Limit Threshold	R2, R8 = 1KΩ	135	150	165	mV
Over Voltage Threshold	2µs delay	115		117	%VO
Under Voltage Threshold	2µs delay			75	%VO
$\overline{SDN}$ Full On Voltage Min.		2			V
$\overline{SDN}$ Full Off Voltage Max.				800	mV
Max Duty Cycle			94		%
Min $\overline{PWM}$ Time			200		nsec
FB Input Leakage Current			50		nA
Output to Gate Forced-ON Propagation Delay			100		nsec
V_{SW} Low State	Iload=1mA Vin=5.6V			TBD	V
12V Regulator					
Output Voltage Precision	V_5 =4.9 to 5.1V and Io=0 to 150mA	-2		+2	%
V_{FB12}			2.5		V
V_{FB12} Input Current				50	nA
Oscillator Frequency (f_{osc}/3)		85	100	115	kHz
Gate Drive On-Resistance	High or Low		4	7	Ω
On Output, $V_{5V\text{-}Always}$-V_{GS}	I = 10µA			100	mV
Off Output, V_{GS}	I = 10µA			100	mV
Ramp Amplitude, pk-pk			2		V
Error Amplifier GBW			1		MHz
Under Voltage Shut Down	2µs delay			9	V
Over Current Shut Down		120		360	mA
Over Voltage Shut Down		13.2V		13.8	V
Min Duty Cycle		0			%
Max Duty Cycle		32	33	34	%
5V and 3.3V Always					
Bypass Switch $R_{DS,on}$				1	Ω
Linear Regulator Accuracy	5.6 to 24V, 0 to 50mA, 5V Main On or Off	-2		2	%
Maximum Output Current	$I_{3.3}$ + I_5	50			mA
Overcurrent Limit	2µs delay	100			mA
Undervoltage Threshold	2µs delay		75		%

Advanced Information

Operating Conditions (Continued)

(V_{IN} = 16V, T_A = 0-70°C, circuit of Figure 8 unless otherwise specified.)

Parameter	Conditions	Min.	Typ.	Max.	Units
Reference					
Reference Accuracy	0-70°C	-1		1	%
Control Functions					
$\overline{SDWN}$ Off Voltage Max.				800	mV
$\overline{SDWN}$ On Voltage Min.		3			V
Over-temperature Shutdown			150		°C
Over-temperature Hysteresis			25		°C
PGOOD Threshold	PWM Buck Converters	-14	-12	-10	$\%V_O$[1]
PGOOD Sink Current		-4			mA
PGOOD leakage				10	µA
+5V Analog Softstart	Css=100nF		22		msec
+3.3V Analog Softstart	Css=100nF		20		msec
Soft Start Current			5		µA
$\overline{PGOOD}$ Min Pulse Width		10			µs

Note:

1. A spinoff of this IC (metal option) provides a Power Good centered around –5% as opposed to the specified –12% of Vo.

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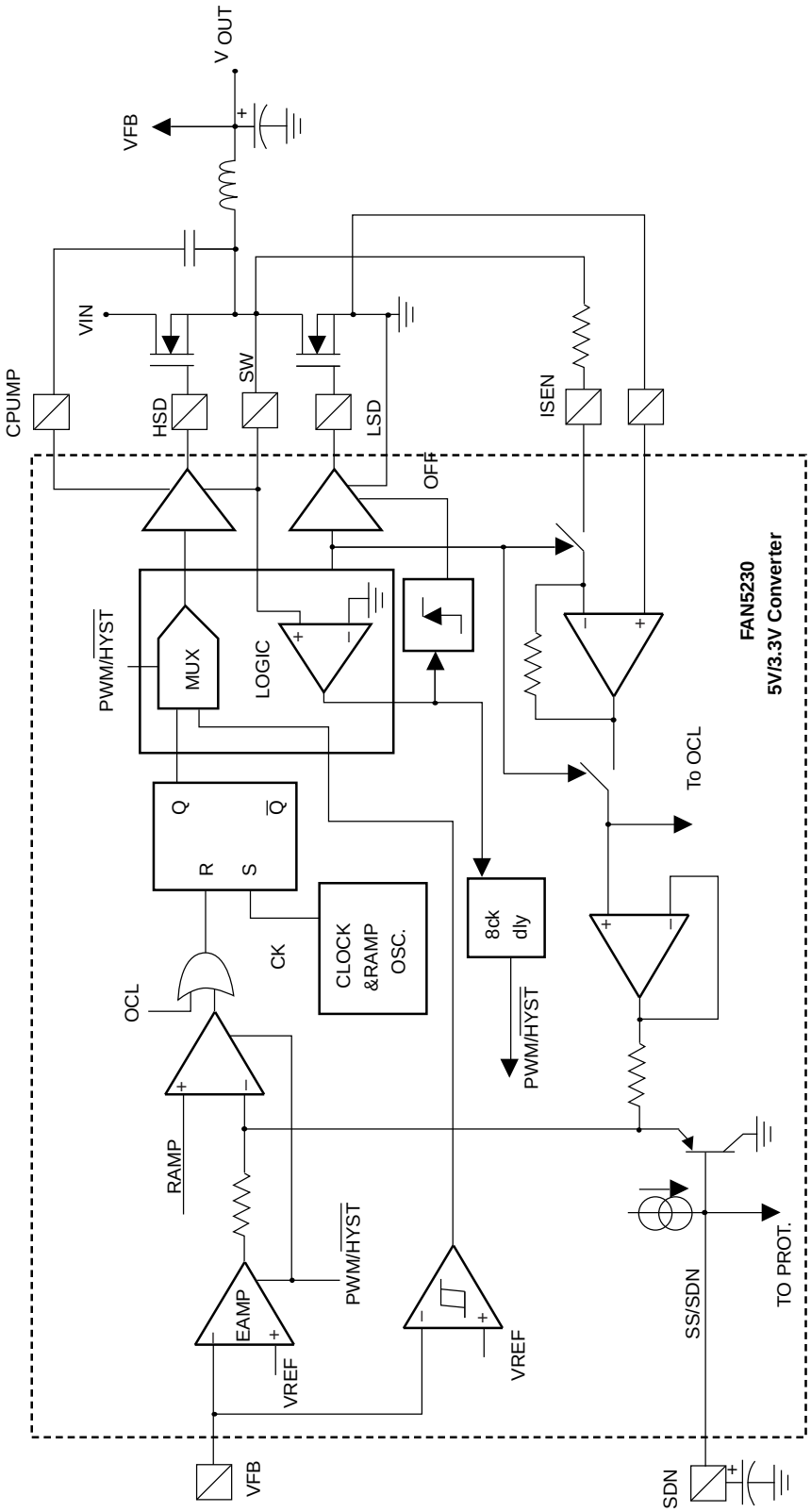

Figure 1. FAN5230 5V/3.3V Internal Block Diagram of PWM/PFM Loops.

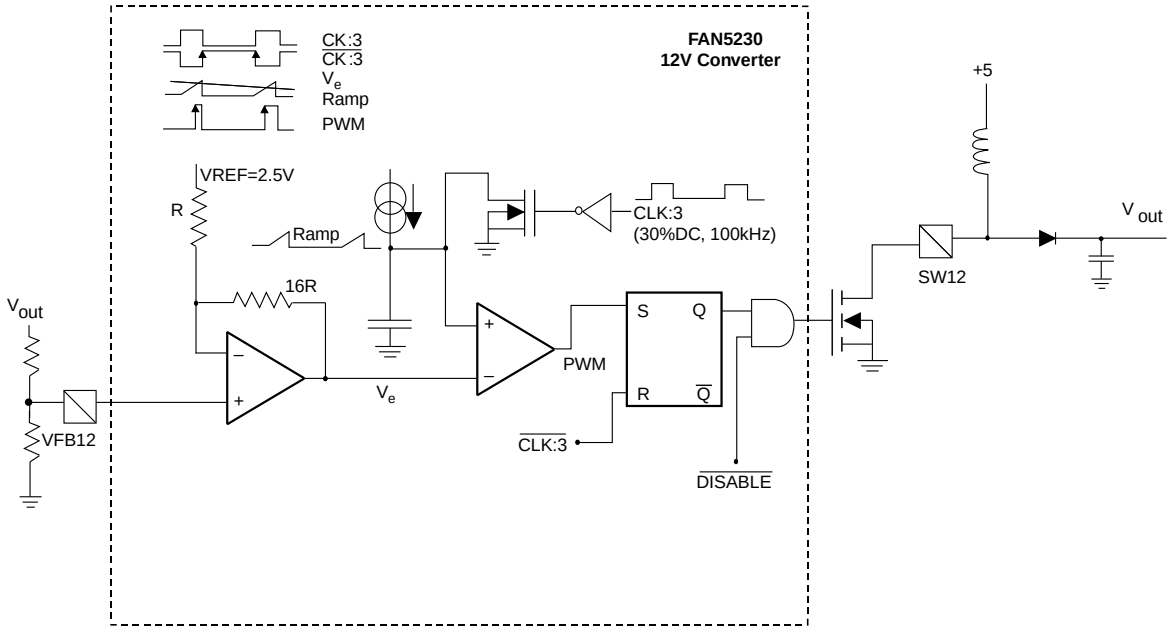

Figure 2. FAN5230 12V Internal Block Diagram

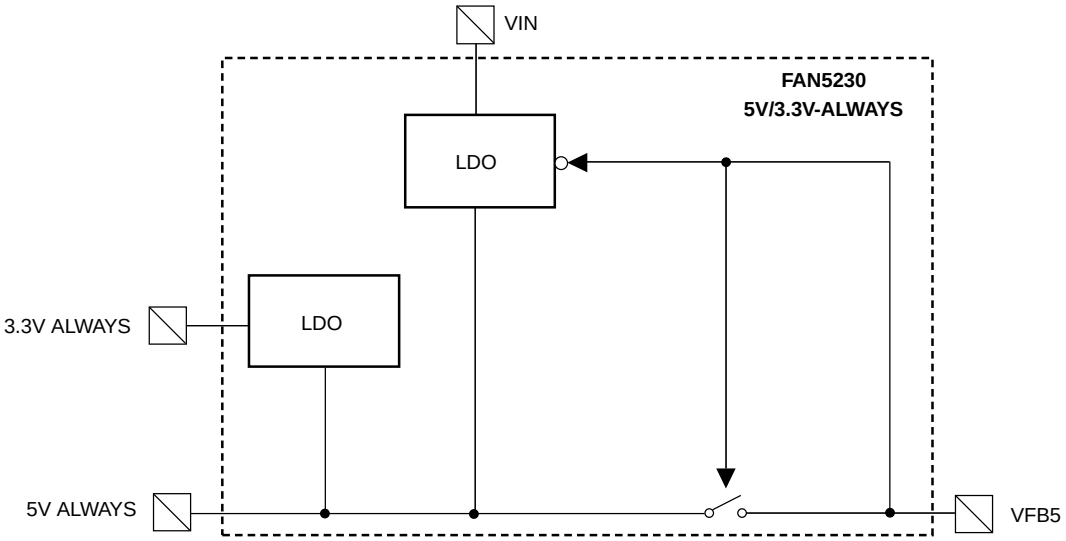

Figure 3. FAN5230 5V/3.3V—ALWAYS Internal Block Diagram

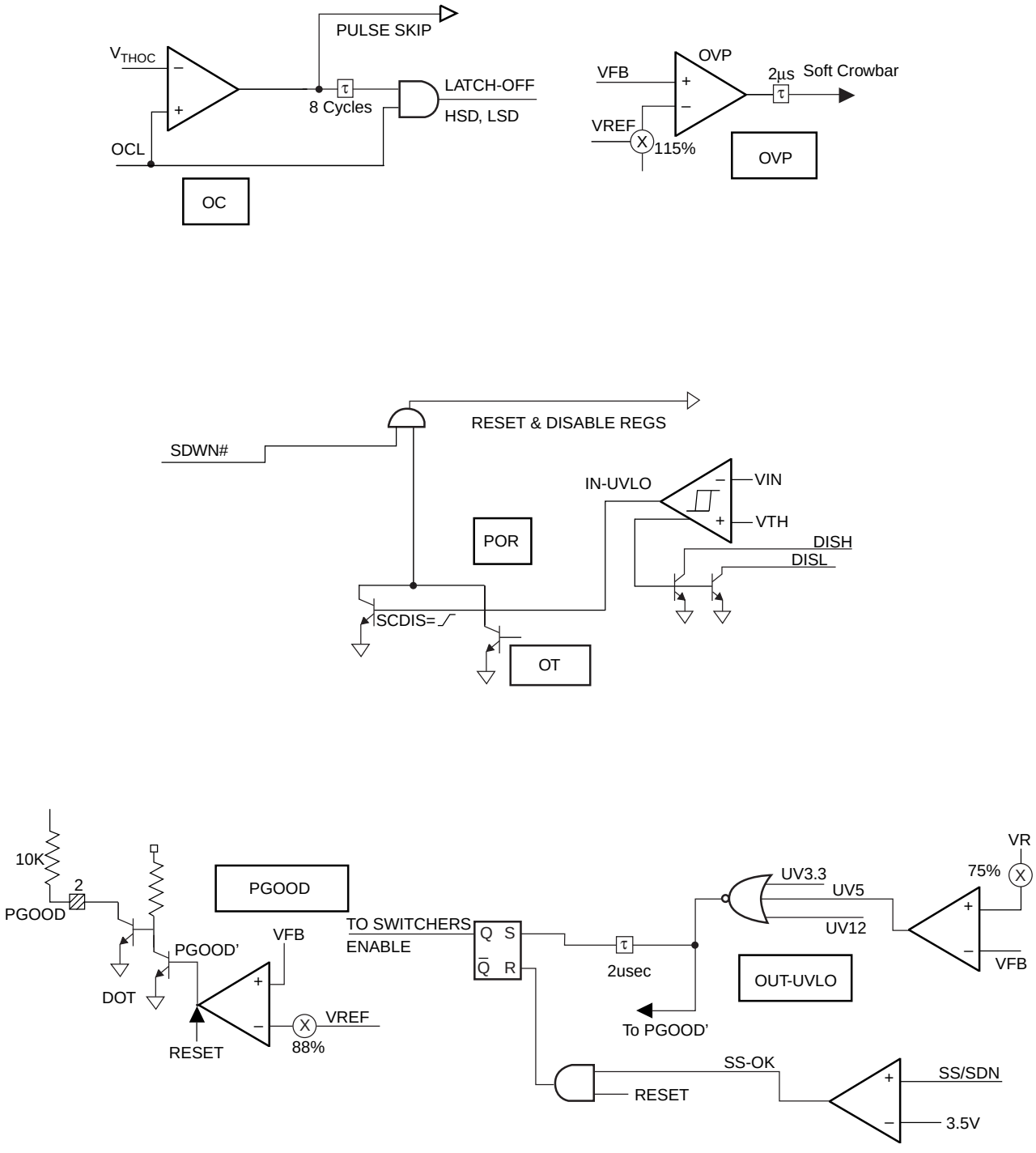

Figure 4. FAN5230 POR and Protections

Advanced Information

Functional Description

The FAN5230 is a high efficiency and high precision DC/DC controller for notebook converters and other portable applications. It provides all of the voltages necessary for system electronics: 5V, 3.3V, 12V, and both 3.3V-ALWAYS and 5V-ALWAYS. Utilization of both input and output voltage feedback in a current-mode control allows for fast loop response over a wide range of input and output variations. Current sense based on MOSFET $R_{DS,on}$ gives maximum efficiency, while also permitting optional use of a sense resistor for high accuracy.

3.3V and 5V Architecture

The 3.3V and 5V outputs of the FAN5230 are generated from the unregulated input voltage using synchronous buck converters. Both high-side and low-side MOSFETs are N-channel.

The 3.3V and 5V have pins for current sensing and setting of output overcurrent using MOSFET $R_{DS,on}$; a pin for voltage-sense feedback; a pin that shuts down the converter; and a pin for generating the boost voltage to drive the high-side MOSFET.

The following discussion of the FAN5230 design will be done with reference to Figures 1 through 4, showing the internal block diagram of the IC.

3.3V and 5V Current Sensing

Peak current sensing is done on the low side driver because of the very low duty cycle on the high-side MOSFET. The current is sampled 50 nsec to 250 nsec after turn on, and the value is held for current feedback and over-current limit.

3.3V and 5V PWM Loop Compensation

The 3.3V and 5V control loops of the FAN5230 are current-mode with slope compensation. They each have an independent voltage feedback pin. In addition, as shown in Figure 1, they use voltage feed-forward to guarantee loop rejection of input voltage variation: the ramp amplitude is varied as a function of the input voltage. Compensation of the control loops is done entirely internally using current-mode compensation. This scheme allows the bandwidth and phase margin to be almost independent of output capacitance and the capacitors' ESR.

3.3V and 5V PWM Current Limit

The 3.3V and 5V converters each sense the voltage across their own low-side MOSFET to determine when to enter current limit. If output current in excess of the current limit threshold is measured, the converter enters pulse skip mode with Iout equal to the set over-current (OC) limit. If this situation persists through 8 clock cycles, the regulator is latched off (HSD and LSD off). This is the likely scenario in case of a "soft" short. If the short is "hard" it will trigger the under-voltage protection without waiting for any clock cycles. This will latch the regulator off (HSD and LSD off) after a 2µsec delay. During soft start current limit (pulse skip mode, unlatched) is enabled while under voltage protection is disabled.

Selection of a current-limit set resistor must include the tolerance of the current-limit trip point, the MOSFET resistance and temperature coefficient, and the ripple current, in addition to the maximum output current.

Example: Maximum DC output current on the 5V is 5A, the MOSFET $R_{DS,on}$ is 17mΩ, and the inductor is 5µH at a current of 5A. Because of the low $R_{DS,on}$, the low-side MOSFET will have a maximum temperature (ambient + self-heating) of only 75°C, at which its $R_{DS,on}$ increases to 20mΩ.

Peak current is DC output current plus peak ripple current:

$$I_{pk} \approx I_{dc} + \frac{TV_0}{2L} = 5A + \frac{4\mu sec \bullet 5V}{2 \bullet 5\mu H} = 7A$$

where T is the maximum period (minimum frequency), V_O is the converter's output voltage, and L is the inductance. This current generates a voltage on the low-side MOSFET of 7A * 20mΩ = 140mV. The current limit threshold is typically 150mV (worst-case 135mV) with R2 = 1KΩ, and so this value is suitable. R2 could be increased a further 10% if additional noise margin is deemed necessary.

Precision Current Limit

Precision current limiting can be achieved by placing a discrete sense resistor between the source of the low-side MOSFET and ground, as shown in Figure 5.

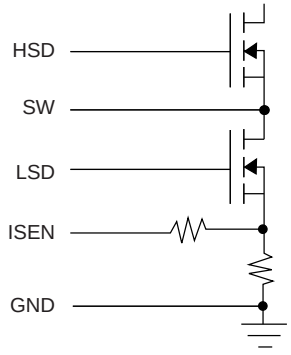

Figure 5. Using a Precision Current Sense Resistor

In this case, current limit accuracy is set by the tolerance of the IC, ±10%.

Shutdown ($\overline{SDWN}$)

The $\overline{SDWN}$ pin turns off all 5 converters (+5V, +3.3V, +12V, and 5V/3.3V-ALWAYS), resetrs all internal Flip-flops, and puts the FAN5230 into a low-power mode (Shut-down mode).

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This mode of operation implies the use of a push button switch between $\overline{SDWN}$ and Vin. Pushing the button powers the 3.3V-ALWAYS and 5V-ALWAYS for the duration of the contact, which will be long enough for the uC to power up and in turn latch the $\overline{SDWN}$ pin high.

Once the $\overline{SDWN}$ is high then the ALWAYS voltages are high and the Main voltages are enabled to go high if the respective $\overline{SDN3.3}$ and $\overline{SDN5}$ go high.

3.3V and 5V Standby, Softstart and Sequencing

The 3.3V (5V) main converter is turned ON if $\overline{SDWN}$ and $\overline{SDN3.3}$ (respectively $\overline{SDN5}$) are both high (open) and is turned OFF if either $\overline{SDWN}$ or $\overline{SDN3.3}$ (respectively $\overline{SDN5}$) is low (shorted to GND)

Softstart of the 3.3V and 5V converters is accomplished by means of an external capacitor between pins $\overline{SDN3.3}$ (respectively $\overline{SDN5}$) and ground.

Stand-by mode is defined as the condition in which the main voltages are OFF and the ALWAYS voltages are ON ($\overline{SDWN}$=1 and $\overline{SDN3.3}$=$\overline{SDN5}$=0).

If it is desired that 5V-ALWAYS and 3.3V-ALWAYS are always ON then the $\overline{SDWN}$ pin must be connected to Vin permanently. This way the two ALWAYS regulators come up as soon as there is power while the state of the Main regulators can be controlled via the $\overline{SDN5}$ and $\overline{SDN3.3}$ pins.

Table 1. Power Control

$\overline{SDN5}$	$\overline{SDN3.3}$	$\overline{SDWN}$	3V&5V ALWAYS	5V MAIN	3.3V MAIN
X	X	0	0	0	0
0	0	1	1	0	0
1	0	1	1	1	0
0	1	1	1	0	1
1	1	1	1	1	1

Input Power for Vclock = 2.5V @ 150mA

This input will normally come from the 3.3V Main. If for any reason this power is required to come from an "ALWAYS" voltage then such power cannot be sourced from the 3.3V-ALWAYS which is limited to 50mA max.

One of many possible solutions is to force the 5VMain to became also "ALWAYS" by forcing the pin $\overline{SDN5}$ high all the time. Now the 2.5V can be obtained from 5V Main with a linear regulator such as the Fairchild RC1117-2.5 (5 to 2.5V conversion).

Another possibility is to buffer the 5V-ALWAYS with a discrete NPN and feed the RC1117-2.5 from the emitter of this NPN having the collector to Vin.

3.3V and 5V Light Load Mode

Because the 3.3V and 5V converters are synchronous bucks, they can operate in two quadrants, which means that the ripple current is a constant independent of the load current. At light loads, this ripple current translates into poor efficiency, since it causes circulating current losses in the MOSFETs. To optimize the efficiency at light loads, then, the FAN5230 switches from normal operation to a special light load mode—after an 8 clock period delay to prevent false triggering—when the voltage across the on-state low-side MOSFET goes positive. Conversely, when this voltage becomes negative the FAN5230 switches back to PWM operation. The current threshold for the switch to and from light load is therefore:

$$Ith = Iripple\ peak$$

In light load mode, the FAN5230 switches from PWM (pulse width modulation) to PFM (pulse frequency modulation), which reduces the gate drive current.

As the load current becomes very light, the FAN5230 begins pulse-skipping, but remains clocked. See the next section for low side drive management.

Low Side Driver Forcing in Light Load

During light load operation the Low Side Driver (LSD) is traditionally turned permanently OFF to avoid current inversion in the inductor and associated efficiency losses. However, the low side driver also needs to be turned ON in order to a) measure current (current is sensed on the low side driver) and b) assure proper operation of the charge pump, especially under low current and low input voltage conditions. In order to accomplish all of the above, after the circuit enters light load mode operation, the LSD is kept "ON" to re-circulate positive and decaying currents (corresponding to negative drops across low side driver R_{dson}) and turned off as soon as current crosses zero (corresponding to drop across R_{dson} becoming positive). This way the low side driver is utilized in "partial duty" or as an "active zero drop diode" (compared to classic light load operation in which the LSD is turned permanently OFF), allowing more functionality without loss in efficiency.

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3.3V and 5V PWM Overvoltage Protection (Soft Crowbar)

When the output voltage of 3.3V (or the 5V) converter exceeds approximately 115% of nominal, that one converter enters into over-voltage (OV) protection, with the goal of protecting the load from damage. During operation, severe load dump or a short of an upper MOSFET can cause the output voltage to increase significantly over normal operation range. When the output exceeds the over-voltage threshold of 115% of the DAC voltage, the over-voltage comparator forces the lower gate driver high and attempts to turn the upper MOSFET off. This will pull down the output voltage, and eventually may blow the battery fuse if the upper MOSFET is shorted. As soon as the output voltage drops below the threshold, the OVP comparator is disengaged.

Such an OVP scheme provides a soft crowbar function (bang-bang control followed by blowing of the fuse) which helps to tackle severe load transients and does not invert output voltage when activated—a common problem for OVP schemes with a latch. The prevention of the output inversion removes the need to use a Schottky diode across the load.

3.3V and 5V PWM Undervoltage Protection

When the output voltage of either 3.3V or 5V falls below 75% of nominal value, all PWM converters, after a 2µsec delay, go into under-voltage (UV) protection. In under-voltage protection, all MOSFETs are turned off. Once under-voltage protection is triggered, it remains on until power is recycled.

12V Architecture

The 12V converter is a traditional non-isolated fly-back (also known as a “boost” converter). The converter’s input voltage is the +5V converter output, so that +12V can only be present if +5V is. Also, in the usual way, if the external MOSFET is off, the output of the converter is +5V, not zero. This in turn will provide non-zero output for the 12V regulator. For complete turn-off of the 12V regulator an external P channel MOSFET or an LDO regulator with on/off control may be used. If an LDO is used for 12V then the boost converter can be set to a higher voltage such as 13.2V via an external resistor divider.

12V Loop Compensation

The 12V converter should be run in discontinuous conduction mode. In this mode, the converter will be stable if a capacitor with a suitable ESR value is selected. A 68µF tantalum with 500mA ripple current rating and 95mΩ ESR is recommended.

12V Protection

The 12V converter is protected against overvoltage. If the 12V feedback is more than 10–15% above the nominal, a comparator forces the MOSFET off until the voltage recovers below the comparator threshold.

The 12V converter is also protected against overcurrent. If a short circuit pulls the output below 9V, all converters, after a 2µsec delay, go into UV protection. In UV protection, all MOSFETs are turned off. Once UV protection is triggered, it remains on until power is recycled.

12V Softstart and Sequencing

The 12V output is started at the same time as the 5V output. The softstart of the 5V output automatically generates a softstart of the 12V output. The duty cycle of the 12V PWM is limited to prevent excessive current draw.

The 12V supply must build up a voltage higher than the UVLO limit (9V) by the time the 5V is above its UVLO (3.75V) in order to avoid triggering of UV protection during soft start.

5V/3.3V-ALWAYS Architecture

The 5V-ALWAYS supply is generated either from the on-chip linear regulator off the input supply voltage, or through an internal switch from the 5V switching supply.

When the 5V switching supply is off, or if its output voltage is not within tolerance, the 5V-ALWAYS switch is open, and the linear regulator is on. When the 5V switching supply is running and has an output voltage within specification, the linear regulator is off, and the switch is on. The switch has sufficiently low resistance that at maximum current draw on the 5V-ALWAYS supply, the output voltage is regulated within specifications.

The 3.3V-ALWAYS is generated from a linear regulator attached internally to the 5V-ALWAYS.

The purpose of these two supplies -whose combined current must never exceed 50mA- is to provide power to the system micro-controller (8051 class) as well as a few other ICs needing a stand-by power. The micro-controller as well as the other ICs discussed here are migrating from 5V to 3.3V power at different times and we expect that some “legacy” devices will continue to need 5V indefinitely.

5V/3.3V-ALWAYS Protection

The two internal linear regulators are current limit and under-voltage protected. Once protection is triggered **all** outputs go off until power is recycled.

Power Good

Power good is asserted when both PWM buck converters are above specified threshold. No other outputs are monitored by Power good. When PGOOD goes low it will stay low for at least 10µsec (Tw). See Figure 6.

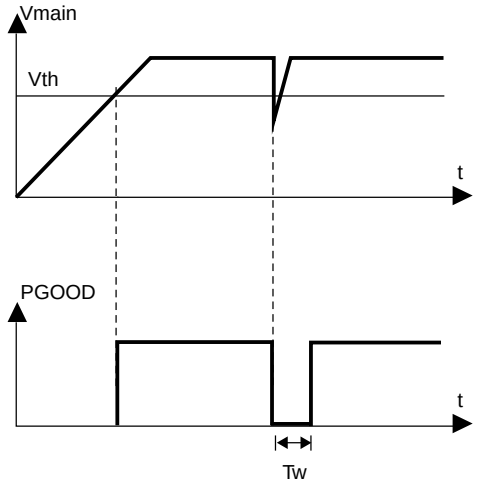

Figure 6. PGOOD Timing Diagram

Error Amplifier Output Voltage Clamp

During transient this voltage is allowed full swing. After two clock cycles, if the amplifier is still out of range the voltage and consequently the duty cycle (DC) is clamped. The DC clamp automatically limits the build up of over-currents during abnormal conditions including short circuits:

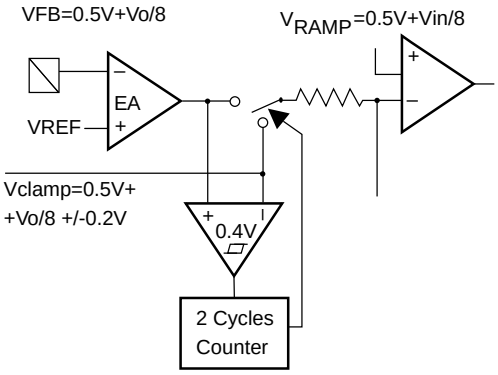

Figure 7. Duty-Cycle Clamp

Thermal Shutdown

If the die temperature of the FAN5230 exceeds safe limits, the IC shuts itself off . When over-temperature (OT) ends then the IC comes back to normal operation in soft start mode. OT has 25°C hysteresis.

Input UVLO

If the input voltage falls below the UVLO threshold, the FAN5230 turns itself off and stays off as long as input voltage is below threshold. Input UVLO has 500mV hysteresis.

Table 2. IC Protection

	HSD Buck	LSD Buck	LDO	LSD Boost
OC/UV (Bucks)	OFF-LATCH	OFF-LATCH	ON	OFF-LATCH
OC/UV (LDO)	OFF-LATCH	OFF-LATCH	OFF-LATCH	OFF-LATCH
OV (Buck)[1]	OFF	SOFT CROWBAR	ON	ON
OV (Boost)	ON	ON	ON	OFF
$\overline{\text{SDWN}}$=0	OFF	OFF	OFF	OFF
OT	OFF	OFF	OFF	OFF
UV (Boost)	OFF-LATCH	OFF-LATCH	ON	OFF-LATCH
OC (Boost)	ON	ON	ON	33% DC

Note:

1. Only the converter in Over-Voltage goes into SOFT CROWBAR mode.

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Generic Mobile System Block Diagram

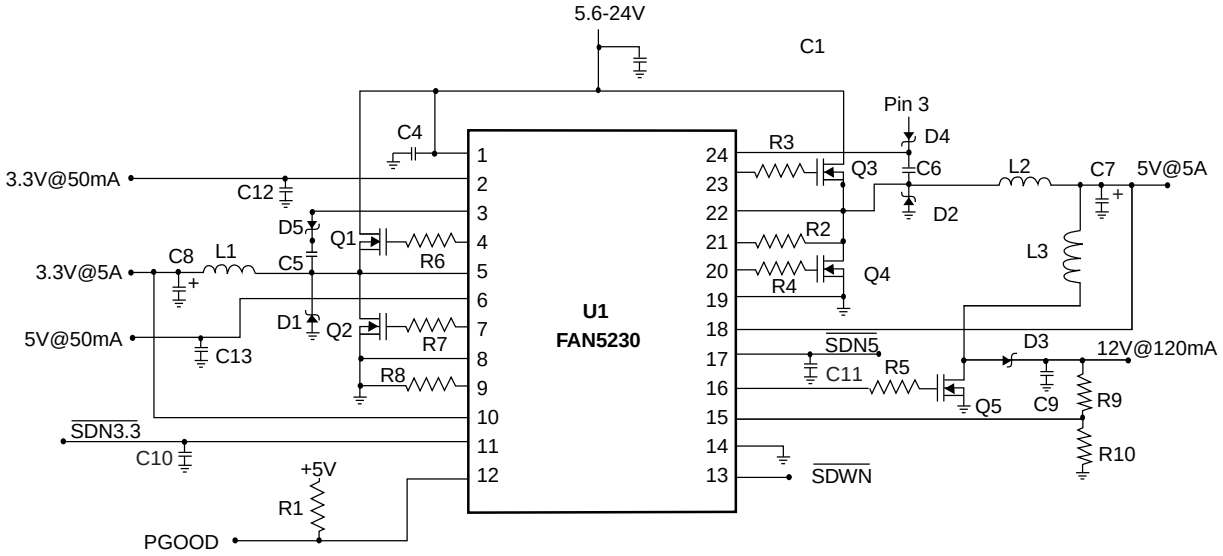


Figure 8. System Block Diagram

Notebook Application Circuit

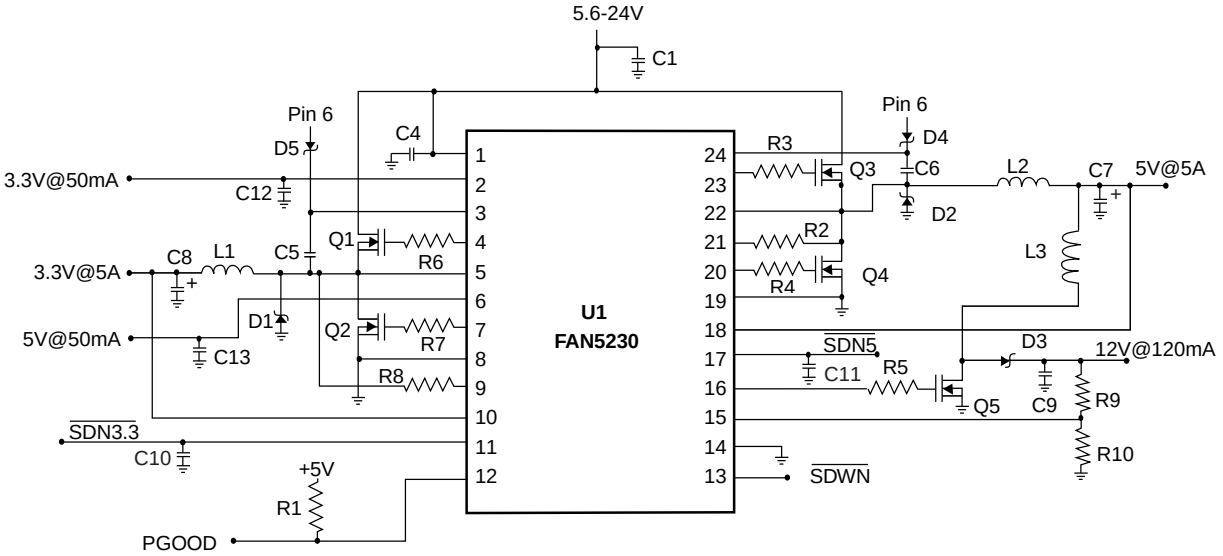


Figure 9. FAN5230 Notebook Application Circuit

Table 3. FAN5230 Application Bill of Materials

Reference	Manufacturer, Part #	Quantity	Description	Comments
C1	SANYO 25SP33M	1	33µF, 25V	OSCON, I_{rms} = 3A, 19V adapter.
C4-6, C10-11	Any	5	100nF, 50V	Ceramic
C7-8, C12-13	KEMET T510X337(1)010AS	2	330µF, 10V	Tantalum, ESR=35mΩ
C9	AVX TPSV68*025R0095	1	68µF, 25V	Tantalum, ESR=95mΩ I_{rms} = 0.5A
R1	Any	1	10KΩ, 1%	
R2, R8	Any	2	1KΩ, 1%	
R3-7	Any	4	4.7Ω, 1%	
R9	Any	1	380KΩ	1%
R10	Any	1		1%
D1-3	Fairchild MBRS340	3	3A, 40V Schottky	
D4-5	Fairchild MBR0520L	2	500mA, 20V Schottky	
L1-2	Any	2	4.7µH, 5A	R < 25mΩ
L3	Any	1	5.6µH, 2A	
Q1-4	Fairchild FDS6690A	4	30V N-channel MOSFET	R_{DS} = 17mΩ
Q5	Fairchild NDC631N	1	20V N-channel MOSFET	R_{DS} = 60mΩ
U1	Fairchild FAN5230	1	SER Controller	

MOSFET Selection

The notebook application circuit shown in Figure 9 is designed to run with an input voltage operating range of 5.6-24V. This wide input range helps determine the selection of the MOSFETs for the 3.3V and 5V converters, since the high-side MOSFET is on (V_{out} / V_{in}) of the time, and the low-side MOSFET 1 – (V_{out} / V_{in}) of the time. The maxima and minima are tabulated in Table 4 and Table 5:

Table 4. High-Side MOSFET Duty Cycles

V_{out}	V_{in}	
	5.6V	24V
3.3V	.59	.14
5V	.89	.21

Table 5. Low-Side MOSFET Duty Cycles

V_{out}	V_{in}	
	5.6V	24V
3.3V	.41	.86
5V	.11	.79

All four MOSFETs have maximum duty cycles greater than 50%. Thus, it is necessary to size all four approximately the same.

3.3V and 5V Schottky Selection

Selection of a schottky is determined by the maximum current at which the converters operate in PFM mode. In the application shown in Figure 8, since the transition can occur at a current as high as 28mV * (17.5KΩ/10KΩ)/35mΩ = 1.4A, the diode (with 24V input) will be conducting 86% of the period (from Table 5). It thus has an average current of 1.4A * .86 = 1.2A, which requires a schottky current rating >1A.

3.3V and 5V Inductor Selection

See Table 3.

3.3V and 5V Output Cap Selection

See Table 3.

12V Component Selection

Selection of the components for the 12V flyback converter must be done carefully to ensure proper operation. Select the inductor to have a maximum inductance of

$$L \leq \frac{4.1 \bullet 10^{-6} \bullet \eta}{V_{out} \bullet I_{out}}$$

where is is assumed that all parameters take their worst-case values. η is the efficiency and may be assumed to be 85%.

Having selected the inductance value, the inductor current can now be chosen to be a minimum saturation current of

$$I_{pk} = \frac{4.87 \bullet 10^{-6}}{L}$$

The diode should have a peak current rating of the same value, and an average current rating of

$$I_{avg} = .165 \bullet I_{pk}$$

Finally, the output capacitor must have a ripple current rating of no less than

$$I_{RMS} \geq \frac{4.26}{L(\mu H)}$$

Input Capacitor Selection

Input capacitor selection is determined by ripple current rating of the caps. This in turn is determined by the output current of the two converters (3.3V and 5V). Select capacitors having a ripple current rating of

$$I_{RMS} \geq \frac{1}{2}\sqrt{\frac{(33I_{3.3}^2 + 50I_5^2)^2}{1089I_{3.3}^2 + 2500I_5^2}}$$

where $I_{3.3}$ is the average current being drawn by the 3.3V output and I_5 is the average current being drawn by the 5V output. Remember to include power being used on the +12V converter. Be aware that capacitor ripple current ratings are temperature dependent: lower average temperature of the converter produces better ratings, requiring fewer caps.

Soft Start Capacitor selection

The recommended value of the soft start capacitor Css is C10 and C11=100nF. This will result in roughly 20msec turn on time. The general formula is:

Css=(Iss*Tss)/[(Vout/8)+0.5V]

where Iss is the soft start current (5µA), Tss is the soft start delay (i.e. 20msec) and Vout is the output voltage (3.3V or 5V).

Advanced Information

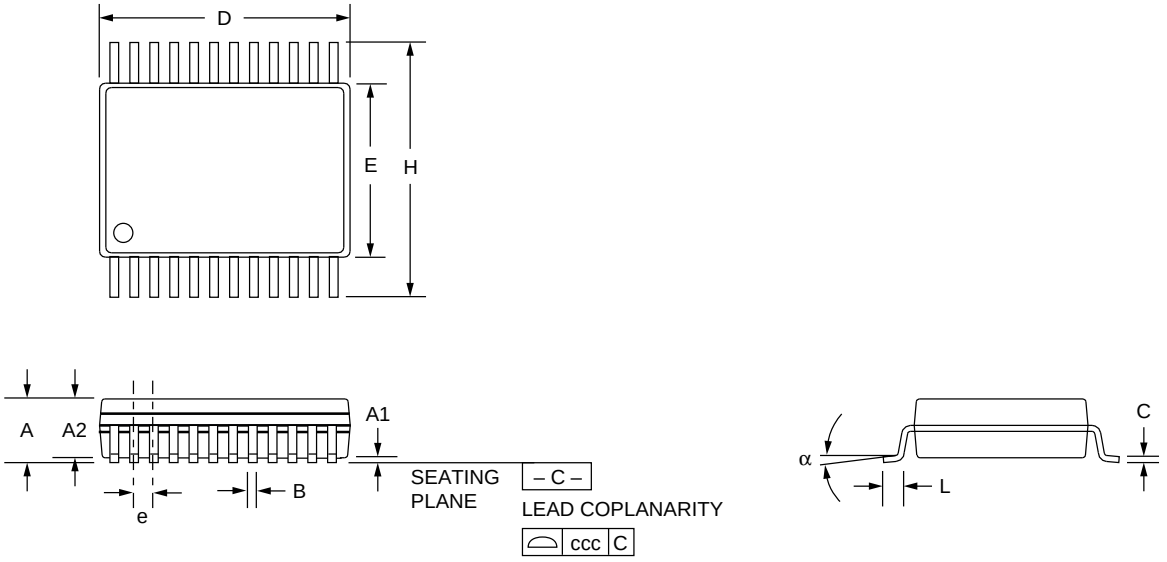
Mechanical Dimensions

QSOP 24-Lead

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	0.0532	0.0668	1.35	1.75	
A1	0.0040	0.0098	0.1	0.25	
A2	0.054	0.062	1.37	1.57	
b	0.008	0.012	0.20	0.30	5
c	0.0075	0.0098	0.19	0.25	5
D	0.337	0.344	8.55	8.74	2, 4
E	0.150	0.157	3.81	3.99	2
e	0.025 BSC		0.635 BSC		
H	0.228	0.244	5.79	6.20	
L	0.016	0.050	0.40	1.27	3
N	24		24		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .006 inch (0.15mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "b" and "c" dimensions include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



Advanced Information

Ordering Information

Product Number	Package
FAN5230	24 Lead QSOP

Advanced Information