FAN5231

Precision Dual PWM Controller And Linear Regulator for Notebook CPUs

Features

- Provides 3 Regulated Voltages
  - Microprocessor core
  - Microprocessor I/O
  - Microprocessor Clock Generator
- High Efficiency Over Wide Load Range
- Not Dissipative Current-Sense Scheme
- Uses MOSFET's $R_{DS(ON)}$
  - Optional Current-Sense Resistor for Precision Overcurrent
  - Adaptive Dead Time Drivers for N-Channel MOSFETs
  - Operates from +5V, +3.3V and Battery (4.5-24V) Inputs
- Precision Core Voltage Control: ±1% Over Temperature
  - Remote "Kelvin" Sensing
  - On-Chip "Droop" for Optimum Transient Response (Voltage positioning)
- TTL-Compatible 5-Bit Digital Output Voltage Selection
  - Wide Range -0.925VDC to 1.3VDC in 25mV Steps, and from 1.3VDC to 2.0VDC in 50mV Steps
  - Programmable "On-the-Fly" with Less than 100µs Settling Time
- Excellent Dynamic Response
  - Average Current Mode with Voltage Feed-Forward
  - Forced-On Feedback for Ultra Fast Transients Handling
  - Dynamic Duty Cycle Clamp to Minimize Inductor Current Build-Up
- Power-Good Output Voltage Monitor
- Microprocessor Core and I/O Circuitry are Protected Against Shorted Upper MOSFETs
- Over-Voltage, Under-Voltage and Over-Current Fault Monitors
- 300kHz Fixed Switching Frequency
- Thermal Shut-Down

Applications

- Mobile "Dual-Mode" CPUs for Notebook PCs
- Low-Voltage Digitally Controlled Converters for Distributed Power Systems

Advanced Specification

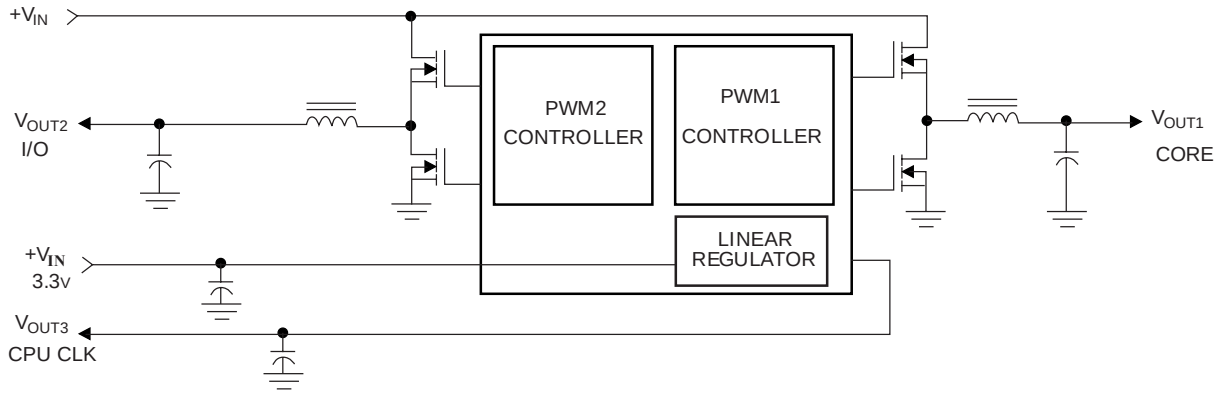


Figure 1. Simplified Power System Diagram

Advanced Specification

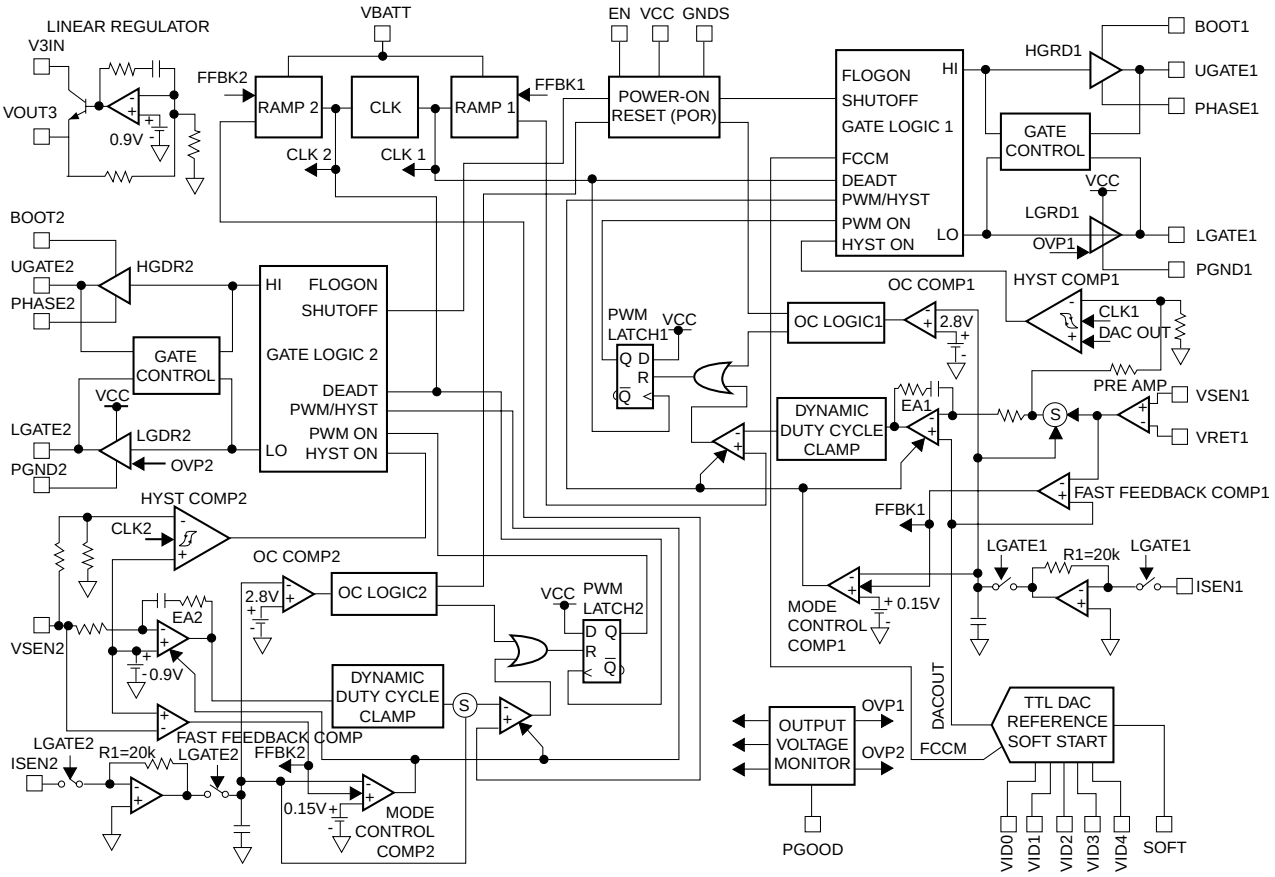
Description

The FAN5231 provides the power control and protection for three output voltages required in high-performance notebook PC applications. The IC integrates two PWM controllers and a linear regulator as well as monitoring and protection circuitry into a single 28 lead QSOP (narrow body SSOP) package. The two PWM controllers regulate the microprocessor core and I/O voltages with synchronous-rectified buck converters, while the linear regulator supplies the 2.5V necessary for the clock driver.

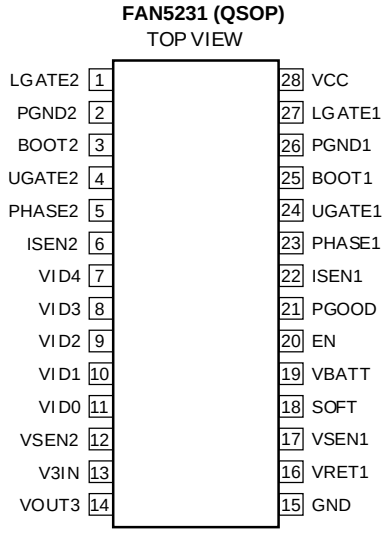
The FAN5231 includes an Intel-compatible, 5-input digital-to-analog converter (DAC) that adjusts the core PWM output voltage from $0.925V_{DC}$ to $2.0V_{DC}$. The DAC setting may be changed during operation to accommodate "Dual-Mode" microprocessors. Measures are taken to provide such a transition in less than 100µs. A precision reference, remote sensing, and a proprietary architecture with integrated "droop" provide excellent static and dynamic core voltage regulation. The second PWM controller has a fixed 1.5V output voltage and powers the microprocessor's I/O circuitry. The linear regulator uses an internal pass device to provide 2.5V for the microprocessor's clock generator.

The FAN5231 monitors all the output voltages. A single Power-Good signal is issued when soft start is completed and all outputs are within ±10% of their respective set points. A built-in over-voltage protection for the core and I/O outputs forces the lower MOSFETs on to prevent output voltages from going above 115% of their settings. Under-voltage protection latches the chip off when any of the output drops below 75% of its setting value. The PWM controller's over-current circuitry monitors the output current by sensing the voltage drop across the lower MOSFETs. If precision current-sensing is required, an external current-sense resistor may optionally be used.

Block Diagram



Pin Out



Application Bill of Materials

Reference	Manufacturer Part #	Qty	Description	Requirements/Comments
C1–3		3	56µF, 35V Capacitor	
C4–6, C19–26	Any	10	1µF, 16V Capacitor	
C7–8	Any	2	220nF, 50V Capacitor	
C9		1	330µF, 6.3V Electrolytic	
C11–18		8	680µF, 10V Electrolytic	I_{RMS} = 2A
C27–8		2	10µF, 6.3V Electrolytic	ESR ≤ 44mΩ
C29		1	68µF, 10V Electrolytic	I_{RMS} = 2A
C30	Any	1	100nF, 50V Capacitor	
D1–2	Fairchild BAT54	2	30V, 200mA Schottky Diode	
D3	Fairchild MBRS130L	1	1A, 30V Schottky Diode	
D4	Fairchild MBR735	1	7A, 35V Schottky Diode	
L1	Any	1	10µH, 4A Inductor	DCR ~ 20mΩ
L2	Any	1	2µH, 14A Inductor	DCR ~ 20mΩ
Q1	Fairchild FDS6680A	1	N-Channel MOSFET	$R_{DS(ON)}$ = 13mΩ @ V_{GS} = 4.5V
Q2	Fairchild FDD6670A	1	N-Channel MOSFET	$R_{DS(ON)}$ = 10mΩ @ V_{GS} = 4.5V
Q3	Fairchild FDS9936A	1	N-Channel MOSFET	$R_{DS(ON)}$ = 60mΩ @ V_{GS} = 4.5V
R1–2	Any	2	1KΩ	
U1	Fairchild FAN5231	1	DC/DC Controller	

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Absolute Maximum Ratings

Supply Voltage, V_{CC} ..... +7.0V
Input Voltage, Vbatt ..... +30.0V
V3in ..... +7.0V
PGOOD, RT/FAULT,
and GATE Voltage ..... GND - 0.3V to V_{CC} + 0.3V
Core Output or I/O Voltage ..... GND -0.3V to 7V
ESD Classification ..... Class 2

Recommended Operating Conditions

Supply Voltage, V_{CC} ..... +5.0V ±10%
Input Voltage, Vbat ..... +7.5V to 24.0V
V3in ..... +3.3V ±10%
Ambient Temperature Range ..... 0°C to 70°C
Junction Temperature Range ..... 0°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1) ..... Θ_{JA} (°C/W)
QSOP Package ..... TBD
QSOP Package (with 3 in^2 of copper) ..... TBD
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... 65°C to 150 °C
Maximum Lead Temperature (Soldering 10s)
(QSOP - Lead Tips Only) ..... 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Note:

1. Θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted. Refer to Figures 1, 2 and 3.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
V_{CC} Supply						
Nominal Supply Current	I_{CC}	GATE1, GATE2 Open	-	-	1	mA
Shut-down Supply Current	I_{CCS}		-	-	10	µA
Battery Pin Supply Current	I_{BATT}		-	-	10	µA
Battery Pin Leakage Current at Shut-Down	I_{BATTS}		-	-	1	µA
Power-on Reset						
Rising V_{CC} Threshold			4.4	4.5	4.6	V
Falling V_{CC} Threshold			3.9	4.0	4.1	V
Oscillator						
Free Running Frequency			255	300	345	kHz
Ramp Amplitude, pk-pk		Vbat = 16V	-	2	-	V
Ramp Offset			-	0.5	-	V
Reference, Dac and Soft Start						
VID0-VID4 Input Low Voltage			-	-	0.8	V
VID0-VID4 Input High Voltage			2.0	-	-	V
DAC Voltage Accuracy			-1.0	-	+1.0	%
Soft-Start Current During Start-Up	I_{SS}	Vss = 0V…0.9V	-	25	-	µA
Soft-Start Current During Mode Change	I_{SSM}	Vss = 0.925V…2.0V	-	300	-	µA
Enable						
Enable Voltage Low	V_{ENLOW}	IC Inhibited	-	-	0.8	V
Enable Voltage High	V_{ENHIGH}	IC Enabled Input has internal pull-up current source 2µA typ	-	-	2.0	V

Electrical Specifications (Continued)

Recommended Operating Conditions, Unless Otherwise Noted. Refer to Figures 1, 2 and 3.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
PWM 1 Converter						
Output Voltage	VOUT1	Defined by the current VID code (Table 1)	0.925	-	2.0	V
Static Load Regulation		100mA < I_{VOUT1} < 15.0A	-2.0	-	+2.0	%
Under-Voltage Shut-Down Level	V_{UV1}	Percent of the voltage set by VID code. Disabled for 150µs during dynamic VID code change.	-	-	75	%
Under-Voltage Shut Down Delay	T_{DOC1}		1.5	-	3.5	µs
Over-Voltage	V_{OVP1}	Percent of the voltage set by VID code.	115	-	117	%
Over-Voltage Shut Down Delay	T_{DOV1}		2.0	-	3.5	µs
Over-Current Comparator Threshold	I_{OC1}		TBD	TBD	TBD	µA
Switchover to Hysteretic Operation Threshold	I_{HYST1}		TBD	TBD	TBD	µA
Switchover to PWM Operation Threshold	I_{PWM1}		TBD	TBD	TBD	µA
PWM 2 Converter						
Output Voltage	VOUT2			1.5		V
Load Regulation Under-Voltage Shut-Down Level	 V_{UV2}	100mA < I_{VOUT3} < 2.1A	-2.0 1.11	- -	+2.0 1.14	% V
Under-Voltage Shut Down Delay	T_{DOC2}		1.5	-	3.5	µs
Over-Voltage Shut-Down	V_{OVP2}		1.72	-	1.76	V
Over-Voltage Shut Down Delay	T_{DOV2}		2.0	-	3.5	µs
Over-Current Comparator Threshold	I_{OC2}		TBD	TBD	TBD	µA
Switchover to Hysteretic Operation Threshold	I_{HYST2}		TBD	TBD	TBD	µA
Switchover to PWM Operation Threshold	I_{PWM2}		TBD	TBD	TBD	µA
Linear Regulator						
Output Voltage	VOUT3			2.5		V
Load Regulation		10mA < I_{VOUT3} < 150mA	-2.5	-	2.5	%
Under-Voltage Shut-Down Level	V_{UV3}		1.85	-	1.9	V
Over-Current Shut-Down	I_{oc3}		-	250	-	mA
PWM Controller Error Amplifiers						
DC Gain		By design	-	88	-	dB
Gain-Bandwidth Product	GBWP	By design	-	15	-	MHz
Slew Rate	SR	By design	-	6	-	V/µs
PWM 1 Controller Gate Drivers						
Upper Drive Source Current	I_{1UGON}		-	0.5	-	A
Upper Drive Pull-Up Resistance	R_{1UGPUP}		-	3	5	Ω
Upper Drive Sink Current	I_{1UGOFF}		-	1.0	-	A
Upper Drive Pull-Down Resistance	R_{1UGPDN}		-	3	5	Ω
Lower Gate Source Current	I_{1LGON}		-	1	-	A
Lower Drive Pull-Up Resistance	R_{1LGPUP}		-	3	5	Ω

Advanced Specification

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Electrical Specifications (Continued)

Recommended Operating Conditions, Unless Otherwise Noted. Refer to Figures 1, 2 and 3.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Lower Gate Sink Current	I_{1LGOFF}		-	3	-	A
Lower Drive Pull-Down Resistance	R_{1LGPDN}		-	1	1.7	Ω
PWM 2 Controller Gate Drivers						
Upper Drive Source Current	I_{2UGON}		-	0.5	-	A
Upper Drive Pull-Up Resistance	R_{2UGPUP}		-	6	10	Ω
Upper Drive Sink Current	I_{2UGOFF}		-	0.75	-	A
Upper Drive Pull-Down Resistance	R_{2UGPDN}		-	6	10	Ω
Lower Gate Source Current	I_{2LGON}		-	0.5	-	A
Lower Drive Pull-Up Resistance	R_{2LGPUP}		-	6	10	Ω
Lower Gate Sink Current	I_{2LGOFF}		-	1	-	A
Lower Drive Pull-Down Resistance	R_{2LGPDN}		-	3	5	Ω
Power Good						
V_{OUT1} Upper Threshold		Percent of the voltage defined by the VID code	110	-	112	%
V_{OUT1} Lower Threshold, Falling Edge		Percent of the voltage defined by the VID code	88	-	90	%
V_{OUT1} Lower Threshold, Risisng Edge		Percent of the voltage defined by the VID code	90	-	92	%
V_{OUT2} Upper Threshold			1.65	-	1.68	V
V_{OUT2} Lower Threshold			1.33	-	1.37	V
V_{OUT3} Upper Threshold			2.75	-	2.8	V
V_{OUT3} Lower Threshold			2.22	-	2.28	V
PGOOD Voltage Low	V_{PGOOD}	I_{PGOOD} = -4mA	-	-	0.5	V
PGOOD Leakage Current	I_{PGILKG}	V_{PULLUP} = 5.0V	-	-	10	µA

Functional Pin Description

VID0, VID1, VID2, VID3, VID4 (Pins 11, 10, 9, 8 and 7 respectively)

VID0-VID4 are the input pins to the 5-bit DAC. The states of these five pins program the internal voltage reference (DACOUT). The level of DACOUT sets the core converter output voltage (V_{OUT1}). It also sets the core PGOOD, UVP and OVP thresholds.

BOOT1, BOOT2 (Pins 25 and 3)

Through these pins power is supplied to the upper MOSFET drivers of the core and I/O converters. Connect these pins to their respective junctions of the bootstrap capacitors and the cathodes of the bootstrap diodes. The anodes of the bootstrap diodes are connected to pin 28, V_{CC}.

PHASE1, PHASE2 (Pins 23 and 5)

The PHASE nodes are the junction points of the upper MOSFET sources, output filter inductors, and lower MOSFET drains. Connect the PHASE pins to the respective PWM converter's upper MOSFET source.

ISEN1, ISEN2 (Pins 22 and 6)

These pins are used to monitor the voltage drop across the lower MOSFETs for current feedback, output voltage droop and over-current protection. For precise current detection these inputs could be connected to optional current sense resistors placed in series with sources of the lower MOSFETs. To set the gain of the current sense amplifier, a resistor should be placed in series with each of these inputs. The value of the resistor required can be obtained from the following equation.

$$R_{si} = \frac{34k \bullet Iosc \bullet Rcs}{Vth}$$

where: Iosc—desired overload current trip level; Rcs—either Rdson of the lower MOSFET, or the value of the optional current sense resistor; Vth— threshold of the current protection circuitry.

Vth = TBD for the core output and Vth = TBD for the I/O output.

UGATE1, UGATE2 (Pins 24 and 4)

Connect the UGATE pins to the respective PWM converter's upper MOSFET gate. These pins provide the gate drive for the upper MOSFETs.

LGATE1, LGATE 2 (Pin 27 and 1)

These pins provide the gate drive for the lower MOSFETs. Connect the lower MOSFET gate of each converter to the corresponding pin.

PGND1, PGND2 (Pin 26 and 2)

These are the power ground connection for the core and I/O converters, respectively. Tie each lower MOSFET source to the corresponding pin.

VSEN2 (Pin 12)

This pin is connected to the I/O output and provides voltage feedback to the I/O error amplifier. The PGOOD and OVP comparator circuits use this signal for over-voltage protection.

V3IN (Pin 13)

This pin provides input power for the 2.5V linear regulator.

VOUT3 (Pin 14)

Output of the 2.5V linear regulator. Supplies current up to 150mA. Output current on this pin is internally limited to 250mA.

VSEN1, VRTN1 (Pins 17 and 16)

These pins are connected to the core converter's output voltage to provide remote. The PGOOD and OVP comparator circuits use these signals for over-voltage protection.

SOFT (Pin 18)

Connect a capacitor from this pin to ground. This capacitor (typically 0.1µF), along with an internal 25µA current source, sets the soft-start interval of the converter. When voltage on this pin exceeds 0.9V, the current source is changed to 300µA leading to faster start completion and faster operational mode change.

VBATT (Pin 19)

VBATT provides battery voltage to the oscillator for feed-forward rejection of input voltage variations.

EN (Pin 20)

This pin enables IC operation when left open or pulled-up to V_{CC}. Also, it unlatches the chip when cycled.

PGOOD (Pin 21)

PGOOD is an open collector output used to indicate the status of the PWM converters' output voltages. This pin is pulled low when the core output is not within ±10% of the DACOUT reference voltage, or when any of the other outputs are not within their respective under-voltage and over-voltage thresholds.

The PGOOD output is pulled low for "01111" and '11111' VID code. See Table 1.

GND (Pin 15)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

V_{CC} (Pin 28)

Supplies all the power necessary to operate the chip. The IC starts to operate when the voltage on this pin exceeds 4.5V and shuts down when the voltage on this pin drops below 4.0V.

Operation

The FAN5231 addresses low-voltage, high-current power needs of modern "Dual Mode" processors for notebook and sub-notebook PCs. The IC controls operation of two synchronous buck converters for the core and I/O portions of the processor. The output voltage of the core converter can be adjusted in the range from 0.925V to 2.0 by changing the DAC code settings (see Table 1). The output voltage of the I/O converter is fixed to 1.5V. The internal linear regulator provides fixed 2.5V for the CPU clock generator from the system +3.3V bus. The output voltages of the I/O converter and the linear regulator do not change when the processor changes mode of operation.

Both core and I/O converters have two modes of operation: fixed frequency PWM and variable frequency hysteretic depending on their respective loads. When current consumed by the CPU core drops below 1.5A, the mode control comparator inhibits the core PWM controller and enables the hysteretic comparator. Fairchild's proprietary "droop" output voltage regulation is maintained in both operational modes for the core converter. Output voltage droop is favorable for optimum handling of fast load transients found in modern processors. Switchover from PWM to hysteretic operation at light loads improves the converters' efficiency and prolongs battery life. In hysteretic mode, comparators are synchronized to the main clock which allows seamless transition between the operational modes.

Initialization

The FAN5231 automatically initializes upon receipt of input power assuming EN is high or not connected. The Power-On Reset (POR) function continually monitors the input supply voltage on the V_{CC} pin and initiates soft-start operation after input supply voltage exceed 4.5V. Should this voltage drop lower than 4.0V, POR disables the chip.

Soft-Start

When soft start is initiated by the POR or EN, the voltage on the SOFT pin starts to ramp gradually due to the 25µA current sourced into the external capacitor. This voltage is applied to the gain-controlled voltage follower on the DAC's output, effectively delaying voltage rise on the error amplifiers inputs.

When SOFT reaches 0.9V, the value of the sourcing current is changed to 300µA rapidly charging the soft-start capacitor to the level determined by the DAC and completing the soft start sequence. As long as the DAC voltage is above 0.9V, the internal soft start current source is set to 300µA allowing faster rate-of-change in the core output voltage in the operational range from 0.925V to 2.0V.

This dual slope approach helps to provide slow and safe rise of voltages and currents in the converters during initial start-up and at the same time sets a controlled speed of the core voltage change when the processor commands to do so.

Soft-start circuits for the I/O and clock outputs are slaved to the core output soft-start circuits and they complete their ramp-up when voltage on the SOFT pin reaches 0.9V.

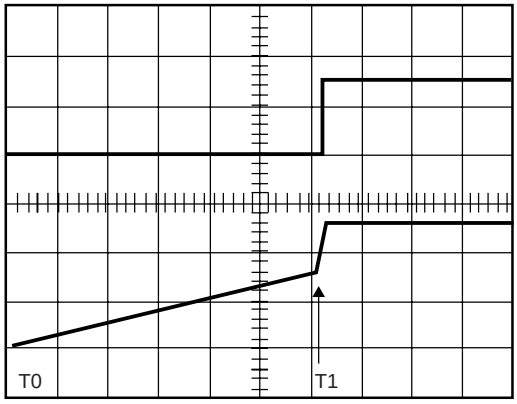


Figure 2.

The value of the soft-start capacitor can be estimated by the following equation:

$$Css = \frac{\Delta Issm}{\Delta Vdac}\Delta t$$

For the typical conditions when ΔVdac=0.25V, Δt=100µs

$$Css = \frac{300\mu A}{0.25V}100\mu s \approx 0.1\mu F$$

With this value of the soft-start capacitor, turn-on time will be equal to

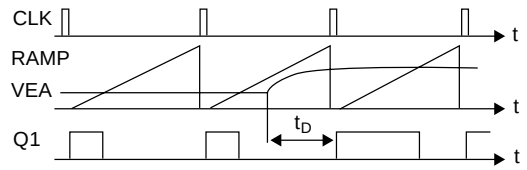
$$Tss = \frac{0.1\mu F \bullet 0.9V}{25\mu A} = 3.6ms$$

PWM Operation

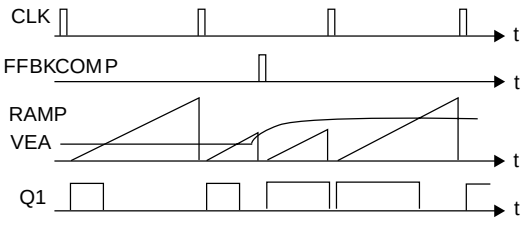
When the CPU core consumes current higher than about 1.5A, PWM1 converter operates in a fixed frequency PWM mode. The output voltage is compared with a reference voltage set by the DAC. The derived error signal is amplified by an internally compensated error amplifier and applied to the inverting input of the PWM comparator. To provide output voltage droop for enhanced dynamic load regulation, a signal proportional to the output current is added to the voltage feedback signal. This feedback scheme in conjunction with a PWM ramp proportional to the input voltage allows for fast and stable loop response over a wide range of input voltage and output current variation. For the sake of efficiency and maximum simplicity, the current sense signal is derived from the voltage drop across the lower MOSFET during it's conduction time.

In mobile computer applications the conduction time of the upper MOSFET is normally very short. Thus the probability that the response to a transient will be delayed to the next switching cycle is very high. To provide fast response to severe load steps, ultra fast feedback is incorporated into the PWM scheme. An additional comparator constantly monitors output. If output voltage excursion exceeds the threshold, comparator forces the ramp generator to start a new additional pulse within the same clock cycle. By these, response time to the transient about 200ns is achieved.

When I/O part of the processor consumes current higher than about 0.5A, PWM2 converter operates in a fixed frequency PWM mode.



A. Regular Feedback



B. With Fast Feedback

Figure 3.

This converter incorporates a peak current mode control scheme by introducing the signal derived from the voltage drop across the lower MOSFET to the PWM comparator.

Advanced Specification

Both PWM controllers have build-in dynamic duty cycle clamp in the path from error amplifier to PWM comparator. During severe load step-up, output signal of an error amplifier can go to its upper limit pushing a duty cycle to almost 100% for significant amount of time. This could cause severe rise of an inductor current and lead to long recovery from a transient or even to a converter failure especially at higher input voltages. To prevent this, output of the error amplifier is clamped to a fixed value after two clock cycles if severe output voltage excursion is detected. Sensitivity of the circuit is set not to affect the PWM scheme during the transients normally expected from the load.

Hysteretic Operation

When the output currents of the converters drop below their threshold settings, the mode control comparators change a function of the respective converter and the way the signals in the chip are processed by entering the hysteretic mode. The comparators and the error amplifiers provided control in the PWM mode are inhibited and hysteretic comparators are now activated. Two clock cycles delay before entering the hysteretic mode prevents undesirable sporadic mode change at near threshold loads.

The voltage on the negative input of the core hysteretic comparator is the sum of the feedback voltage and a voltage proportional to the output current. Voltage on the reference input of the hysteretic comparator is the DAC output voltage with a small addition of the clock frequency pulses. Such a scheme allows to benefit from the advantages of a droop output voltage regulation, i.e. enhanced output voltage excursion at transients even in the hysteretic mode and more importantly during transitions from the hysteretic to the PWM mode and vice versa. Synchronization of the upper MOSFET turn-on pulses with the main clock also contributes positively to the seamless transition between the operation modes.

Operation During Processor Mode Changes

The PWM1 controller is specially designed to provide “on the fly” automatic core voltage changes required by some advanced processors for mobile applications. Dual core voltage and operation frequency scaling allows for significant power savings without sacrificing system performance in battery operation mode.

As processor mode changes can happen when chip is in PWM or hysteretic mode, measures were taken to provide equally fast response to these changes. As soon as a DAC code change is received, the chip is switched into the forced PWM mode for about 150µs regardless of the load level. Operating the controller in the synhronous PWM mode allows faster output voltage transitions especially when a downward output voltage change is commanded.

Gate Control Logic

The gate control logic translates generated PWM signals into the MOSFETs gate drive signals providing necessary amplification, level shift and shoot-trough protection. Also, it bears some functions that help to optimize the IC performance over a wide range of the operational conditions. As MOSFET switching time can vary dramatically from type to type and with input voltage, gate control logic provides adaptive dead time by monitoring gate voltages of both upper and lower MOSFETs.

Fault Protection

All three outputs are monitored and protected against extreme overload, short circuit and under-voltage conditions. Both PWM outputs are monitored and protected from over-voltage conditions. Linear regulator output is only monitored for over-voltage conditions. A sustained overload on any output latches-off all the converters and sets the PGOOD pin low. The chip operation can be restored by cycling V_{CC} voltage or EN pin.

During over-voltage the lower gate driver of the affected converter is forced high turning on the synhronous rectifier for as long time as overvoltage condition persists. Converter restores normal operation when the output voltage returns to the normal value.

Over-Current Protection

Both PWM controllers use the lower MOSFET’s on-resistance, $R_{DS(ON)}$, to monitor the current for protection against shorted outputs. The sensed voltage drop after amplification is compared with an internally set threshold. Several scenarios of the current protection circuit behavior are possible.

If load step is strong enough to pull output voltage lower than the under-voltage threshold, chip shuts down. If the output voltage sag does not reach the under-voltage threshold but the current exceeds the over-current threshold, the pulse skipping circuit is activated. This breaks the output voltage regulation and limits the current supplied to the load.

Because of the nature of used current sensing technique, and to accommodate wide range of the $R_{DS(ON)}$ variation, the value of the threshold should represent overload current about 180% of the nominal value. This could lead to the situation where the converter continuously delivers power about two times the nominal without significant drop in the output voltage. To eliminate this, the time delay circuit (8:1 counter which counts the clock cycles) is activated when the overcurrent condition is detected for the first time. If after the delay the overcurrent condition persists, the converter shuts down. If not-normal operation restores.

In the linear regulator the integrated power device current is actively limited to 250mA which at some point creates an under-voltage condition and sets the fault latch.

Overvoltage Protection

During operation, severe load damp or a short of an upper MOSFET can cause the output voltage to increase significantly over normal operation range. When the output exceeds the over-voltage threshold of 115% of the DAC voltage (1.7V for PWM2), the over-voltage comparator forces the lower gate driver high and turns the lower MOSFET on. This will pull down the output voltage and eventually blow the battery fuse. As soon as output voltage drops below the threshold, OVP comparator is disengaged.

Such OVP scheme provides soft crowbar function which helps to tackle severe load transients and does not invert output voltage when activated, common problem for OVP schemes with a latch.

Overvoltage protection is not provided on the linear regulator.

OUT1 Voltage Program

The output voltage of the PWM1 converter is programmed to discrete levels between $0.925V_{DC}$ and $2.0V_{DC}$. This output is designed to supply the microprocessor core voltage. The voltage identification (VID) pins program an internal voltage reference (DAC) through a TTL-compatible 5-bit digital-to-analog converter. The level of the DAC voltage also sets the PGOOD, UVP and OVP thresholds. Table 1 specifies the DAC voltage for the different combinations of connections on the VID pins. The VID pins can be left open for a logic 1 input, because they are internally pulled up to +3.3V by a 10µA current source.

The '11111' and '0111'VID codes, as shown in Table 1, shut the IC down and set PGOOD low.

Table 1.

Pin Name					Nominal OUT1 Voltage
VID4	VID3	VID2	VID1	VID0	
0	0	0	0	0	2.00
0	0	0	0	1	1.95
0	0	0	1	0	1.90
0	0	0	1	1	1.85
0	0	1	0	0	1.80
0	0	1	0	1	1.75
0	0	1	1	0	1.70
0	0	1	1	1	1.65
0	1	0	0	0	1.60
0	1	0	0	1	1.55
0	1	0	1	0	1.50
0	1	0	1	1	1.45
0	1	1	0	0	1.40
0	1	1	0	1	1.35

Table 1. (Continued)

Pin Name					Nominal OUT1 Voltage
VID4	VID3	VID2	VID1	VID0	
0	1	1	1	0	1.30
0	1	1	1	1	No CPU*
1	0	0	0	0	1.275
1	0	0	0	1	1.250
1	0	0	1	0	1.225
1	0	0	1	1	1.200
1	0	1	0	0	1.175
1	0	1	0	1	1.150
1	0	1	1	0	1.125
1	0	1	1	1	1.100
1	1	0	0	0	1.075
1	1	0	0	1	1.050
1	1	0	1	0	1.025
1	1	0	1	1	1.000
1	1	1	0	0	0.975
1	1	1	0	1	0.950
1	1	1	1	0	0.925
1	1	1	1	1	No CPU*

Note: 0 = connected to GND or V_{SS}, 1 = open or connected to 3.3V through pull-up resistors.

Over Temperature Protection

The chip incorporates an over temperature protection circuit that shuts all the outputs down when the die temperature of 150°C is reached. Normal operation restores at the die-temperatures below 125°C trough the full soft-start cycle.

Application Guidelines

Layout Considerations

Switching type of converters even during normal operation produce short pulses of current which could cause substantial ringing and be a source of EMI pollution if layout constrains are not observed.

There are two sets of critical components in a DC-DC converter. The switching power components evolve processing large amounts of energy at high rate and though, usually appear to be a source of a noise, end a low power components responsible for bias and feedback functions, though appear to be mainly recipients of the noise. Situation with FAN5231 control IC is even more critical as it provides control functions for two independent converters and poor layout design could lead to cross talk between the converters and as a result to degrade in the performance or even malfunction.

Advanced Specification

A multi-layer printed circuit board is recommended. Figure #??? shows the connection of the critical components in the converter.

Dedicate one solid layer for a ground plane.

Dedicate another solid layer as a power plane and break this plane into smaller island of common voltage levels.

Notice all the nodes that are subjected to high dV/dt voltage swing as PHASE1, 2 nodes, for example. All surrounding circuitry will tend to couple the noise from this nodes trough stray capacitance. Do not oversize copper traces connected to these nodes. Do not place traces connected to the feedback components adjacent to these traces.

Keep the wiring traces from the control IC to the MOSFET gate and source as short as possible and capable to handle peak currents up to 2A. Minimize the area within gate-source path to reduce stray inductance and eliminate parasitic ringing at the gate.

Locate small critical components like soft start capacitor and current sense resistors as close, as possible to the respective pins of the IC.

Component Selection Guidelines

Output Capacitor Selection

An output capacitor serves two major functions in a switching power supply. Along with an inductor it filters the sequence of pulses produced by the switcher and supply the load transient currents. The filtering requirements are a function of the switching frequency and the ripple current allowed, and are usually easy to satisfy in high frequency converters.

The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. Modern microprocessors produce transient load rates in excess of 10A/µs. High frequency ceramic capacitors placed beneath the processor socket initially supply the transient and reduce the slew rate seen by the bulk capacitors. The bulk capacitor values are generally determined by the total allowable ESR rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the processor power pins as physically possible. Consult with the processor manufacturer for specific decoupling requirements. For example, Intel recommends that the high frequency de coupling for the Pentium processor to be composed of at least forty 1µF ceramic capacitors in the 1206 surface-mount package.

Use only specialized low-ESR electrolytic capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a transient. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Output Inductor Selection

The minimum practical output inductor value is the one that keeps inductor current just on the boundary of continuous conduction at some minimum load. The industry standard practice is to choose the minimum current some where from 10% to 25% of the nominal current. At light load, FAN5231 PWM controllers switch to a hysteretic mode of operation to sustain high efficiency operation. It is suggested that transition to the hysteretic mode occurred before inductor current becomes discontinuous. Following equations help to choose proper value of the output filter inductor.

$$Imin = \frac{\Delta I}{2}$$

$$L = \frac{Vin - Vout}{Fs \times \Delta I} \times \frac{Vout}{Vin}$$

$$\Delta I = \frac{\Delta Vout}{ESR}$$

MOSFET Selection and Considerations

Requirements to an upper and a lower MOSFETs are different in a mobile applications. The reason for that is 10:1 difference in conduction time of the lower and the upper MOSFETs driven by a difference between the input voltage which is nominally in the range from 8V to 16V while nominal output voltage is about 1.5V.

Requirements to the lower MOSFET are simpler than those to the upper one. The lower Rdson of this device the lower conduction losses, higher converter's efficiency. Switching losses and gate drive losses are not significant because of zero-voltage switching conditions inherent for this device in the buck converter. Important is low reverse recovery charge of the body diode which causes shoot-through current spikes when the upper MOSFET turns on. Also important, is to verify that the lower MOSFET gate voltage does not reach threshold when high dV/dt transition occurs on the phase node. Specially for that reason, FAN5231 is equipped with a very low, 0.5Ω typical, pull-down resistance of low side driver.

Requirements to the upper MOSFET Rdson are less stringent than to the lower MOSFET because its conduction time is significantly shorter while switching losses can dominate especially at higher input voltages. It is recommended to have equal conduction and switching losses in the upper MOSFET at the nominal input voltage and load current. In this case maximum of the converter efficiency is tuned to the operation point when it is most desired.

Precise calculation of power dissipation in the MOSFETs is very complex because many parameters affecting turn-on and turn-off times such as gate reverse transfer charge, gate internal resistance, body diode reverse recovery charge,

package and layout impedances and their variation with the operation conditions are not available to a designer. Following equations are provided only for crude estimation of the power losses and should be accompanied by a detail breadboard evaluation. Attention should be paid to the input voltage extremes where power dissipation in the MOSFETs is usually higher.

$$Pupper = \frac{Io^2 \times Rdson \times Vout}{Vin} + \frac{Io \times Vin \times Fs \times (ton + toff)}{2}$$

$$Plower = Io^2 \times Rdson \times \left(1 - \frac{Vout}{Vin}\right)$$

FAN5231 DC-DC Converter Application Circuit

Figure 4 shows an application circuit of a power supply for a notebook PC microprocessor system. The power supply provides the microprocessor core voltage (V_{core}), the I/O voltage ($V_{I/O}$) and the clock generator voltage (V_{CLK}) from +5-24V_{DC}, +5V_{DC} and +3.3V_{DC}. For detailed information on the circuit, including a Bill-of-Materials and circuit board description, see Application Note ANXXXX.

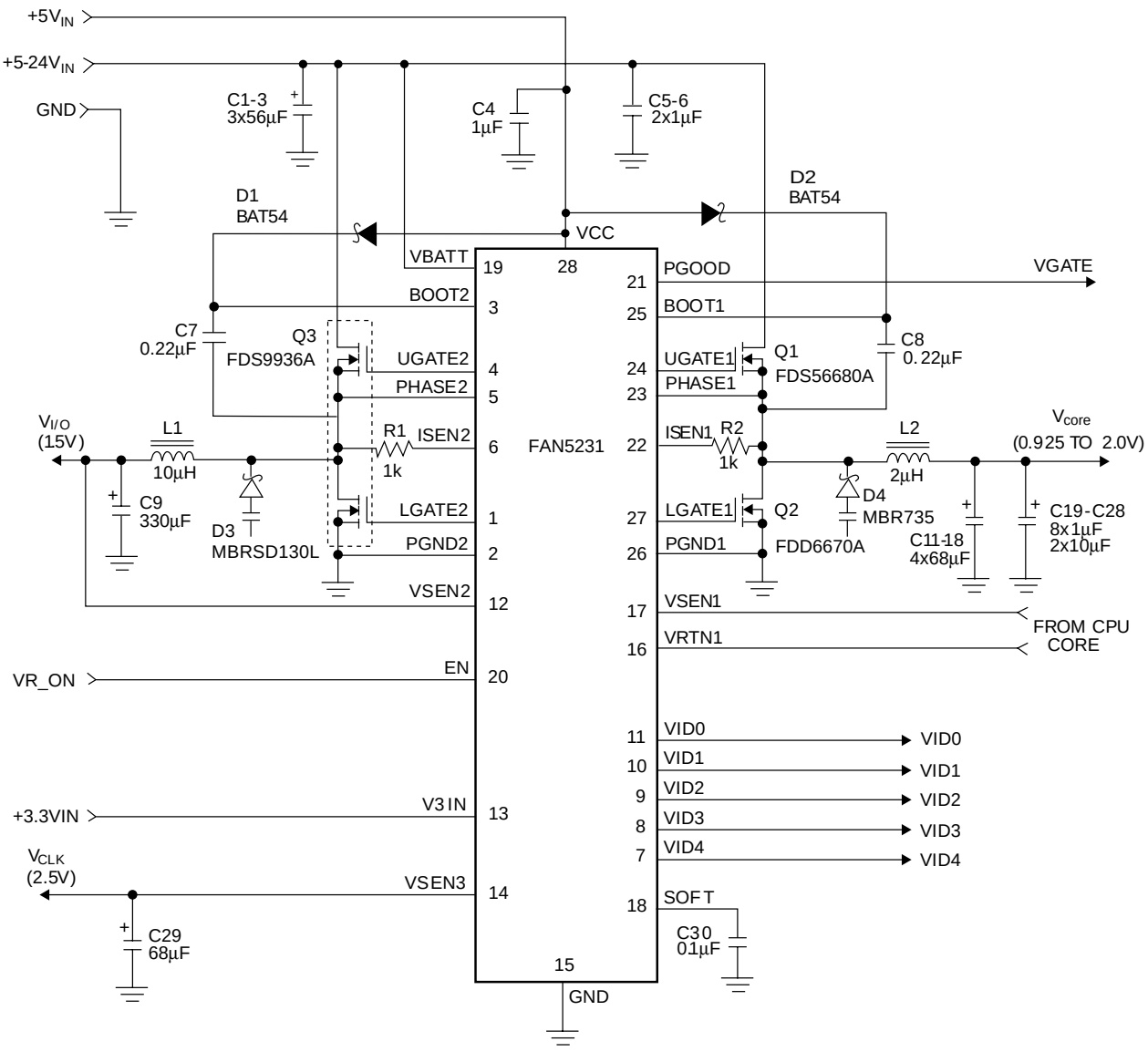


Figure 4. Application Circuit

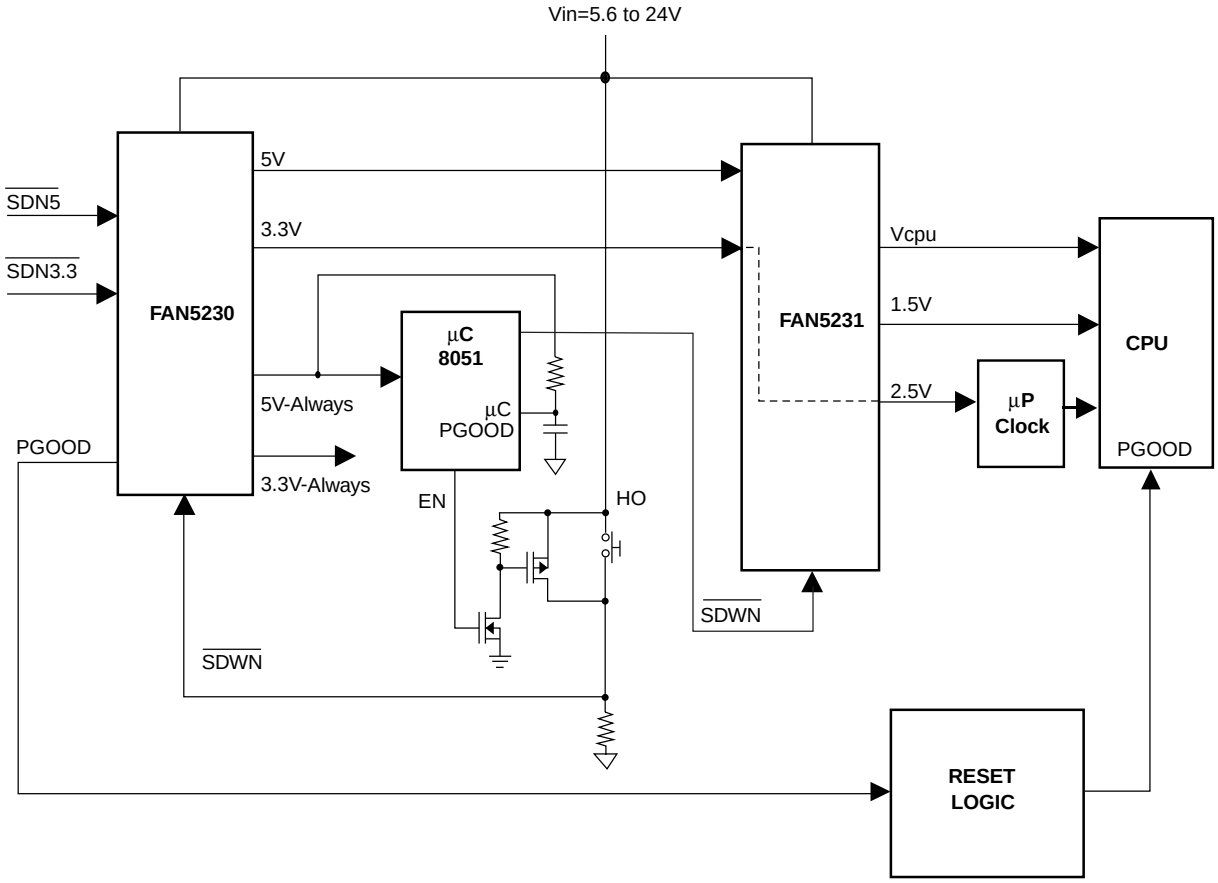


Figure 5. Generic Mobile Block Diagram

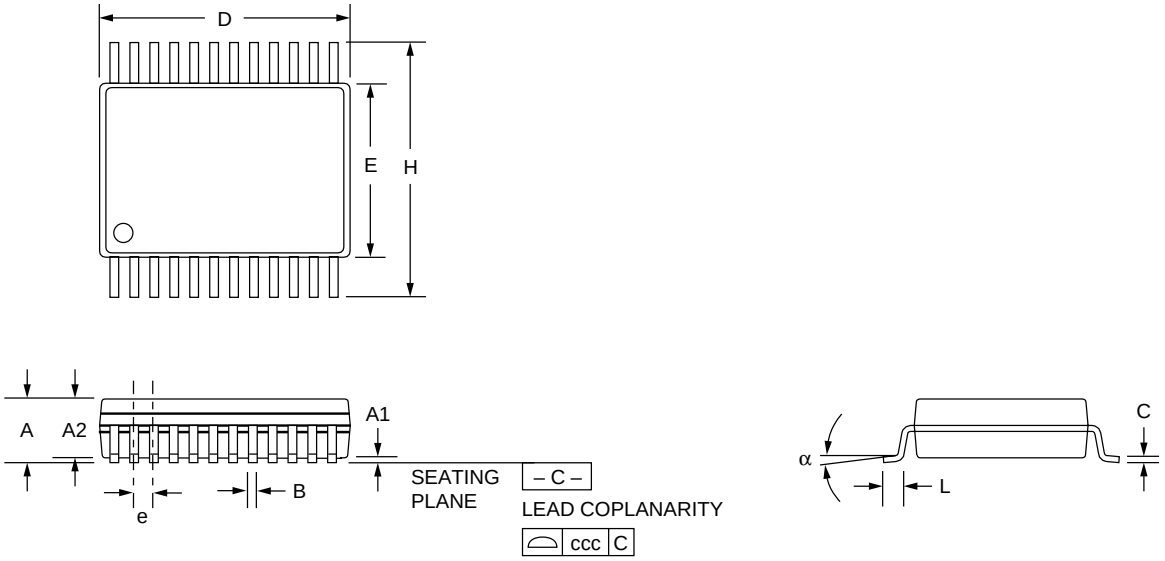
Mechanical Dimensions

Shrink SMall Outline Plastic Packages (QSOP)

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	0.053	0.069	1.35	1.75	
A1	0.004	0.010	0.10	0.25	
A2	-	0.061	-	1.54	
B	0.008	0.012	0.20	0.30	9
C	0.007	0.010	0.18	0.25	
D	0.386	0.394	9.81	10.00	3
E	0.150	0.157	3.81	3.98	4
e	0.025 BSC		0.635 BSC		
H	0.228	0.244	5.80	6.19	
h	0.0099	0.0196	0.26	0.49	5
L	0.016	0.050	0.41	1.27	6
N	28		28		7
α	0°	8°	0°	8°	

Notes:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamber on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the maximum number of terminals.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.



Advanced Specification

Ordering Information

Product Number	Package	Temperature
FAN5231	28 Lead QSOP	0 to 70°C

Advanced Specification