

Architectural Overview

Overall operation of the FMS2701 is controlled by the SMBus which sets register values and interrupt masking. Four sensing inputs are monitored:

1. Remote temperature diode voltage
2. Ambient temperature sensing diode voltage
3. Remote 3.3 volt power supply voltage
4. Local 3.3 volt power supply

Following comparisons against either preset or programmable thresholds, the following hardware outputs are set:

1. Master reset
2. Auxiliary reset
3. Temperature trip point violated ($\overline{\text{THERM}}$)
4. Interrupt ($\overline{\text{INT}}$)

Also set are the following register bits:

1. GPI active (General Purpose Input)
2. Remote Temperature limit exceeded
3. $\overline{\text{THERM}}$ input asserted
4. Remote diode fault

Fan Speed control voltage, FAN_SPD is set in the range 0–2.5V by loading the D/A Register through the SMBus. External $\overline{\text{THERM}} = \text{L}$ forces $\text{FAN_SPD} = 2.5\text{V}$. A Master Reset clears the D/A Register.

Temperature Channel

There are two temperature sense inputs: one for remote sensing; the other for measuring ambient temperature. Both inputs utilize the thermal variation of the voltage drop across a diode, to derive the diode temperature.

Instead of sensing the change in V_D at one current, which is approximately $-2\text{mV}/^\circ\text{C}$, V_D is sampled at two currents ($I_{\text{MAX}} = 10$ and $I_{\text{MIN}} = 100 \mu\text{A}$) to cancel out common error voltages. Difference voltage between the two currents is proportional to absolute temperature:

$$\Delta V_D = \frac{nkT}{q} \cdot \ln \left(\frac{I_{\text{MAX}}}{I_{\text{MIN}}} \right)$$

Where:

n = PN junction ideality factor, typically 1.0065 for the Pentium II thermal diode. Nominal diode sensitivity is $199.7 \mu\text{V}/^\circ\text{C}$.

Following the A/D converter is a DSP block which averages digitized temperature over several samples.

Upper and lower temperature limits are loaded into the limit registers. If a limit is violated, an interrupt is generated. Remote diode open or short circuit fault condition is also sensed.

Power Supply Voltage Monitors

Two Voltage Monitors operating over a 1.0 to 3.8 volt supply range, sense V_{CC3} and V_{CC3AUX} voltages. If input $V_{\text{CC3}} < 2.93$ volt or master reset input, $\overline{\text{MR}} = \text{L}$, then $\overline{\text{RST}} = \text{L}$ until 140 msec after sensing the fault condition.

If the FMS2701 supply, $V_{\text{CC3AUX}} < 2.93$ volt, $\overline{\text{AUXRST}} = \text{L}$ until 140 msec. after sensing the fault condition, and the main reset $\overline{\text{RST}} = \text{L}$ until 180 msec. after $\overline{\text{AUXRST}}$ is cleared. When $\overline{\text{AUXRST}} = \text{L}$, internal reset, $\overline{\text{INTRST}} = \text{L}$. $\overline{\text{AUXRST}}$ is bi-directional, accepting a hard reset input.

SMBus Interface

FMS2701 Registers are accessed through the SMBus interface located at the address $0x2C + n$; where $n = 0, 1, 2$ depending upon the state of ADD , a tri-level input. Within the FMS2701, registers are accessed through an 8-bit bus.

Addressable Memory

Within the FMS2701, there are three sections of addressable memory which implement the following functions.

Command Register (5 locations)

- Configuration
- Interrupt status
- Interrupt mask
- Interrupt status mirror
- Extended function

Read only RAM (2 locations)

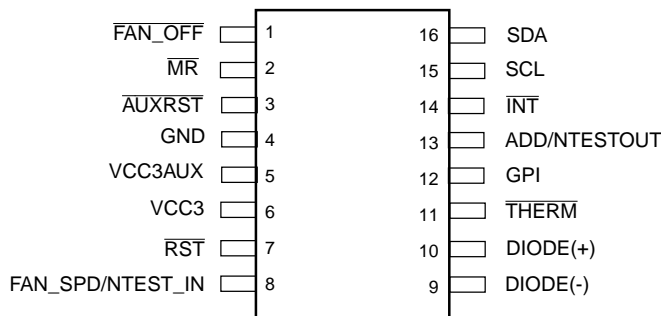
- Company ID
- Revision No.

Value RAM (13 locations)

- Diode temperature, $^\circ\text{C}$
- $\overline{\text{THERM}}$ temperature trip points, $^\circ\text{C}$
- $\overline{\text{INT}}$ temperature limits, $^\circ\text{C}$
- Analog output D/A converter

Write accessible locations have default values that may be overridden by programming through the SMBus interface.

Pin Assignment



Pin Descriptions

Pin No.	Pin Name	Type/Value	Pin Function Description
Reset			
7	RST	Output	Reset. Output pulse from Main Reset Generator, which is tripped by either MR =L or Internal Reset or VCC3 < 2.93 V. When active, RST = L and register D7-0 is cleared.
3	AUXRST	Bi-directional	Auxiliary Reset Input/Output. As an output, AUXRST = L pulse is triggered by VCC3AUX < 2.93 V. As an input, AUXRST = L trips Internal Reset. NAND test input, NTEST_IN is sampled by trailing edge of AUXRST pulse.
2	MR	Input	Manual Reset. Input to Master Reset Generator. If MR = L, a master reset cycle is initiated. MR pin has a 20 kΩ pull-up to VCC3AUX.
Analog I/O			
10	DIODE+	Voltage input/ current source	Positive diode sense input. Current source to remote temperature sensing diode anode and upper voltage sense input.
9	DIODE-	Voltage input/ current sink	Negative diode sense input. Current sink from remote temperature sensing diode cathode and lower voltage sense input.
8	FAN_SPD/NTEST_IN	Analog output/ digital input	Fan speed control voltage output/NAND Test Input. Proportional to the value in register 0x19, output is 0–2.5V. External THERM = L forces a 2.5 volt output. If NTEST_IN = H, the NAND tree test input is enabled for ATE.
Serial Port			
16	SDA	Bi-directional	Data. SMBus data to/from FMS2701
15	SCL	Input	Clock. SMBus clock into FMS2701
13	ADD/NTEST_OUT	Tri-level	SMBus Address Input/NAND Test Output. Lowest two bits of serial port address with three states: 00, 01 and 10, corresponding to H, L and Z inputs. If NTEST_IN is sampled HIGH, the NAND tree test output is enabled.
Digital I/O			
11	THERM	I/O (Open drain)	Thermal Overload. THERM = L indicates that a temperature trip point has been exceeded. Input THERM = L sets the THERM bit in the Interrupt Status Register.
14	INT	Open drain	System interrupt. INT = L when a voltage, temperature limit or temperature trip point is violated and bit 1 of the Configuration Register is set H.

Pin No.	Pin Name	Type/Value	Pin Function Description
12	GPI	Input	General Purpose Input. Sets a bit in the interrupt registers. Assertion polarity is set by the GPI_INV bit. (default is GPI = H causes interrupt)
1	FAN_OFF	Open Drain Output	Fan off request. FAN_OFF reflects the state of the Configuration Register FAN_OFF bit. FAN_OFF = L is a request to shut the fan off.
Power and Ground			
6	VCC3	+3.3 V Input	Voltage Monitor Input. Voltage monitor input to Main Reset Generator. If VCC3 drops below 2.93V, a Main Reset cycle is initiated.
4	GND	0 V	Ground. Return for 3.3 volt supply, VCC3AUX.
5	VCC3AUX	+3.3 V Power	Auxiliary 3.3 volt. Power source for FMS2701. If VCC3AUX drops below 2.93 volt, an Auxiliary Reset cycle is initiated.

Addressable Memory

Addressable memory is divided into two sections:

1. Command, consisting of five registers
2. Value RAM, consisting of thirteen locations, of which: eleven are used to store temperature data, limits and trip points; two are used to store the company ID, version and revision number.

Table 1. Addressable Memory Map

Name	Address	Power-up Value, [7:0]
Configuration Register	0x40	0x25
Interrupt Status Register	0x41	0x00
Interrupt Mask Register	0x43	0x00
Interrupt Status Register Mirror	0x4C	0x00
PTA7-0	0x13	0x46
PTR7-0	0x14	0x64
FTA7-0	0x17	0x46
FTR7-0	0x18	0x64
DAC7-0	0x19	0x00
TR7-0	0x26	0x46
TA7-0	0x27	0x3C
TRHI7-0	0x37	0x50
TRLO7-0	0x38	0x3C
TAHI7-0	0x39	0x46
TALO7-0	0x3A	0x32
Manufacturer ID	0x3E	0xFC
Version, Revision	0x3F	0xCn

Register Definitions

Configuration Register (0x40)

BIT#	Name	Type	Description
0	START	R/W	Start Temperature and Voltage Monitoring 0: Standby mode. (INT is not cleared) 1: Run (Power-up default). All limit and trip values should be entered into FMS2701 registers prior to setting START = 1.

BIT#	Name	Type	Description
1	INT_EN	R/W	Interrupt Enable 0: Disabled (Power-up default) 1: Enables the INT output.
2	INT_CLR	R/W	Interrupt Clear 0: INT output unaffected. 1: Clears the INT output. Contents of the Interrupt Status Register preserved. (Power-up default = 1)
3	TRIP_LOCK	R/(W-once)	Temperature Trip Point Lock 0: THERM trip points set by fixed value registers FTA7-0 and FTR7-0. Writes to programmable registers PTA7-0 and PTR7-0 are enabled. (Power-up default = 0) 1: THERM trip points set by values preserved in programmable registers PTA7-0 and PTR7-0, while RST = H.
4	SOFT_RST	R/W	Soft Reset 0: Power-up default restored by SOFT_RST cycle. 1: Restore power-up values to the Configuration, Interrupt Status, Interrupt Status Mirror and Interrupt Mask registers.
5	FAN_OFF	R/W	Fan Off 0: Set output pin FAN_OFF = L. (fan-off) 1: Set output pin FAN_OFF = Z. (Power-up default, fan-on) If pin THERM = L, then FAN_OFF = H.
6	GPI_INV	R/W	GPI Polarity Invert 0: GPI input passed to Interrupt registers. (Power-up default) 1: Invert the GPI input passed to Interrupt registers
7	Reserved	R/W	Reserved (Default=0)

Interrupt Status Register¹ (0x41)

BIT#	Name	Type	Description															
0	ATV	R	Ambient Temperature Violation 0: On-chip temperature within limits. 1: On-chip temperature limit violated															
1	Reserved	R	Reserved for Remote Thermal Diode 2 temp error															
2	Reserved	R	Reserved for Remote Thermal Diode 2 fault															
3	Reserved	R	Undefined															
4	GPI	R	General Purpose Input Status. GPI is set according to the following truth table: <table border="1" style="margin-left: 40px;"> <thead> <tr> <th>GPI pin</th> <th>GPI_INV</th> <th>GPI bit</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table> Reading this register will not clear the GPI bit.	GPI pin	GPI_INV	GPI bit	0	0	0	1	0	1	0	1	1	1	1	0
GPI pin	GPI_INV	GPI bit																
0	0	0																
1	0	1																
0	1	1																
1	1	0																
5	RTV	R	Remote Temperature Violation. 0: Remote temperature within limits. 1: Remote temperature limit violated															
6	THERM	R	THERM input status. 0: THERM input negated. ($\overline{\text{THERM}} = \text{H}$) 1: THERM input asserted. ($\overline{\text{THERM}} = \text{L}$)															

BIT#	Name	Type	Description
7	FAULT	R	Remote Diode Fault. 0: Diode functional 1: Remote temperature sensing diode short or open circuit.

Note:

1. Reading this register will clear ATV, RTV \overline{THERM} and FAULT bits.

Interrupt Mask Register (0x43)

BIT#	Name	Type	Description
0	MSKATV	R/W	Mask Ambient Temperature Violation bit. 0: Allow ATV bit to affect \overline{INT} output. 1: Prohibit ATV bit from affecting the \overline{INT} output.
1	Reserved	R	Undefined
2	Reserved	R	Undefined
3	Reserved	R	Undefined
4	MSKGPI	R/W	Mask GPI bit 0: Allow GPI bit to affect \overline{INT} output. 1: Prohibit GPI bit from affecting the \overline{INT} output.
5	MSKRTV	R/W	Mask Remote Temperature Violation bit. 0: Allow RTV bit to affect \overline{INT} output. 1: Prohibit RTV bit from affecting the \overline{INT} output.
6	MSKTHERM	R/W	Mask THERM bit. 0: Allow THERM bit to affect \overline{INT} output. 1: Prohibit THERM bit from affecting the \overline{INT} output.
7	MSKFAULT	R/W	Mask Remote Fault bit. 0: Allow FAULT bit to affect \overline{INT} output. 1: Prohibit FAULT bit from affecting the \overline{INT} output.

Note:

1. An error that causes continuous interrupts to be generated may be masked using the mask register, until the error can be alleviated.

Interrupt Status Mirror Register¹ (0x4C)

BIT#	Name	Read/Write	Description															
0	MATV	R	Mirrored Ambient Temperature Violation 0: On-chip temperature within limits. 1: On-chip temperature limit violated															
1	Reserved	R	Reserved for Remote Thermal Diode 2 temp error															
2	Reserved	R	Reserved for Remote Thermal Diode 2 fault															
3	Reserved	R	Undefined															
4	MGPI	R	Mirrored General Purpose Input Status. MGPI is set according to the following table: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>GPI pin</th> <th>GPI_INV</th> <th>MGPI</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table> Reading this register will not clear the GPI bit.	GPI pin	GPI_INV	MGPI	0	0	0	1	0	1	0	1	1	1	1	0
GPI pin	GPI_INV	MGPI																
0	0	0																
1	0	1																
0	1	1																
1	1	0																
5	MRTV	R	Mirrored Remote Temperature Violation. 0: Remote temperature within limits. 1: Remote temperature limit violated															

BIT#	Name	Read/Write	Description
6	M THERM	R	Mirrored THERM input status. 0: THERM input negated. ($\overline{\text{THERM}} = \text{H}$) 1: THERM input asserted. ($\text{THERM} = \text{L}$)
7	MFAULT	R	Mirrored Remote Diode Fault. 0: Diode functional 1: Remote temperature sensing diode short or open circuit.

Note:

1. Reading this register will clear MATV, MRTV, M THERM and MFAULT bits.

Extended Function Register (0x15)

BIT#	Name	Type	Description
0	MIT	R	Mask Internal THERM 0: Internally generated THERM affects $\overline{\text{INT}}$ output. 1: Internally generated THERM does not impact $\overline{\text{INT}}$ output.
7-1	-	N/A	Reserved

Value RAM (0x13-0x4A)

Unless stated otherwise, Power-on defaults are not defined,.

Address	Name	Type	Description
0x13	PTA7-0	R/W	Programmable Ambient Temperature Automatic Trip Point. If $\text{TA}_{7-0} > \text{PTA}_{7-0}$, then $\overline{\text{THERM}} = \text{L}$. Write access is disabled if the TRIP_LOCK bit in the Configuration Register been set. (default: 46h (70°C))
0x14	PTR7-0	R/W	Programmable Remote Thermal Diode Automatic Trip Point. If $\text{TR}_{7-0} > \text{PTR}_{7-0}$, then $\overline{\text{THERM}} = \text{L}$. Write access is disabled if the TRIP_LOCK bit in the Configuration Register been set. (default: 64h (100°C))
0x17	FTA7-0	R	Fixed Ambient Temperature Automatic Trip Point. (default: 46h (70°C))
0x18	FTR7-0	R	Fixed Remote Thermal Diode Automatic Trip Point. (default: 64h (100°C))
0x19	DAC7-0	R/W	D/A Converter Input. Value supplied to D/A converter to generate fan speed control voltage. (default: 00h)
0x20		N/A	Reserved
0x26	TR7-0	R	Remote Thermal Diode Temperature. Temperature output derived from remote thermal diode.
0x27	TA7-0	R	Ambient Temperature. Temperature output derived from on-chip thermal diode.
0x2B	-	N/A	Reserved
0x2C	-	N/A	Reserved
0x37	TRHI7-0	R/W	Remote Thermal Diode High Temperature Limit. $\text{TR}_{7-0} > \text{TRHI}_{7-0}$ will set the RTV and MRTV bits in the Interrupt and Mirrored Interrupt registers.
0x38	TRLO7-0	R/W	Remote Thermal Diode Low Temperature Limit. $\text{TR}_{7-0} < \text{TRLO}_{7-0}$ will set the RTV and MRTV bits in the Interrupt and Mirrored Interrupt registers.
0x39	TAHI7-0	R/W	Ambient Temperature High Temperature Limit. $\text{TA}_{7-0} > \text{TAHI}_{7-0}$ will set the ATV and MATV bits in the Interrupt and Mirrored Interrupt registers.
0x3A	TALO7-0	R/W	Ambient Temperature Low Temperature Limit. $\text{TA}_{7-0} < \text{TALO}_{7-0}$ will set the ATV and ARTV bits in the Interrupt and Mirrored Interrupt registers.
0x3E	MFR7-0	R	Manufacturer ID. Value is FC.
0x3F	NUM7-0	R	Version and Revision. NUM7-4 = C, the FMS2701 version number. NUM3-0 = revision number
0x44 - 0x4A	-	N/A	Reserved
0x4D - 0x53	-	N/A	Reserved

Functional Description

Operation of the FMS2701 is divided into three sections:

- Temperature Processor
- Reset Generators
- Data Processor

Temperature Processor

Remote and ambient thermal diode voltages are processed by the Temperature Processor which outputs values of remote and ambient temperature alternately. Inputs are derived from a remote diode that is connected by two wires to the input of the processor; and the ambient diode, which is located on-chip. Output is supplied to the Data Processor which loads the TA7-0 and TR7-0 registers with the digitized ambient and remote temperatures.

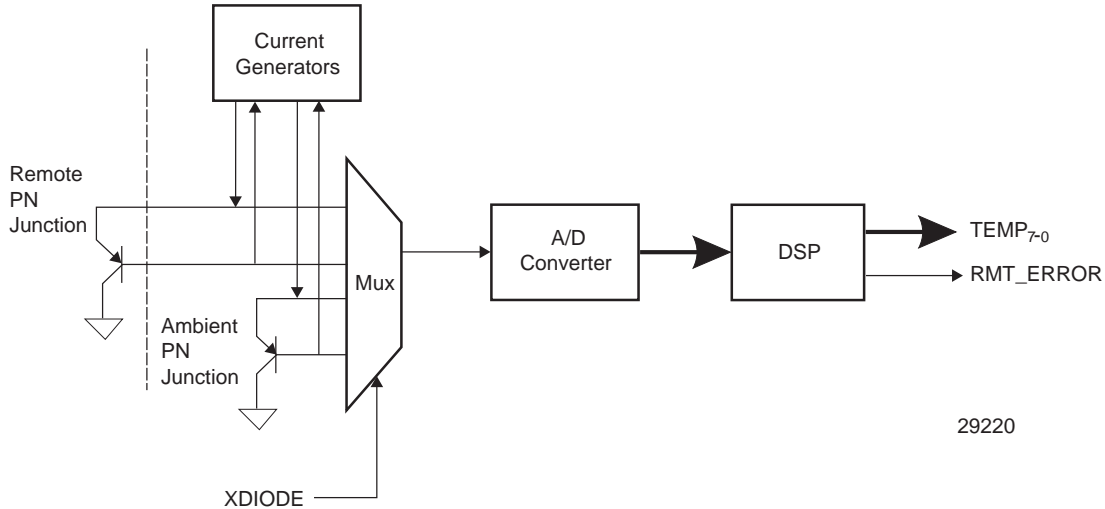


Figure 1. Temperature Processor Block Diagram

A multiplexer selects the thermal diode to be sensed. Voltage of the diode is sensed at two currents: 10 and 100 μ A. During the diode sampling interval, the A/D converter digitizes low and high current samples. DSP averages and subtracts the samples to output an 8-bit temperature that is updated a rate greater than 1 Hz. Remote and Ambient diode temperatures are outputted alternately on the TEMPR[7:0] bus which is connected to the Data Processor.

Remote Diode fault sensing is included within the DSP block. If the remote diode voltage indicates either a short or an open circuit, the RMT_ERROR signal causes the RMT_FAULT bit to be set in the Interrupt Status Register.

Temperature data format is 8-bit, two's complement with the LSB equivalent to 1.0°C. Range and conversion between °C and equivalent binary and hexadecimal data is exemplified in Table 2.

Table 2. Temperature/Data Conversion/Format

Temperature	Digital Output	
	Binary	Hex
+125°C	0111 1101	0x7D
+25°C	0001 1001	0x19
+1.0°C	0000 0001	0x01
0°C	0000 0000	0x00
-1.0°C	1111 1111	0xFF
-25°C	1110 0111	0xE7
-55°C	1100 1001	0xC9

Reset Generators

There are two reset generators:

1. Auxiliary Reset
2. Main Reset

Auxiliary Reset responds to the power supply voltage, VCC3AUX applied to the FMS2701. Main Reset responds to a separate power supply voltage level, VCC3. Threshold level of both reset generators is 2.93 volt. If $1.0\text{ V} < \text{VCC3AUX} < 2.93$ both generators output an active L reset level.

Auxiliary Reset Generator

The Auxillary Reset Generator responds to either a low value of VCC3AUX by outputting an $\overline{\text{AUXRST}} = \text{L}$ pulse and an internal reset pulse, $\overline{\text{INTRST}}$; or to an external $\overline{\text{AUXRST}}$ input by emitting an internal reset. Internal reset restores power-up register values (except DAC7-0 which is cleared by RST) and initiates a Master Reset Cycle.

In Figure 2, $\text{VCC3AUX} < 2.93\text{V}$ represents the state of the VCC3AUX power supply voltage.

$\overline{\text{AUXRST}}$ is a bi-directional pin. $\overline{\text{AUXRST}}(\text{OUT})$ signifies an outgoing signal. $\overline{\text{AUXRST}}(\text{IN})$ signifies an incoming signal. Auxiliary Reset is triggered by either of two events:

1. **VCC3AUX < 2.93 volt.** After a VCC3AUX < 2.93 transition:
 - a) $\overline{\text{AUXRST}}(\text{OUT}) = \text{L}$, continuing low for 140 msec. after VCC3AUX > 2.93 volt.
 - b) $\overline{\text{INTRST}} = \text{L}$, while $\overline{\text{AUXRST}}(\text{OUT}) = \text{L}$.
2. **$\overline{\text{AUXRST}}(\text{IN}) = \text{L}$.** In response, $\overline{\text{INTRST}} = \text{L}$, continuing low until $\overline{\text{AUXRST}}(\text{IN}) = \text{H}$

Internal reset, $\overline{\text{INTRST}}$ tracks $\overline{\text{AUXRST_OUT}}$. To terminate a reset cycle, VCC3AUX must rise above 2.93 volt. During power-up, the $\overline{\text{AUXRST}}$ output remains low until the 2.93 volt threshold is reached.

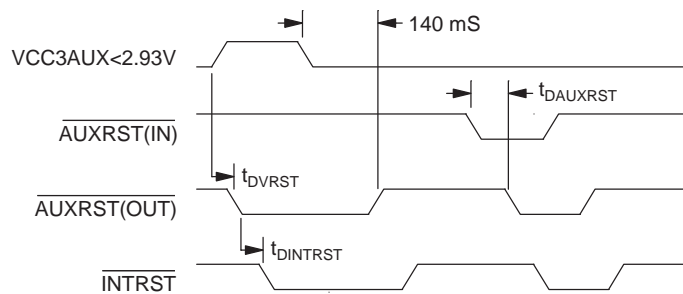


Figure 2. Timing Diagram, Auxiliary Reset

Main Reset

Depending upon the source of reset, the Main Reset Generator outputs either a 140 or a 180 msec. pulse as shown in Figure 3. $\text{VCC3} < 2.9$ represents the state of the VCC3

power supply voltage. $\overline{\text{RST}} = \text{L}$ clears the D/A Converter register.

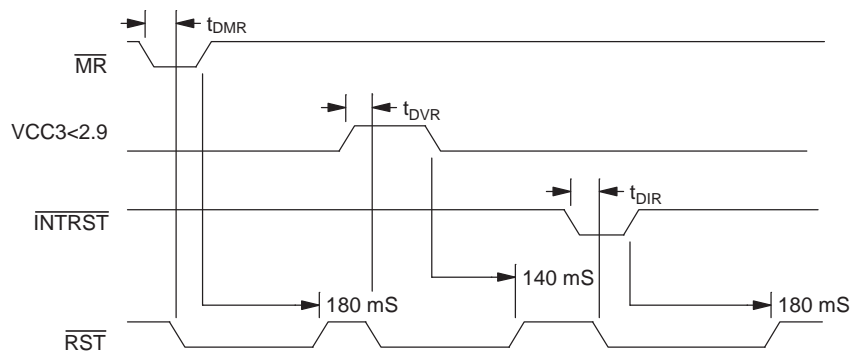


Figure 3. Timing Diagram, Main Reset

Internal Reset

Internal reset, $\overline{\text{INTRST}}$ originates from the Auxiliary Reset Generator. When power is supplied to the FMS2701 via VCC3AUX, output $\overline{\text{INTRST}} = \text{L}$ for 140 msec. after VCC3AUX transitions >2.93 volt. $\overline{\text{INTRST}} = \text{L}$ instigates four events:

1. Configuration, Interrupt and Mask registers are reset to default values.
2. $\overline{\text{THERM}}$ Temperature Trip Point registers: PTA7-0, PTR7-0, FTA7-0, FTR7-0 are set to default values.
3. DAC7-0 register is set to 0x00.
4. Temperature Processor and Data Processor are reset.

Data Processor

Based upon setup commands via the SMBus, the Data Processor gathers sensor inputs from the Temperature Processor and Reset Generators. Temperature inputs are compared against values stored in the Trip and Limit registers. Fault conditions set flags in the interrupt registers and activate the $\overline{\text{THERM}}$ and $\overline{\text{INT}}$ outputs. Temperature and interrupt status are passed to the host via the SMBus interface. Host commands set the FMS2701 configuration, interrupt masking and the fan speed.

Preliminary Information

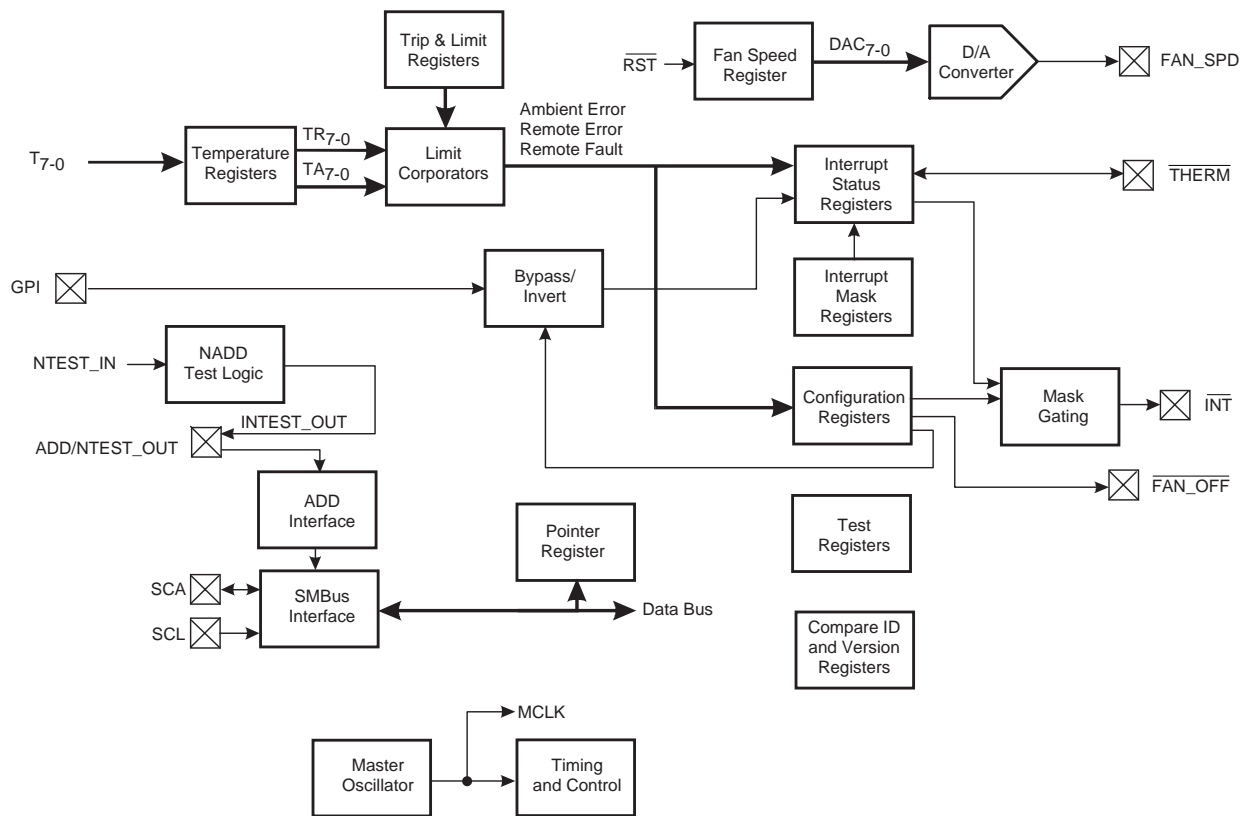


Figure 4. Data Processor Block Diagram

SMBus Interface

FMS2701 register access is via a 2-wire SMBus interface. Base address is $0x2C + n$, where n is an offset defined by the state of the ADD pin: Z, H, L == 0, 1, 2. (see Table 3) State Z corresponds to the ADD pin being open circuit.

Two signals comprise the bus: clock (SCL) and bi-directional data (SDA). When receiving and transmitting data through the serial interface, the FMS2701 acts as a slave, responding only to commands by the SMBus master.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA may change only when SCL = L. An SDA transition while SCL = H is interpreted as a start or stop signal.

Table 3. Serial Port Slave Addresses

ADD	Address
Z	2C
H	2D
L	2E

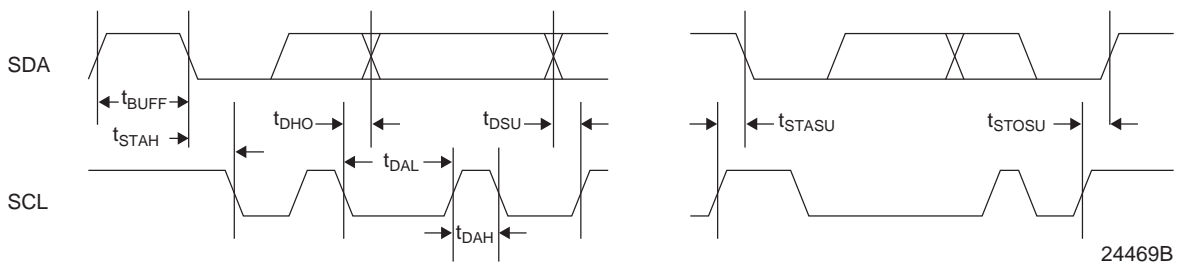


Figure 5. SMBus: Read/Write Timing

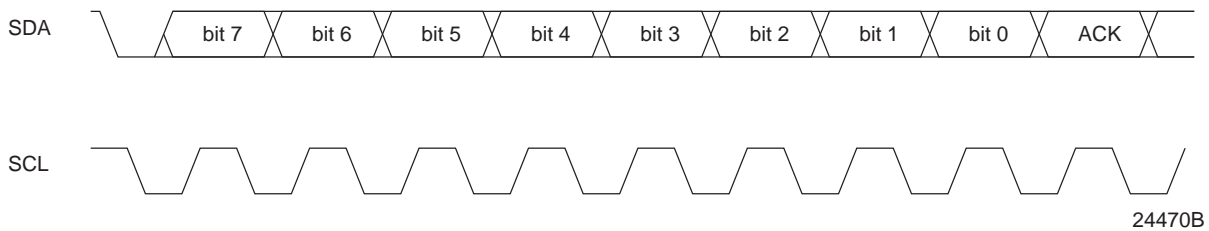


Figure 6. SMBus: Typical Byte Transfer

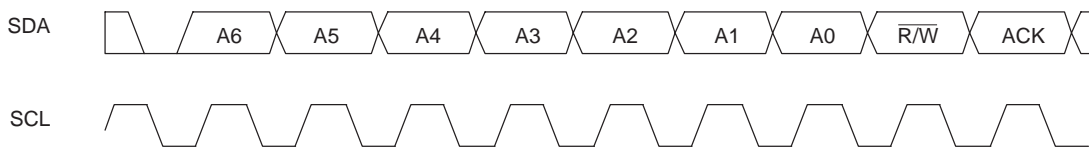


Figure 7. SMBus: Slave Address with Read/Write Bit

There are five steps within an SMBus cycle:

1. Start signal
2. Slave address byte
3. Pointer register address byte
4. Data byte to read or write
5. Stop signal

When the SMBus interface is inactive ($SCL = H$ and $SDA = H$) communications are initiated by sending a start signal. The start signal (Figure 5, left waveform) is a HIGH-to-LOW transition on SDA while SCL is HIGH. This signal alerts all slaved devices that a data transfer sequence is imminent.

After a start signal, the first eight bits of data that are transferred, comprise a seven bit slave address followed a single R/W bit (Read = H, Write = L). As shown in Figure 6, the R/W bit indicates the direction of data transfer: read from; or write to the slave device. If the transmitted slave address matches the address of the FMS2701 which set by the state of the ADD pin, the FMS2701 acknowledges by pulling SDA LOW on the 9th SCL pulse (see Figure 7) to send an acknowledge bit, ACK. If the addresses do not match, the FMS2701 does not acknowledge.

For each byte of data read or written, the MSB is the first bit of the sequence.

DATA TRANSFER

If a slave device such as the FMS2701 does not acknowledge the master device during a write sequence, SDA remains HIGH so that the master can generate a stop signal. During a read sequence, if the master device does not acknowledge ($ACK = L$), the FMS2701 interprets this as “end of data.” SDA remains HIGH so the master can generate a stop signal.

To write data to a specific FMS2701 control register, three bytes are sent:

1. Write the slave address byte with bit $\overline{R/W} = L$.
2. Write the pointer byte.
3. Write to the control register indexed by the pointer.

Data is read from the control registers of the FMS2701 in a similar manner, except that two data transfer operations are required:

1. Write the slave address byte with bit $\overline{R/W} = L$.
2. Write the pointer byte.
3. Write the slave address byte with bit $\overline{R/W} = H$
4. Read the control register indexed by the pointer.

Preceding each slave write, there must be a start cycle. Following the pointer byte there should be a stop cycle. After the last read, there must be a stop cycle comprising a LOW-to-HIGH transition of SDA while SCL is HIGH. (see Figure 5, right waveform)

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

Serial Interface Read/Write Examples

Examples below show how serial bus cycles can be linked together for multiple register read and write access cycles. For sequential register accesses, each ACK handshake initiates further SCL clock cycles from the master to transfer the next data byte.

Write to one control register

1. Start signal
2. Slave Address byte ($\overline{R/W}$ bit = LOW)
3. Pointer byte
4. Data byte to base address
5. Stop signal

Read from one control register

1. Start signal
2. Slave Address byte ($\overline{R/W}$ bit = LOW)
3. Pointer byte (= base address)
4. Stop signal
5. Start signal
6. Slave Address byte ($\overline{R/W}$ bit = HIGH)
7. Data byte from base address
8. Stop signal

Addressable Memory

Although the FMS2701 will respond to external inputs, control of the operation of the FMS2701 is through the internal registers. Following power-up, registers are set to default values. After a 140 msec. power up reset delay, the FMS2701 will begin checking sensor inputs to determine if the temperature in voltages fall within default limits.

These default values may be overridden by changing the values stored in the Value RAM. If the PTA7-0 and PTR7-0 values are changed, then the TRIP_LOCK (Temperature Trip Point Lock) bit in the Configuration Register must be set to enable temperature values to be compared against the programmable rather than the fixed trip point values. If the temperature limit values are changed, then the changes are effective immediately. Interrupt masking (register 0x43), enabling (INT_EN bit) and clearing (INT_CLR bit) can be used to disable interrupts during register setup.

There are four control registers and 21 Value RAM locations, with functions and bit assignments defined in the Addressable Memory section.

D/A Converter

An 8-bit D/A converter supplies a voltage to the FAN_SPD pin which, can be used to control the speed of a fan. Input of the D/A converter is connected to the DAC7-0 register. DAC7-0 value is loaded from the SMBus. In the event of a THERM condition, the DAC7-0 output remains unchanged but the D/A converter output is set full scale, equivalent to DAC7-0 = 0xFF. RST = L clears DAC7-0 in the fan speed register.

THERM Processing

THERM is a bi-directional pin with an open drain output. When the THERM output is asserted L, the THERM input is disabled. Figure 8 depicts the logical flow of the internal and external THERM signals, showing the origins and destinations.

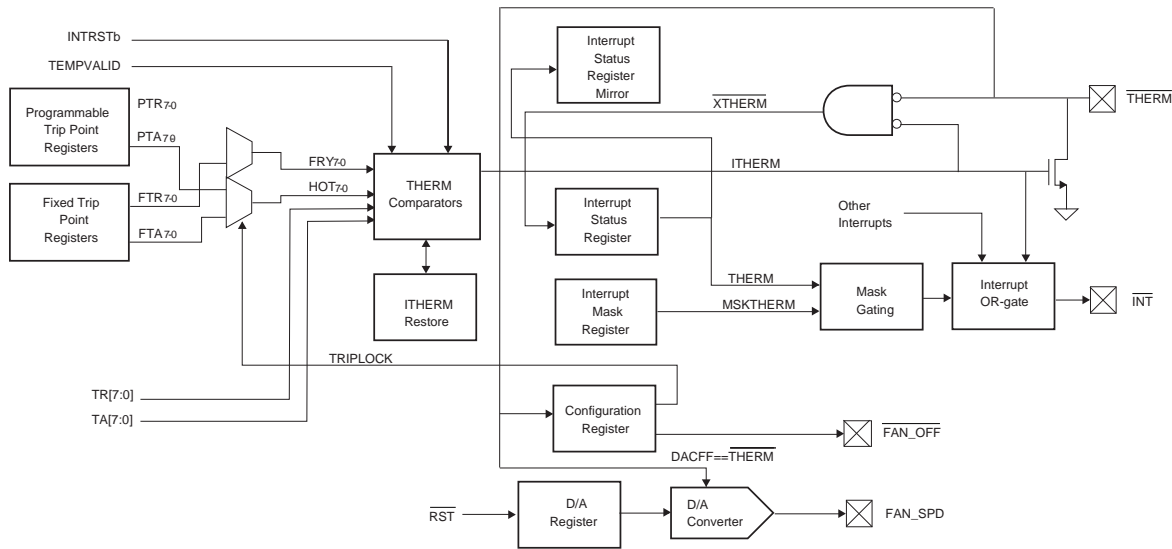


Figure 8. THERM I/O Structure/Detail

As an input, if THERM = L the following events occur:

1. If the mask bit, MSKTHERM = L, output pin, INT = L
2. Configuration Register bit, FAN_ON = H.
3. Output pin, FAN_SPD = 2.5 V for maximum fan speed but register DAC7-0 is unchanged.
4. Interrupt Status Register bit, THERM = H.
5. Interrupt Status Register Mirror bit, MOTHERM = H.

As an output, ITHERM = H, causes THERM = L; ITHERM = L, causes THERM = Z, open drain. ITHERM = H, if any of the following conditions occur:

1. If Configuration Register bit, TRIPLOCK = H and Programmable Ambient Temperature Automatic Trip Point PTA7-0 is exceeded.
2. If Configuration Register bit, TRIPLOCK = H and Programmable Remote Temperature Automatic Trip Point PTR7-0 is exceeded.

3. If Configuration Register bit, TRIPLOCK = L and Fixed Ambient Temperature Automatic Trip Point FTA7-0 is exceeded.
4. If Configuration Register bit, TRIPLOCK = L and Fixed Remote Temperature Automatic Trip Point FTR7-0 is exceeded.

TRIPLOCK is Temperature Trip Point Lock bit in the Configuration Register.

After a Trip Point has been exceeded, to restore the open drain output, THERM = Z, the temperature must fall 5°C below the trip point.

INT Processing

INT is a hardware interrupt output. INT operation is controlled by the Configuration Register bits: INT_EN and INT_CLR bits, which enable and clear the open drain INT output. Subject to the setting of the Interrupt Mask Register,

INT = L, if any bit in the Interrupt Register is active. Otherwise INT = Z, open drain. Figure 9 depicts the logical flow of the interrupt sources to the INT output.

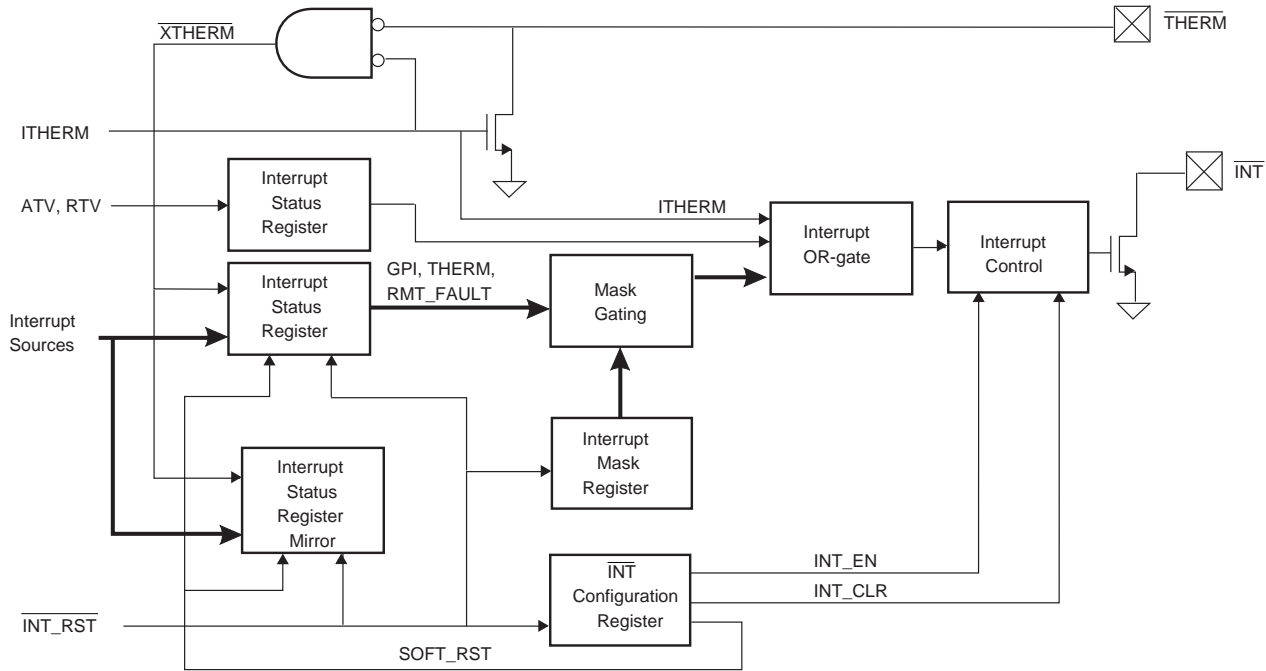


Figure 9. INT Output Structure

With Configuration Register bits INT_EN = 1 and INT_CLR = 0, output pin INT = L, if any of the following bits are set in the Interrupt Register:

1. ATV: An ambient temperature limit is violated indicating that the on-chip temperature falls outside the boundaries established by TALO7-0 and TAHI7-0.
2. GPI: General Purpose Input, GPI is asserted. Polarity of the GPI pin is determined by the setting of the GPI_INVNT bit in the Configuration Register.
3. RTV: A remote thermal diode temperature limit is violated, indicating that the temperature falls outside the boundaries established by TRLO7-0 and TRHI7-0.
4. THERM: Temperature exceeds an selected automatic trip point (PTA7-0, PTR7-0, FTA7-0, or FTR7-0) causing output THERM = L or the THERM input = L even if the THERM bit in the Interrupt Register is masked.

5. RMT_FAULT: Remote diode is either open or short circuit.

Output pin INT = Z, clearing the interrupt output, if any of the following events occur:

1. Interrupt Status Register is read, causing this register to be cleared to the default state.
2. Configuration Register bit INT_CLR = 1, which is the default condition following an internal reset.
3. Configuration Register bit INT_EN = 0, which is the default condition following an internal reset.

Status of the INT_CLR and INT_EN bits does not impact the contents of the Interrupt Status or the Interrupt Status Mirror Registers. Reading the Interrupt Status Registers clears only that register. Reading the Interrupt Status Mirror Register, clears only that register.

Note that setting the $\overline{\text{INT}}$ output by exceeding a temperature limit is an edge-driven event. Only when the temperature actually crosses the limit boundary does $\text{INT} \setminus$ transition LOW. An example of interrupts caused by a series of temperature, T transitions across temperature limits is shown in Figure 10. Temperature limits are fixed for the first series of temperature

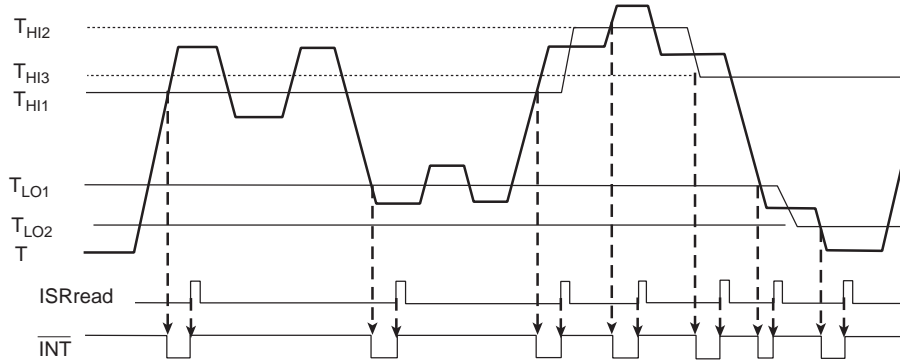


Figure 10. Profile of Temperature Driven Interrupts

ATV and RTV bits operate in conjunction with the $\overline{\text{INT}}$ output and Interrupt status Register as follows:

- When the temperature exceeds a high limit, the corresponding Interrupt Status Register bit, either ATV or RTV is set.
- Reading the Interrupt Status Register clears ATV and RTV.
- Once the high limit has been exceeded, a subsequent transitions through the high level will not cause an interrupt, unless:
 - The temperature passes through the low limit.
 - Or, the high temperature limit is changed.
- If the high temperature limit is changed from a level above the temperature to a level below, then the relevant Interrupt Status Register bit, either ATV or RTV is set.
- If the temperature falls below a low limit, the corresponding Interrupt Status Register bit, either ATV or RTV is set.
- Once the low limit has been exceeded, a subsequent transitions through the low level will not cause an interrupt, unless:
 - The temperature passes through the high limit.
 - Or, the low temperature limit is changed.
- If the low temperature limit is changed from a level below the ambient/remote temperature to a level above, then the ATV/RTV bit is set.

GPI—General Purpose Input

GPI is a General Purpose Input that can be used to trigger an interrupt. Configuration Register bit GPI_INVT determines the polarity of the GPI input. Interrupt Register bit, $\text{GPI} = \text{H}$ sets output $\overline{\text{INT}} = \text{L}$ if Mask Register bit $\text{MSK_GPI} = \text{L}$.

Limit and Trip Point Comparators

Temperature register outputs, TR7-0 and TA7-0 are compared with the limit values TRHI7-0 , TRLO7-0 , TAHI7-0 and TALO7-0

excursions. Then, for the second series, following the THI1 violation, the THI limit is raised from THI1 to THI2 . If THI is reprogrammed from a value above T to a value below THI , then an interrupt is generated. $\overline{\text{INT}}$ is cleared by reading the Interrupt Status Register (ISRread).

that are stored in the Limit Registers. Out of range TA7-0 and TR7-0 values set the INT bit in the Interrupt Status Register.

TR7-0 and TA7-0 are also compared with the values in Trip Point Registers, PTA7-0 and PTR7-0 if these registers have been loaded or FTA7-0 and FTR7-0 , which contain power up default values. If a trip point is violated, two outputs are asserted: $\overline{\text{THERM}} = \text{L}$ and $\text{FAN_SPD} = \text{H}$.

Mask Gating

Setting the corresponding bit in the Interrupt Mask Register can mask any bit in the Interrupt Status Register.

Timing and Control

Timing and Control logic generates a master clock and orchestrates on-chip timing.

NAND Gate Test

A selectable NAND tree test is provided for Automated Test Equipment (ATE) board level connectivity testing. NAND tree test mode is enabled by setting the input pin, $\overline{\text{FAN_SPD}} \text{NTEST_IN} = \text{H}$, while the $\overline{\text{AUXRST}}$ output transitions L to H, causing the output of a D flip-flop to:

- Enable the NAND tree output, connecting it to the ADD/NTEST_OUT pin.
- Disable the D/A converter output to the $\overline{\text{FAN/SPD}} \text{NTEST_IN}$.

To perform a NAND tree test, NAND tree pins should be driven high.

Each pin is toggled in turn to generate an output pattern with values that can be verified against those shown in Table 4.

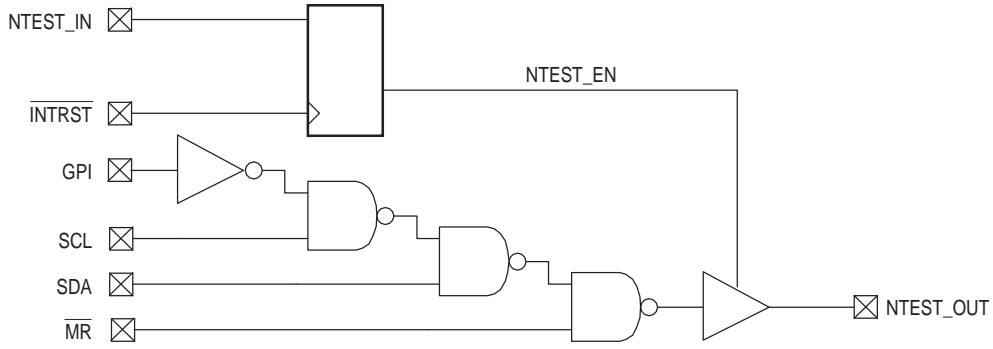


Figure 11. NAND Tree Test Logic

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Table 4. NAND Tree Truth Table

GPI	SCL	SDA	MR	ADD/NTESTOUT
0	0	0	0	1
0	0	0	1	0
0	0	1	1	1
0	1	1	1	0
1	1	1	1	1

To implement the NAND-TREE test on a PWB, no pins listed in the tree should be connected directly to power or ground. Instead, pins should be biased through a low load resistor with a value of 1.0 k to 100 k to allow ATE to drive pins high/low.

Equivalent Circuits

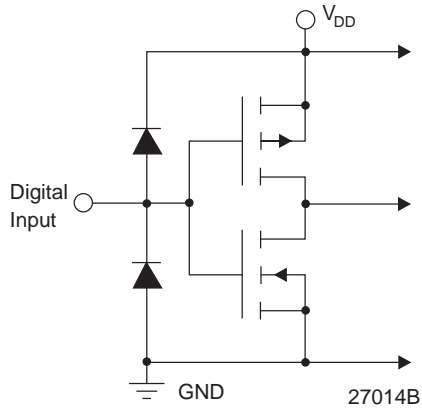


Figure 12. Equivalent Digital Input Circuit

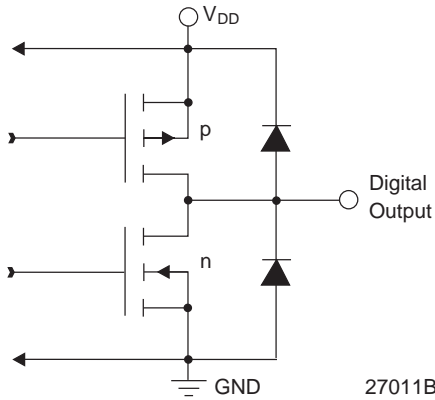


Figure 13. Equivalent Digital and D/A Output Circuit

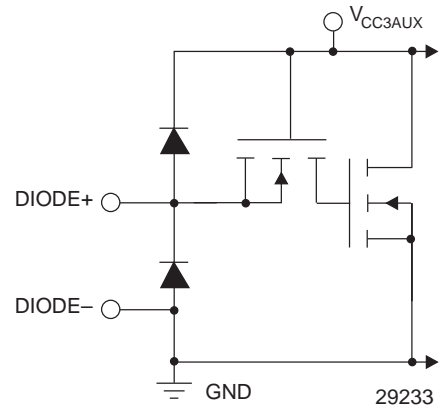


Figure 14. Equivalent Remote Diode Interface Circuit

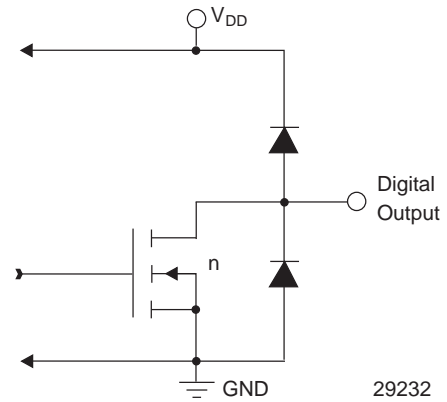


Figure 15. Equivalent Open Drain Output Circuit

Preliminary Information

Absolute Maximum Ratings (beyond which the device may be damaged)¹

Parameter	Min	Typ	Max	Unit
Power Supply Voltages				
VCC3AUX (Measured to GND)	-0.5	3.3	5.75	V
VCC3AUX (Measured to GND)		3.3		V
Digital Inputs				
3.3 V logic applied voltage (Measured to GND) ²	-0.3		VCC3AUX + 0.3	V
Forced current ^{3, 4}	-5.0		5.0	mA
Analog Inputs				
Applied Voltage (Measured to GND) ²	-0.5		VCC3AUX + 0.5	V
Forced current ^{3, 4}	-10.0		10.0	mA
Digital Outputs				
3.3 V logic applied voltage (Measured to GND) ²	-0.5		VDD3AUX + 0.5	V
Forced current ^{3, 4}	-10.0		10.0	mA
Short circuit duration (single output in HIGH state to ground)			1	second
Temperature				
Operating, Ambient	-40		125	°C
Junction			150	°C
Lead Soldering (10 seconds)			300	°C
Vapor Phase Soldering (1 minute)			220	°C
Storage	-65		150	°C
Electrostatic Discharge ⁵			±150	V

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.
5. EIAJ test method.

Operating Conditions

Parameter		Min	Nom	Max	Units
VCC3AUX	Digital Power Supply Voltage		3.3		V
TA	Ambient Temperature, Still Air	-40		125	°C

Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
Power Supply Currents						
IVCC3AUX	3.3 volt current	Operating		1	2	mA
		Standby		0.5		mA
Digital Inputs/Outputs						
CI	Input Capacitance			5	10	pF
CO	Output Capacitance			10		pF
I _{IH}	Input Current, HIGH		-1	0.005		μA
I _{IL}	Input Current, LOW			0.005	+1	μA
I _{ILR}	Input Current, LOW, Master Reset	$\overline{MR} = L$		200		μA
V _{IH}	Input Voltage		2.0			V
V _{IL}	Input Voltage				0.8	V
I _{OZH}	Output Current, HIGH, open drain			-0.1	100	μA
I _{OH}	Output Current, HIGH				-2	mA
I _{OL}	Output Current, LOW	Other / FAN_OFF			3 / 6	mA
V _{OH}	Output Voltage, HIGH	I _{OH} = max.	2.4			V
V _{OL}	Output Voltage, LOW	I _{OL} = max.			0.4	V
SMBus I/O						
V _{SMIH}	Input Voltage, HIGH		2.1			V
V _{SMIL}	Input Voltage, LOW				0.8	V
V _{SMOL}	Output Voltage, LOW	I _{SMOL} = max.			0.4	V
I _{SMOH}	Output Current, HIGH			-0.1	-100	μA
I _{SMOL}	Output Current, LOW				4	mA
Diode Inputs						
I _{DH}	Source Current, High		80	100	120	μA
I _{DL}	Source Current, Low		8	10	12	μA
Analog Output						
V _{AH}	Output Voltage, high	DAC7-0 = 0xFF		2.5		V
V _{AL}	Output Voltage, low	DAC7-0 = 0x00		0		V
I _{AH}	Output Current, source			2		mA
I _{AL}	Output Current, sink			1		mA

Switching Characteristics

Parameter		Conditions	Min	Typ ¹	Max	Unit
Digital Inputs						
t _{DGPI}	Delay, GPI input to register					
t _{THERM}	Delay \overline{THERM} input to register					
t _{NAND}	Delay, NAND input to NTEST_OUT					
Reset Generators						
t _{DVA}	Delay, VCC3AUX < 2.93 V to \overline{AUXRST} output					ns
t _{WVA}	Pulsewidth, \overline{AUXRST} after VCC3AUX > 2.93 V		140		500	ms
t _{DVAR}	Delay, VCC3AUX < 2.93 V to RST\ output					ns

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Parameter		Conditions	Min	Typ ¹	Max	Unit
tDAR	Delay, input AUXRST ↓ to RST\ output					ns
tWAR	Pulsewidth, \overline{RST} after VCC3AUX > 2.93 V or AUXRST ↓		180		500	ms
tDR	Delay, \overline{MR} ↓ to $\overline{RST} = L$					ns
tWR	Pulsewidth, \overline{MR} ↑ to $\overline{RST} = H$		180		500	ms
tDVR	Delay, VCC3 < 2.93 V to \overline{RST} output					ns
tDVW	Pulsewidth, \overline{RST} after VCC3 > 2.93 V		140		500	ms
SMBus Interface						
tDAL	SCL Pulse Width, LOW			4.7		μs
tDAH	SCL Pulse Width, HIGH			4.0		μs
tSTAH	SDA Start Hold Time			4.0		μs
tSTASU	SCL to SDA Setup Time (Stop)			4.0		μs
tSTOSU	SCL to SDA Setup Time (Start)			4.7		μs
tBUFF	SDA Stop Hold Time Setup			4.7		μs
tDSU	SDA to SCL Data Setup Time			250		ns
tDHO	SDA to SCL Data Hold Time			300		ns

Notes:

- ↓ is a H to L transition.
- ↑ is a L to H transition.

System Performance Characteristics

Parameter		Conditions	Min	Typ ¹	Max	Unit
Temperature Channel						
	Remote Accuracy	$-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$		±5		°C
		$+60^{\circ}\text{C} \leq T_A \leq +100^{\circ}\text{C}$		±3		°C
	Ambient Accuracy	$0^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$		±5		°C
		$20^{\circ}\text{C} \leq T_A \leq +50^{\circ}\text{C}$		±3		°C
A/D Converter						
ETUADC	Error, Total Unadjusted			±1		%
ELDADC	Differential Linearity Error			±1		LSB
PSS	Power Supply Sensitivity			±1		%/V
tC	Total Monitoring Cycle Time	Remote and Ambient samples		1.0	1.4	Sec.
D/A Converter Output						
ETUDAC	Error, Total Unadjusted		-3		+3	%
ELDDAC	Differential Linearity Error		-1		+1	LSB
VRES	Threshold Voltage			2.93		V

Notes:

- Values shown in Typ column are typical for VCC3AUX5 = 3.3V and T_A = 25°C.

Application Information

Since the FMS2701 is intended to be embedded on a Pentium motherboard, external connections cannot be specifically defined. Although in Figure 16, only the schematic symbol and power supply connections are shown, there are several guidelines that should be adopted.

Power is supplied to the VCC3AUX pin which should be decoupled to ground through a local 0.1 μ F chip capacitor. To minimize the effects of noise, locate the FMS2701 over a ground plane.

Cleanly route the DIODE \pm analog traces as a pair over the ground plane. Segregate DIODE \pm traces from digital traces and areas of noise. Sensitivity to noise is approximately 1°C/200 μ V.

VCC3 must be maintained at 3.3 volts to avoid tripping the Main Reset Generator. If VCC3 is not used, connect it to VCC3AUX.

Input pin $\overline{\text{MR}}$ and bi-directional pins $\overline{\text{AUXRST}}$ and $\overline{\text{THERM}}$, should be biased to VCC3AUX through a pull-up resistor to prevent spurious triggering.

If unused, GPI should be connected to ground through a pull-down resistor, unless the bit: GPI_INV = H, in which case GPI should be connected to VCC3AUX through a pull-up resistor.

The FAN_SPD/INTESTOUT pin should be biased to ground through a pull-down resistor to ensure that the NAND Test is not inadvertently enabled.

SMBus pins SCL SDA require pull-up resistors along the bus which are not necessarily local to the FMS2701. ADD must be set H, L or open to match the FMS2701 address to the assigned SMBus address.

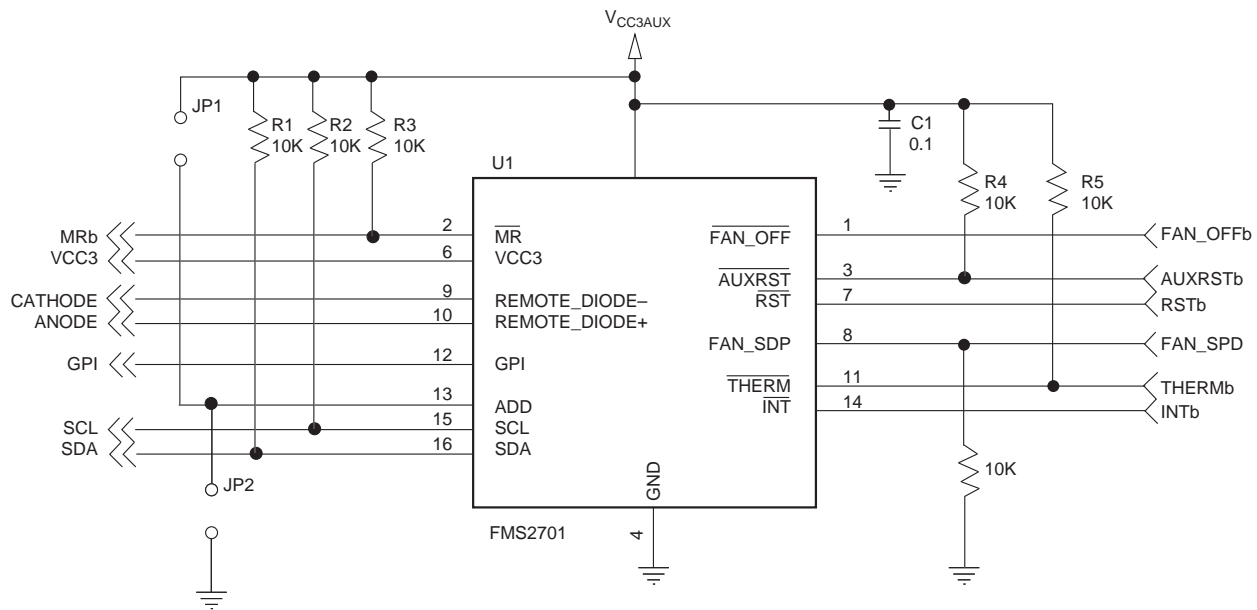


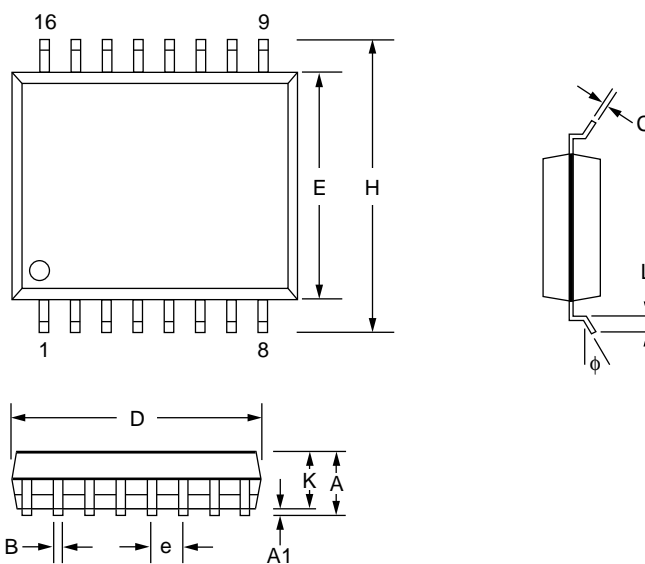
Figure 16. FMS2701 Reference Schematic

Pin Assignments

16-lead QSOP Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.061	.068	1.55	1.73	
A1	.004	.010	0.10	0.25	
B	.008	.012	0.20	0.30	
C	.007	.010	0.18	0.25	
D	.189	.196	4.80	4.98	
E	.150	.157	3.81	3.99	
e	.025 BSC		0.63 BSC		
H	.230	.244	5.84	6.19	
K	-	-	-	-	
L	.016	.035	0.41	0.89	
ϕ	0°	8°	0°	8°	

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Notes

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Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
FMS2701QSC	-40°C to 125°C	Commercial	16 Lead QSOP	2701QS

Preliminary Information

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