FMS2704/FMS2704L

Smart TTV Hardware Monitor

Features

- Six tachometer inputs
- Two analog/PWM fan-speed outputs
- Fan speed controller mode
- Dual remote thermal diode inputs
- Local (on-chip) temperature sense
- Voltage monitoring
- Serial Bus access to internal registers
- Thermal Alarm output
- Maskable Interrupt output
- Status & Configuration registers
- Integrated Reset Generators

Description

The FMS2704 is a Smart Tachometer/ Thermometer/ Voltmeter with a fan speed control mode independent of system management software or BIOS. Outputs are two fan control voltages, $\overline{\text{THERM}}$ alarm and interrupt $\overline{\text{INT}}$.

Tachometer inputs are monitored continuously with speeds compared with internal limits stored in registers. Individual fan speeds can be sensed through the six TACH inputs.

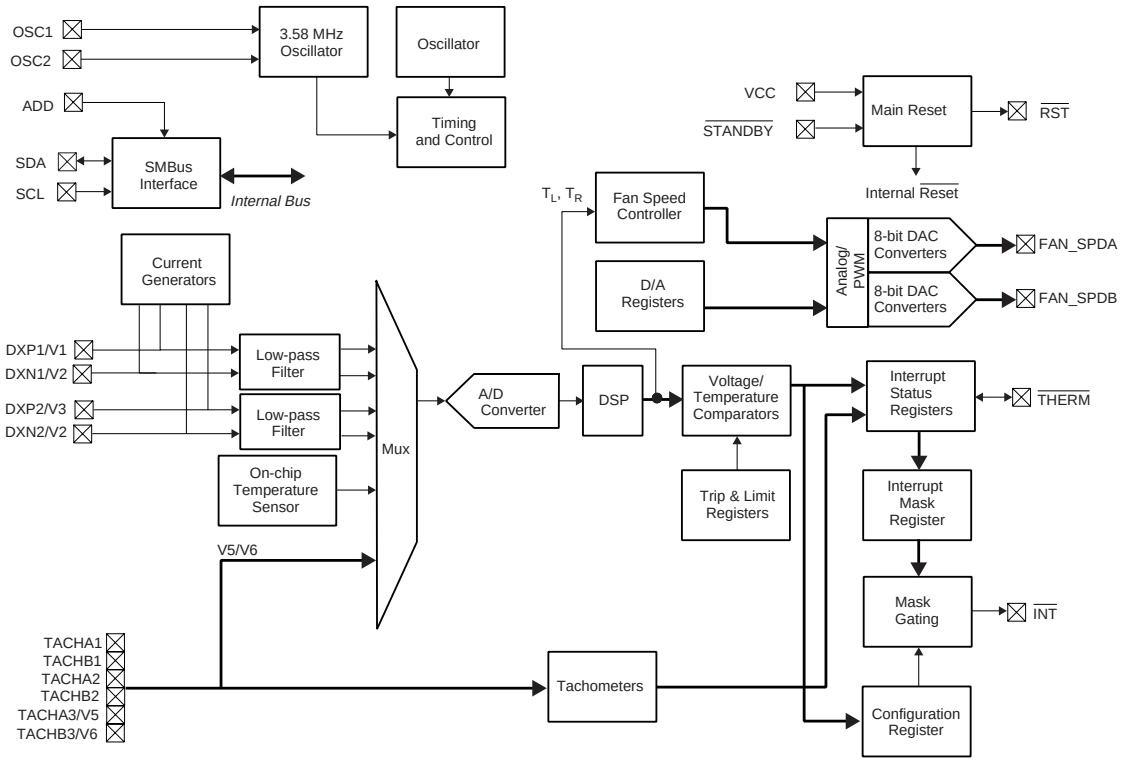
Remote and local diode temperatures are monitored at a 1Hz rate. Diode temperatures are digitized to 1°C resolution prior to storage in remote and local temperature registers. Violations of temperature limits/trip points set interrupt register bits and assert the $\overline{\text{INT}}$ or $\overline{\text{THERM}}$ outputs.

Reset output, $\overline{\text{RST}}$ is asserted if $\overline{\text{STANDBY}}$ = L or VCC ≤ 2.9/2.9/4.4V. Voltages $V_{1\text{-}6}$ can be monitored in place of the diode inputs and tachometer inputs 5 and 6.

Fan noise can be minimized using the Controller Mode to set speed as a function of temperature. Alternatively, external firmware/software can be used to control the fan speed voltages, $FAN\_SPD_{A,B}$.

Supply voltages are 5.0V for the FMS2704 and 3.3V for the FMS2704L. Performance is specified from 0 to 85°C. Package is a 24-lead TSSOP

Block Diagram



Architectural Overview

As a sensor, the FMS2704 has three monitoring functions:

1. Tachometer
2. Thermometer
3. Voltmeter.

Additional functions are:

1. Fan speed controller mode.
2. Programmable dual fan speed outputs.
3. Reset Generator.

Overall operation of the FMS2704 is controlled by the Serial Bus, which sets register values and interrupt masking. Ten of sixteen inputs can be monitored:

1. Two remote thermal diode voltages.
2. Local thermal diode voltage.
3. VCC voltage.
4. Six tachometer, TACH.
5. V_{4-1} voltages instead of external diode inputs.
6. V_{6-5} voltages instead of TACHA3 and TACHB3.

Following comparisons against either preset or programmable thresholds the following hardware outputs are set:

1. Reset, $\overline{RST}$ if VCC is low.
2. $\overline{THERM}$ if a remote or local thermometer trip point violated.
3. Interrupt ($\overline{INT}$), if:
   a) Fan speed is low.
   b) Remote/Local High/Low temperature limit is violated.
   c) Remote diode fault.
   d) V_{6-1} voltage out of tolerance.

Register bits also indicate status:

1. Fan speed error.
2. Remote high/low temperature limit violated.
3. Local high/low temperature limit violated.
4. $\overline{THERM}$ input asserted.
5. Remote diode fault.
6. Voltage error.

Tachometers

Six tachometers monitor fan speed. Stored in each 8-bit tachometer register is the fan speed value expressed in 22.5kHz clock counts per blade revolution. Sensitivity is established by the Tachometer Divisor Register which matches pulse counting to the sensor pulses per revolution.

Each tachometer output is compared against a low speed threshold. A violation will trip the interrupt output to notify System Management software or BIOS that a fault has occurred.

Thermometers

There are three thermometers: two for remote sensing; one for measuring local temperature. All channels utilize the thermal variation of the voltage drop, V_D across a diode, sampled at two currents to derive the diode temperature.

To facilitate tracking of temperatures for controlling fan speed, upper and lower temperature limits can be loaded into the Limit Registers. If a limit is violated, the $\overline{INT}$ output is asserted to indicate that limits must be updated and fan speed changed. A remote diode open or short circuit fault will also assert $\overline{INT}$. All interrupt sources are maskable.

Maximum allowable remote and local temperatures are loaded into the Trip Point registers. If a Trip Point is violated, the $\overline{THERM}$ output is asserted warning that system temperature is too high.

Instead of sensing the change in V_D at one current, which is approximately –2mV/°C, V_D is sampled at two currents (I_{HI} = 100 and I_{LO} = 10µA) to cancel out common error voltages. Difference voltage between the two currents is proportional to absolute temperature:

$$\Delta V_D = \frac{nkT}{q} \bullet 1n\left(\frac{I_{HI}}{I_{LO}}\right)$$

where:

n = PN junction ideality factor, typically 1.0065 for the Pentium II thermal diode.

k = Boltmann's constant, 1.381×10^{-23} J.K^{-1}

T = Absolute temperature, °K

q = Electron charge, 1.602×10^{-19} C

Nominal thermal diode sensitivity is 199.7µV/°C. Diode voltage variation over a –40 to +125°C temperature range, is approximately 300 to 800mV, while the difference voltage variation is approximately 50 to 110mV. Overall sensitivity of the conversion is 1°C/lsb.

Voltmeters

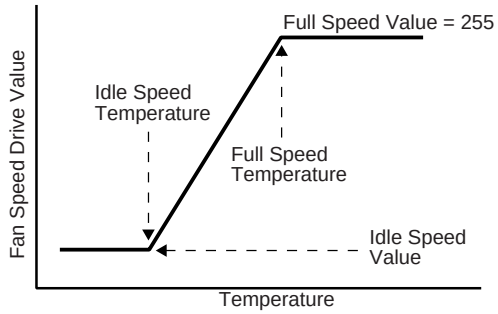
If the TACA3/V_5, TACB3/V_6 or the DX_{2-1}/V_{4-1} inputs are configured to measure voltage, corresponding tachometer or diode registers are disabled. V_{6-1} inputs are sequentially sampled by an Analog Multiplexer, prior to digitization by the A/D Converter with 8-bit accuracy over a 0–1300mV range. Using external voltage dividers, each incoming voltage should be normalized to 1000mV.

Upper and Lower Voltage Thresholds are common to all six voltmeters. If an input violates a threshold, a flag is set in the Voltmeter Configuration Register. A voltage error will cause a maskable interrupt.

Fan Speed Controller

If the FMS2704 is operating in the controller mode, local and/or remote temperatures: T_L, T_{R1} and T_{R2} establish the fan speed drive voltages or PWM output. Fan drive voltage range is 0–2.5V corresponding to 0–255 DAC value.

Overall response to one sensor will be a straight-line segment that is defined by the upper and lower temperatures and the minimum fan speed. Maximum fan speed always corresponds to $SPEED_{7-0}$ = 255.



For each temperature input, a fan speed value is calculated as a function of temperature along a straight line segment preset to match the thermal characteristics of the system environment. The value inserted into the fan speed register is the sum of the responses of the local and two remote diode segments. Updating control points through the Serial Bus can change response.

Remote and Local responses can be set up with different:

1. Idle temperatures.
2. Full speed temperatures.
3. Idle speed values

By varying the balance between these parameters, over limited ranges, either local or remote temperatures can dominate the fan speed. With both remote temperature inputs processed against the same values, fan speed control parameters are established through three groups of six registers. There is one group for each temperature input, while within each group there are four registers containing the following data:

1. $FANLO_{7-0}$, the idle-speed fan-drive value if the temperature is below $TEMPLO_{7-0.}$
2. $TEMPLO_{7-0}$, the threshold for the start of fan drive rising from $RFANLO_{7-0}$ in proportion to temperature minus $TEMPLO_{7-0}$.
3. $TEMPHI_{7-0}$, the limit above which the fan drive will have the value 255.
4. $SLOPE_{7-0}$ the incremental rate of fan speed versus temperature.

Either the analog output from the D/A or the PWM digital output can be selected.

Reset Generators

If VCC ≤ 2.9/4.4V, then $\overline{RST}$ = L and internal reset is active, resetting all internal registers to default values.

If the input $\overline{STANDBY}$ = L, then $\overline{RST}$ = L and the Standby Mode is active with sensing suspended and tachometer, temperatures and voltage register values frozen, while supply current is minimized. Internal reset in not active.

After input VCC > 2.9/4.4V and input, $\overline{STANDBY}$ = H, then $\overline{RST}$ = L for a timeout period of 0.2 seconds.

Serial Interface

Registers are accessed through an I^2C/SMBus compatible Serial Interface located at the address selected by the A address pin.

Registers

Registers setup the monitoring configuration and report status:

Configuration: Establish the mode of operation: Run/standby, Interrupt control, etc.

Status: Report violations of limits or trip points and fault conditions.

Tachometer: Fan speed periods.

Temperature: Local and remote temperatures in °C.

Voltage: Digitized voltage inputs.

Limits: Tachometer, Temperature and Voltage limit and trip point values.

Fan Speed Controller: minimum fan speed, lowest temperature, slope.

Pin Assignments

No.	Name	No.	Name
1.	OSC1	13.	DXP1/V1
2.	OSC2	14.	DXN1/V2
3.	$\overline{RST}$	15.	DXP2/V3
4.	$\overline{THERM}$	16.	DXN2/V4
5.	SDA	17.	TACHA3/V5
6.	SCL	18.	TACHB3/V6
7.	V_{CCD}	19.	V_{CCA}
8.	$\overline{INT}$	20.	TACHB2
9.	ADD	21.	TACHA2
10.	FAN_SPDA	22.	TACHB1
11.	FAN_SPDB	23.	TACHA1
12.	GND	24.	$\overline{STANDBY}$

Pin Descriptions

Pin Name	Pin No.	Type/Value	Pin Function Description
Analog I/O (11)			
DXP1/V1	13	Voltage input/ current source	**External diode input/V1 sense.** **DISXD1 = 0:** Current source to remote thermal diode 1 anode and voltage sense input. **DISXD1 = 1:** V1 voltage sense input (0–1000mV)
DXN1/V2	14	Voltage input/ current sink	**External diode input/V2 sense.** **DISXD1 = 0:** Current sink from remote thermal diode 1 cathode and voltage sense input. **DISXD1 = 1:** V2 voltage sense input (0–1000mV)
DXP2/V3	15	Voltage input/ current source	**External diode input/V3 sense.** **DISXD2 = 0:** Current source to remote thermal diode 1 anode and voltage sense input. **DISXD2 = 1:** V3 voltage sense input (0–1000mV)
DXN2/V4	16	Voltage input/ current sink	**External diode input/V4 sense.** **DISXD2 = 0:** Current sink from remote thermal diode 1 cathode and voltage sense input. **DISXD2 = 1:** V4 voltage sense input (0–1000mV)
TACHA3/V_5	17	Voltage input	**Fan Tachometer 5/V5 sense.** Dual function pin. 10KΩ pull-up **TACH5 = 0:** V5 Voltage input (0–1000mV) **TACH5 = 1:** Tachometer TACA3 Input
TACHB3/V_6	18	Voltage input	**Fan Tachometer 6/V6 sense.** Dual function pin. **TACH6 = 1:** Tachometer TACB3 Input **TACH6 = 0:** V6 Voltage input (0–1000mV)
FAN_SPD$_{A,B}$	10, 11	Analog/Digital output	**Fan A, B speed control.** Analog (± 2mA) or PWM (± 12mA) output programmed from the Fan Speed Configuration Register. Analog output is 0–2.5V. External $\overline{THERM}$ = L forces a 2.5 volt output.
OSC_{2-1}	2, 1	Output/Input	**Oscillator/Clock Inputs.** Connection to 3.58MHz external frequency reference: ceramic resonator across OSC_{2-1} or clock connected to OSC_1.

Pin Descriptions (continued)

Pin Name	Pin No.	Type/Value	Pin Function Description
Serial Port (3)			
SDA	5	Bi-directional	**Data.** Serial Bus data to/from FMS2704
SCL	6	Input	**Clock.** Serial Bus clock into FMS2704
ADD	9	3-level	**Address Select Pins.** Serial Port address select corresponding to H, L and Z levels.
Digital Inputs/Outputs (6)			
TACHB2, TACHA2, TACHB1, TACHA1	20, 21, 22, 23	Input	**Fan Tachometer 4-1 Inputs.** One,two, four or eight pulses per revolution. Three tachometers inputs per bank of fans, A or B. 10KΩ pull-up.
$\overline{\text{THERM}}$	4	I/O (Open drain)	**Thermal Overload.** Output $\overline{\text{THERM}}$ = L indicates that a temperature trip point has been exceeded. Input $\overline{\text{THERM}}$ = L sets the THERM bit in the Interrupt Status Register.
$\overline{\text{INT}}$	8	Open drain	**Interrupt Output.** $\overline{\text{INT}}$ = L when a voltage, temperature limit or temperature trip point is violated and bit 1 of the Configuration Register is set H.
Reset (3)			
$\overline{\text{RST}}$	3	Output	**Reset.** Output from Main Reset Generator, which is tripped by $\overline{\text{STANDBY}}$ = L or VCC < 2.9/4.4 volt.
$\overline{\text{STANDBY}}$	24	Input	**Standby Mode.** Forces the Standby Mode with interrupts disabled and register read backs frozen. Initiates a master reset cycle. Current is minimized by powering down: D/A converters, A/D converters, serial bus ADD detection. The $\overline{\text{STANDBY}}$ pin should biased to VCC through a 20KΩ pull-up resistor.
Power and Ground (2)			
V_{CCD}	7	+3.3/5V	**Digital Supply Voltage.**
V_{CCA}	19	+3.3/5V	**Analog Supply Voltage.**
GND	12	0 V	**Ground.** Return for V_{CC} supply.

Addressable Memory

FMS2704 Memory Map

Name	Address (hex)	POR[7:0] (hex)	
Thermometer			
PTL_{7-0}	0x13	0x46	70°C
PTR_{7-0}	0x14	0x64	100°C
$SPEEDA_{7-0}$	0x16	0x00	
FTL_{7-0}	0x17	0x46	70°C
FTR_{7-0}	0x18	0x64	100°C
$SPEEDB_{7-0}$	0x19	0x00	
$TR2_{7-0}$	0x20	0x16	22°C
$TR1_{7-0}$	0x21	0x15	21°C
TL_{7-0}	0x22	0x14	20°C
$TR2HI_{7-0}$	0x23	0x20	32°C
$TR2LO_{7-0}$	0x24	0x02	02°C

FMS2704 Memory Map (continued)

Name	Address (hex)	POR[7:0] (hex)	
TRAVE, TLAVE	0x29	0x04	Temperature samples averaged
$TRSENS_{13-8}$	0x2A	0x16	5708 + $TROS_8$
$TRSENS_{7-0}$	0x2B	0x4C	5708
$TROS_{7-0}$	0x2C	0xF8	249-1
$TLSENS_{13-8}$	0x2D	0x53	5008 + $TLOS_8$
$TLSENS_{7-0}$	0x2E	0x90	5008
$TLOS_{7-0}$	0x2F	0x08	265-1
$TR1HI_{7-0}$	0x37	0x1F	31°C
$TR1LO_{7-0}$	0x38	0x01	01°C
$TLHI_{7-0}$	0x39	0x1E	30°C
$TLLO_{7-0}$	0x3A	0x00	0°C
Global			
Manufacturer ID	0x3E	0xFC	
Version, Revision	0x3F	0x10	
Configuration	0x40	0x05	
Interrupt Status	0x41	0x00	
Interrupt Mask	0x43	0x00	
Fan Speed Configuration	0x44	0x00	
	0x45		reserved
	0x46		reserved
	0x47		reserved
	0x48		reserved
	0x49		N/A
	0x4A		reserved
	0x4B		reserved
	0x4C		reserved
	0x4D		reserved
	0x4E		reserved
	0x4F		reserved
Tachometer			
	0x50		reserved
$TACA1_{7-0}$	0x51	00	
	0x52		reserved
$TACA2_{7-0}$	0x53	00	
	0x54		reserved
$TACA3_{7-0}$	0x55	0x00	
	0x56		reserved
$TACB1_{7-0}$	0x57	0x00	
	0x58		reserved
$TACB2_{7-0}$	0x59	0x00	
	0x5A		reserved

FMS2704 Memory Map (continued)

Name	Address (hex)	POR[7:0] (hex)	
$TACB3_{7-0}$	0x5B	0x00	
	0x5C		reserved
$TACHTRIPA_{7-0}$	0x5D	0xFF	Bank A speed boundary
	0x5E		reserved
$TACHTRIPB_{7-0}$	0x5F	0xFF	Bank B speed boundary
Tachometer Status	0x60	0x00	
Tachometer Mask	0x61	0x00	
Tachometer Divisor	0x62	0x09	Divide by 2, A and B banks
	0x63	0x3F	Tachometer Configuration
Voltage			
Voltage $V1_{7-0}$	0x70	0x00	
Voltage $V2_{7-0}$	0x71	0x00	
Voltage $V3_{7-0}$	0x72	0x00	
Voltage $V4_{7-0}$	0x73	0x00	
Voltage $V5_{7-0}$	0x74	0x00	
Voltage $V6_{7-0}$	0x75	0x00	
VHI_{7-0}	0x76	0xFF	Voltage High Limit
VLO_{7-0}	0x77	0x00	Voltage Low Limit
Voltmeter Configuration	0x78	0x00	
Voltage Error	0x79	0x00	
Voltage Mask	0c7A	0x00	
VAVE	0x7C	0x01	Voltage samples averaged
$VSENS_{13-8}$	0x7D	0x00	$0 + VOS_8$
$VSENS_{7-0}$	0x7E	0xF0	240
VOS_{7-0}	0x7F	0x00	Zero offset
Controller			
$SPEEDLOA_{7-0}$	0x80	0x00	Controller A low speed
$TLLOA_{7-0}$	0x81	0x00	Controller A local low temp
$SLOPEAL_{7-0}$	0x82	0x00	Controller A local slope
$TRLOA1_{7-0}$	0x83	0x00	Controller A remote low temp 1
$SLOPEA1_{7-0}$	0x84	0x00	Controller A remote slope 1
$TRLOA2_{7-0}$	0x85	0x00	Controller A remote low temp 2
$SLOPEA2_{7-0}$	0x86	0x00	Controller A remote slope 2
$SPEEDLOB_{7-0}$	0x87	0x00	Controller B low speed
$TLLOB_{7-0}$	0x88	0x00	Controller B local low temp
$SLOPEBL_{7-0}$	0x89	0x00	Controller B local slope
$TRLOB1_{7-0}$	0x8A	0x00	Controller B remote low temp 1
$SLOPEB1_{7-0}$	0x8B	0x00	Controller B remote slope 1
$TRLOB2_{7-0}$	0x8C	0x00	Controller B remote low temp 2
$SLOPEB2_{7-0}$	0x8D	0x00	Controller B remote slope 2
Controller Configuration	0x8E	0x00	Fan Speed Controller Modes

Global Register Definitions

Address	Name	Type	Description
0x3E	MFR_{7-0}	R	**Manufacturer ID.** Value is FC.
0x3F	NUM_{7-0}	R	**Version and Revision.** NUM_{7-4} = 1, the FMS2704 version number. NUM_{3-0} = revision number.

Configuration Register (0x40)

BIT#	Name	Type	Description
0	START	R/W	**Start Temperature and Voltage Monitoring.** (Power-up default = 1) **0:** Standby mode. ($\overline{INT}$ is not cleared) **1:** Run. All limit and trip values should be entered into FMS2704 registers prior to setting START = 1.
1	INT_EN	R/W	**Interrupt Enable** **0:** Disabled (Power-up default) **1:** Enables the $\overline{INT}$ output.
2	INT_CLR	R/W	**Interrupt Clear.** (Power-up default = 1) **0:** $\overline{INT}$ output unaffected. **1:** Clears the $\overline{INT}$ output. Contents of the Interrupt Status Register preserved.
3	TRIP_LOCK	R/(W-once)	**Temperature Trip Point Lock. (Power-up default = 0)** **0:** 1. $\overline{THERM}$ limits are the fixed values: FTL_{7-0} and FTR_{7-0}. 2. Writes to programmable registers PTL and PTR are enabled. 3. Writes to A/D Converter Calibration Registers are enabled. **1:** 1. $\overline{THERM}$ limits are the programmable values PTL_{7-0} and PTR_{7-0}, while $\overline{RST}$ = H. 2. Writes to A/D Converter Calibration Registers are inhibited.
4	SOFT_RST	R/W	**Soft Reset.** (Power-up default = 0) **0:** Power-up default restored by SOFT_RST cycle. **1:** Restore power-up values to the Configuration, Interrupt Status, and Interrupt Mask registers.
5			Reserved

Fan Drive Configuration Register (44)

BIT#	Name	Type	Description
0	VOLTA	R/W	**Fan Speed A Analog Voltage Output Enable.** **0:** Disable. **1:** Enable analog voltage output on FAN_SPDA.
1	PWMA	R/W	**Fan Speed A PWM Output Enable.** **0:** Disable. **1:** Enable pulse width modulated output on FAN_SPDA.
2	VOLTB	R/W	**Fan Speed B Analog Output Enable.** **0:** Disable. **1:** Enable analog voltage output on FAN_SPDB.
3	PWMB	R/W	**Fan Speed B PWM Output Enable.** **0:** Disable. **1:** Enable pulse width modulated output on FAN_SPDB.

Fan Drive Configuration Register (44) (continued)

BIT#	Name	Type	Description
4	PWM_INVA		**Fan Speed A PWM Output Invert.** **0:** Mark-space ratio increases with drive. **1:** Mark-space ratio decreases with drive.
5	PWM_INVB		**Fan Speed B PWM Output Invert.** **0:** Mark-space ratio increases with drive. **1:** Mark-space ratio decreases with drive.

Thermometer Register Definitions

Thermometer Value Registers

Address	Name	Type	Description
0x13	PTL_{7-0}	R/W	**Programmable Local Temperature Automatic Trip Point.** If $TA_{7-} > PTL_{7-0}$, then $\overline{THERM}$ = L. Write access is disabled if the TRIP_LOCK bit in the Configuration Register been set. (default: 46_h [70°C])
0x14	PTR_{7-0}	R/W	**Programmable Remote Thermal Diode Automatic Trip Point.** If $TR1_{7-} > PTR_{7-0}$ or $TR2_{7-} > PTR_{7-0}$ then $\overline{THERM}$ = L. Write access is disabled if the TRIP_LOCK bit in the Configuration Register been set. (default: 64_h [100°C])
0x16	$SPEEDA_{7-0}$	R/W	**Fan Speed Register.** Fan speed control value. (default: 00_h)
0x17	FTL_{7-0}	R	**Fixed Local Temperature Automatic Trip Point.** (default: 46_h [70°C])
0x18	FTR_{7-0}	R	**Fixed Remote Thermal Diode Automatic Trip Point.** (default: 64_h [100°C])
0x19	$SPEEDB_{7-0}$	R/W	**Fan Speed Register.** Fan speed control value. (default: 00_h)
0x20	$TR2_{7-0}$	R	**Remote Thermal Diode 2 Temperature.**
0x21	$TR1_{7-0}$	R	**Remote Thermal Diode 1 Temperature.**
0x22	TL_{7-0}	R	**Local Temperature.** Temperature output derived from on-chip thermal diode.
0x23	$TR2HI_{7-0}$	R/W	**Remote Thermal Diode 2 High Temperature Limit.** $TR2_{7-0} > TR2HI_{7-0}$ will set the RTV2 bit in the Interrupt Status Register.
0x24	$TR2LO_{7-0}$	R/W	**Remote Thermal Diode 2 Low Temperature Limit.** $TR2_{7-0} < TR2LO_{7-0}$ will set the RTV2 bit in the Interrupt Status Register.
0x37	$TR1HI_{7-0}$	R/W	**Remote Thermal Diode 1 High Temperature Limit.** $TR1_{7-0} > TR1HI_{7-0}$ will set the RTV1 bit in the Interrupt Status Register.
0x38	$TR1LO_{7-0}$	R/W	**Remote Thermal Diode 1 Low Temperature Limit.** $TR1_{7-0} < TR1LO_{7-0}$ will set the RTV1 bit in the Interrupt Status Register.
0x39	$TLHI_{7-0}$	R/W	**Local Temperature High Temperature Limit.** $TA_{7-0} > TAHI_{7-0}$ will set the ATV and MATV bits in the Interrupt Register.
0x3A	$TLLO_{7-0}$	R/W	**Local Temperature Low Temperature Limit.** $TA_{7-0} < TALO_{7-0}$ will set the ATV and ARTV bits in the Interrupt Register.

Temperature Status Register (0x41)

BIT#	Name	Type	Description
0	LTV	R	**Local Temperature Violation** **0:** On-chip temperature within limits. **1:** On-chip temperature limit violated
1	RTV2	R	**Remote Diode 2 Temperature Violation.** **0:** Remote temperature within limits. **1:** Remote temperature limit violated

Temperature Status Register (0x41) (continued)

BIT#	Name	Type	Description
2	FAULT_D2	R	**Remote Diode 2 Fault.** **0:** Diode functional **1:** Short or open circuit.
4–3		R	Reserved
5	RTV1	R	**Remote Diode 1 Temperature Violation.** **0:** Remote temperature within limits. **1:** Remote temperature limit violated
6	THERM	R	**$\overline{\text{THERM}}$ input status.** **0:** $\overline{\text{THERM}}$ input negated. **1:** $\overline{\text{THERM}}$ input asserted.
7	FAULT_D1	R	**Remote Diode 1 Fault.** **0:** Diode functional **1:** Short or open circuit.

Note: An error that causes continuous interrupts may be concealed using the mask register, until the error can be alleviated.

Temperature Interrupt Mask Register (0x43)

BIT#	Name	Type	Description
0	MASKLTV	R/W	**Mask Local Temperature Violation bit.** **0:** Allow ATV bit to affect $\overline{\text{INT}}$ output. **1:** Prohibit ATV bit from affecting the $\overline{\text{INT}}$ output.
1	MASKRTV2	R/W	**Mask Remote Diode 2 Temperature Violation.** **0:** Allow RTV2 bit to assert $\overline{\text{INT}}$ output. **1:** Prevent RTV2 bit from asserting the $\overline{\text{INT}}$ output.
2	MASKFAULT_D2	R/W	**Mask Remote Diode 2 Fault bit.** **0:** Allow FAULT_D2 bit to assert the $\overline{\text{INT}}$ output. **1:** Prohibit FAULT_D2 bit from asserting the $\overline{\text{INT}}$ output.
3	MASKITHERM	R/W	**Mask Internal THERM.** **0:** Allow ITHERM to affect $\overline{\text{INT}}$ output. **1:** Block ITHERM from affecting the $\overline{\text{INT}}$ output.
4			Reserved
5	MASKRTV1	R/W	**Mask Remote Diode 1 Temperature Violation bit.** **0:** Allow RTV1 bit to assert $\overline{\text{INT}}$ output. **1:** Prevent RTV1 bit from asserting the $\overline{\text{INT}}$ output.
6	MSKTHERM	R/W	**Mask THERM bit.** **0:** Allow THERM bit to affect $\overline{\text{INT}}$ output. **1:** Block THERM bit from affecting the $\overline{\text{INT}}$ output.
7	MASKFAULT_D1	R/W	**Mask Remote Diode 1 Fault bit.** **0:** Allow FAULT_D1 bit to assert the $\overline{\text{INT}}$ output. **1:** Prohibit FAULT_D1 bit from asserting the $\overline{\text{INT}}$ output.

Temperature Samples Averaged Register (0x29)

BIT#	Name	Type	Description
2-0	TRAVE	R/W	**Number of remote samples averaged.** 000 1 001 2 010 4 011 8 100 16 101 32 110 64
5-3	TLAVE	R/W	**Number of local samples averaged.** 000 1 001 2 010 4 011 8 100 16 101 32 110 64

Thermometer Calibration Registers (0x2A–2F)

Register[bit]	Name	Type	Description
0x2A[6]	$TROS_8$	R/W	**Remote Diode A/D Converter Offset MSB.** MSB of a 9-bit number that offsets the remote temperature by TR_{OS} °C. Default = 0 (TR_{OS} = 249-1) Range = 0 to 255.
0x2A[5:0]	$TRSENS_{13-8}$	R/W	**Remote Diode A/D Converter Sensitivity HI.** Upper six bits of the A/D sensitivity (lsbs/volt) value programmed into the Voltage Counter Limit Register. Default = 0x16 (TR_{SENS} = 5708). Range 0 to 16383.
0x2B	$TRSENS_{7-0}$	R/W	**Remote Diode A/D Converter Sensitivity LO.** Lower eight bits of the A/D sensitivity (lsbs/volt) value programmed into the Voltage Counter Limit Register. Default = 0x4C (TR_{SENS} = 5708) Range 0 to 16383.
0x2C	$TROS_{7-0}$	R/W	**Remote Diode A/D Converter Offset LO.** Lower eight bits of a 9-bit number that offsets the remote temperature by TR_{OS} °C. Default = 0xF8 (TR_{OS} = 249-1) Range = 0 to 511.
0x2D[6]	$TLOS_8$	R/W	**Local Diode A/D Converter Offset MSB.** MSB of a 9-bit number that offsets the remote temperature by TL_{OS} °C. Default = 1 (TL_{OS} = 265-1) Range = 0 to 511.
0x2D[5:0]	$TLSENS_{13-8}$	R/W	**Local Diode A/D Converter Sensitivity HI.** Upper six bits of the A/D sensitivity (lsbs/volt) value programmed into the Voltage Counter Limit Register. Default = 0x13 (TL_{SENS} = 5008) Range 0 to 16383.
0x2E	$TLSENS_{7-0}$	R/W	**Local Diode A/D Converter Sensitivity LO.** Lower eight bits of the A/D sensitivity (lsbs/volt) value programmed into the Voltage Counter Limit Register. Default = 0x90 (TL_{SENS} = 5008) Range 0 to 16383.
0x2F	$TLOS_{7-0}$	R/W	**Local Diode A/D Converter Offset LO.** Lower eight bits of a 9-bit number that offsets the local temperature by TL_{OS} °C. Default = 0x08 (N_{OS} = 265-1) Range = 0 to 511.

Tachometer Register Definitions

Tachometer Value Registers

Address	Name	Type	Description
0x51	$TACA1_{7-0}$	R	**Fan Bank A Tachometer 1 Speed LSB.**
0x53	$TACA2_{7-0}$	R	**Fan Bank A Tachometer 2 Speed LSB.**
0x55	$TACB3_{7-0}$	R	**Fan Bank A Tachometer 3 Speed LSB.**
0x57	$TACB1L_{7-0}$	R	**Fan Bank B Tachometer 1 Speed LSB.**
0x59	$TACB2_{7-0}$	R	**Fan Bank B Tachometer 2 Speed LSB.**
0x5B	$TACB3_{7-0}$	R	**Fan Bank B Tachometer 3 Speed LSB.**
0x5D	$TACHTRIPA_{7-0}$	R/W	**Tachometer speed boundary A LSB**
0x5F	$TACHTRIPB_{7-0}$	R/W	**Tachometer speed boundary B LSB**

Tachometer Status Register (0x60)

BIT#	Name	Type	Description
0	ERROR_TA1	R	**Bank A Fan 1 speed status.** **0:** Speed within TACHTRIPA register boundary. **1:** Speed violates TACHTRIPA register boundary.
1	ERROR_TA2	R	**Bank A Fan 2 speed status.** **0:** Speed within TACHTRIPA register boundary. **1:** Speed violates TACHTRIPA register value.
2	ERROR_TA3	R	**Bank A Fan 3 speed status.** **0:** Speed within TACHTRIPA register boundary. **1:** Speed violates TACHTRIPA register value.
3	ERROR_TB1	R	**Bank B Fan 1 speed status.** **0:** Speed within TACHTRIPB register boundary. **1:** Speed violates TACHTRIPB register value.
4	ERROR_TB2	R	**Bank B Fan 2 speed status.** **0:** Speed within TACHTRIPB register boundary. **1:** Speed violates TACHTRIPB register value.
5	ERROR_TB3	R	**Bank B Fan 3 speed status.** **0**: Speed within TACHTRIPB register boundary. **1:** Speed violates TACHTRIPB register value.
7–6			

Tachometer Status Mask Register (0x61)

BIT#	Name	Type	Description
0	MASKA1	R	**Mask Bank A Fan 1 speed status.** **0:** Allow A1LO bit to assert $\overline{INT}$ output. **1:** Prevent A1LO bit from asserting $\overline{INT}$ output.
1	MASKA2	R	**Mask Bank A FAN 2 speed status.** **0:** Allow A2LO bit to assert $\overline{INT}$ output. **1:** Prevent A2LO bit from asserting $\overline{INT}$ output.
2	MASKA3	R	**Mask Bank A FAN 3 speed status.** **0:** Allow A3LO bit to assert $\overline{INT}$ output. **1:** Prevent A2LO bit from asserting $\overline{INT}$ output.

Tachometer Status Mask Register (0x61) (continued)

BIT#	Name	Type	Description
3	MASKB1	R	**Mask Bank B FAN 1 speed status.** **0:** Allow B1LO bit to assert $\overline{INT}$ output. **1:** Prevent B1LO bit from asserting $\overline{INT}$ output.
4	MASKB2	R	**Mask Bank B FAN 2 speed status.** **0:** Allow B2LO bit to assert $\overline{INT}$ output. **1:** Prevent B2LO bit from asserting $\overline{INT}$ output.
5	MASKB3	R	**Mask Bank B FAN 3 speed status.** **0:** Allow B2LO bit to assert $\overline{INT}$ output. **1:** Prevent B2LO bit from asserting $\overline{INT}$ output.
7–6			Reserved

Tachometer Divisor Register (0x62)

BIT#	Name	Type	Description
2–0	ADIV	R/W	**Bank A Divisor.** **000:** Divide tachometer input rate by 1. **001:** 2 **010:** 4 **011:** 8 **100:** 16 **101:** 32
5–3	BDIV	R/W	**Bank B Divisor.** **000:** Divide tachometer input rate by 1. **001:** 2 **010:** 4 **011:** 8 **100:** 16 **101:** 32
7–6			Reserved

Tachometer Configuration Register (0x63)

BIT#	Name	Type	Description
0	ENA1	R/W	**Enable Bank A Fan 1 Tachometer.** **0:** Standby. **1:** Run.
1	ENA2	R/W	**Enable Bank A Fan 2 Tachometer.** **0:** Standby. **1:** Run.
2	ENA3	R/W	**Enable Bank A Fan 3 Tachometer.** **0:** Standby. **1:** Run.
3	ENB1	R/W	**Enable Bank B Fan 1 Tachometer.** **0:** Standby. **1:** Run.
4	ENB2	R/W	**Enable Bank B Fan 2 Tachometer.** **0:** Standby. **1:** Run.

Tachometer Configuration Register (0x63) (continued)

BIT#	Name	Type	Description
5	ENB3	R/W	**Enable Bank B Fan 3 Tachometer.** **0:** Standby. **1:** Run.
7–6			Reserved

Voltmeter Register Definitions

Voltmeter Value Registers

Address	Name	Type	Description
0x70	$V1_{7-0}$	R	**Voltage Value V1.** 200 == 1000mV input.
0x71	$V2_{7-0}$	R	**Voltage Value V2.** 200 == 1000mV input.
0x72	$V3_{7-0}$	R	**Voltage Value V3.** 200 == 1000mV input.
0x73	$V4_{7-0}$	R	**Voltage Value V4.** 200 == 1000mV input.
0x74	$V5_{7-0}$	R	**Voltage Value V5.** 200 == 1000mV input.
0x75	$V6_{7-0}$	R	**Voltage Value V6.** 200 == 1000mV input.
0x76	VHI_{7-0}	R/W	**High Voltage Trip Level.** Common to V_{6-1}
0x77	VLO_{7-0}	R/W	**Low Voltage Trip Level.** Common to V_{6-1}
0x7D	$VSENS_{15-8}$	R/W	**Voltmeter Sensitivity HI.** (Default = 0)
0x7E	$VSENS_{7-0}$	R/W	**Voltmeter Sensitivity LO.** (Default = 240)
0x7F	VOS_{7-0}	R/W	**Voltmeter Offset.** (Default = 0)

Voltmeter Configuration Register (0x78)

BIT#	Name	Type	Description
0	V12D1	R	**DXP1/V1 and DXN1/V2 Configuration.** **0:** Thermometer inputs DXP1 and DXN1 **1:** Voltmeter inputs V1 and V2.
1	V34D2	R	**DXP2/V2 and DXN3/V4 Configuration.** **0:** Thermometer inputs DXP2 and DXN2 **1:** Voltmeter inputs V3 and V4.
2	V5TACHA3	R/W	**Tachometer A3/Voltage 5 input configuration.** **0:** Tachometer A3 input. **1:** Voltmeter V5 input.
3	V6TACHB3	R/W	**Tachometer B3/Voltage 6 input configuration.** **0:** Tachometer B3 input. **1:** Voltmeter V6 input.
7-4	-	-	-

Voltage Error Register (0x79)

BIT#	Name	Type	Description
0	ERROR_V1	R	**Voltage 1 Error.** **0:** V1 within tolerance. **1:** V1 out of tolerance.
1	ERROR_V2	R	**Voltage 2 Error.** **0:** V2 within tolerance. **1:** V2 out of tolerance.
2	ERROR_V3	R	**Voltage 3 Error.** **0:** V3 within tolerance. **1:** V3 out of tolerance.
3	ERROR_V4	R	**Voltage 4 Error.** **0:** V4 within tolerance. **1:** V4 out of tolerance.
4	ERROR_V5	R	**Voltage 5 Error.** **0:** V5 within tolerance. **1:** V5 out of tolerance.
5	ERROR_V6	R	**Voltage 6 Error.** **0:** V6 within tolerance. **1:** V6 out of tolerance.
6	-		
7	-		

Voltage Error Mask Register (7A)

BIT#	Name	Type	Description
0	MASKV1ERR	R/W	**Mask Voltage 1 Error.** **0**: Allow V1ERR bit to assert $\overline{\text{INT}}$ output. **1:** Prevent V1ERR bit from asserting $\overline{\text{INT}}$ output.
1	MASKV2ERR	R/W	**Mask Voltage 2 Error.** **0:** Allow V2ERR bit to assert $\overline{\text{INT}}$ output. **1:** Prevent V2ERR bit from asserting $\overline{\text{INT}}$ output.
2	MASKV3ERR	R/W	**Mask Voltage 3 Error.** **0:** Allow V3ERR bit to assert $\overline{\text{INT}}$ output. **1:** Prevent V3ERR bit from asserting $\overline{\text{INT}}$ output.
3	MASKV4ERR	R/W	**Mask Voltage 4 Error.** **0:** Allow V4ERR bit to assert $\overline{\text{INT}}$ output. **1:** Prevent V4ERR bit from asserting $\overline{\text{INT}}$ output.
4	MASKV5ERR	R/W	**Mask Voltage 5 Error.** **0:** Allow V5ERR bit to assert $\overline{\text{INT}}$ output. **1:** Prevent V5ERR bit from asserting $\overline{\text{INT}}$ output.
5	MASKV6ERR	R/W	**Mask Voltage 6 Error.** **0:** Allow V6ERR bit to assert $\overline{\text{INT}}$ output. **1:** Prevent V6ERR bit from asserting $\overline{\text{INT}}$ output.
6	-		
7	-		

Voltage Samples Averaged Register (0x7C)

BIT#	Name	Type	Description
2-0	VAVE	R/W	**Number of voltage samples averaged.** 000 1 001 2 010 4 011 8 100 16 101 32 110 64
7-3			

Voltmeter Calibration Registers (0x7D–7F)

Register[bit]	Name	Type	Description
0x7D[6]	VOS_8	R/W	**Voltmeter Offset Polarity.** Polarity of VOS_{7-0} **0:** Positive. **1:** Negative. Default = 0.
0x7D[5:0]	$VSENS_{13-8}$	R/W	**Voltmeter Sensitivity HI.** Upper six bits of the A/D converter sensitivity (LSB/volt) value programmed into the Voltage Counter Limit Register. Default = 0x0 (TR_{SENS} = 240). Range 0 to 16383.
0x7E	$VSENS_{7-0}$	R/W	**Voltmeter Sensitivity LO.** Lower eight bits of the A/D converter sensitivity (LSB/volt) value programmed into the Voltage Counter Limit Register. Default = 0xF0 (TR_{SENS} = 240) for 5mV/LSB. Range 0 to 16383.
0x7F	VOS_{7-0}	R/W	**Voltmeter Offset Magnitude.** An 8-bit number that offsets the Voltage ADC output by V_{OS} LSBs with polarity determined by VOS_8. Default = 0x00 (V_{OS} = 0) Range = 0 to 255.

Controller Register Definitions

Controller Value Registers

Address	Name	Type	Description
0x80	$SPEEDLOA_{7-0}$	R/W	**Controller A low speed**
0x81	$TLLOA_{7-0}$	R/W	**Controller A local low temp**
0x82	$SLOPEAL_{7-0}$	R/W	**Controller A local slope.** (integer + fraction)
0x83	$TRLOA1_{7-0}$	R/W	**Controller A remote low temp 1**
0x84	$SLOPEA1_{7-0}$	R/W	**Controller A remote slope 1.** (integer + fraction)
0x85	$TRLOA2_{7-0}$	R/W	**Controller A remote low temp 2**
0x86	$SLOPEA2_{7-0}$	R/W	**Controller A remote slope 2.** (integer + fraction)
0x87	$SPEEDLOB_{7-0}$	R/W	**Controller B low speed**
0x88	$TLLOB_{7-0}$	R/W	**Controller B local low temp**
0x89	$SLOPEBL_{7-0}$	R/W	**Controller B local slope.** (integer + fraction)
0x8A	$TRLOB1_{7-0}$	R/W	**Controller B remote low temp 1**
0x8B	$SLOPEB1_{7-0}$	R/W	**Controller B remote slope 1.** (integer + fraction)
0x8C	$TRLOB2_{7-0}$	R/W	**Controller B remote low temp 2**
0x8D	$SLOPEB2_{7-0}$	R/W	**Controller B remote slope 2.** (integer + fraction)

Note: All controller register values must be postitive.

Fan Speed Controller Configuration Register (8E)

BIT#	Name	Type	Description
0	FAN_CTRL	R/W	**Fan Speed Control Enable.** (Power up default =0) **0:** Fan speed outputs set through SERIAL BUS (Power up default) **1:** Fan speed outputs depend on local/remote diode temperatures.
1	TLA_CTRL	R/W	**Local Diode Fan Speed A Control Enable.** **0:** Fan speed outputs established by other thermal diode inputs. **1:** Fan speed outputs depend on local thermal diode temperature and any other enabled thermal diode input.
2	TRA1_CTRL	R/W	**Remote Diode 1 Fan Speed A Control Enable.** **0:** Fan speed outputs established by other thermal diode inputs. **1:** Fan speed outputs depend on remote thermal diode 1 temperature and any other enabled thermal diode input.
3	TRA2_CTRL	R/W	**Remote Diode 2 Fan Speed A Control Enable.** **0:** Fan speed outputs established by other thermal diode inputs. **1:** Fan speed outputs depend on remote thermal diode 2 temperature and any other enabled thermal diode input.
4	TLB_CTRL	R/W	**Local Diode Fan Speed B Control Enable.** **0:** Fan speed outputs established by other thermal diode inputs. **1:** Fan speed outputs depend on local thermal diode temperature and any other enabled thermal diode input.
5	TRB1_CTRL	R/W	**Remote Diode 1 Fan Speed B Control Enable.** **0:** Fan speed outputs established by other thermal diode inputs. **1:** Fan speed outputs depend on remote thermal diode 1 temperature and any other enabled thermal diode input.
6	TRB2_CTRL	R/W	**Remote Diode 2 Fan Speed B Control Enable.** **0:** Fan speed outputs established by other thermal diode inputs. **1:** Fan speed outputs depend on remote thermal diode 2 temperature and any other enabled thermal diode input.

Functional Description

Within the FMS2704, there are six major functional blocks:

1. Tachometers
2. Temperature Processor.
3. Voltage Monitor
4. Data Processor
5. Fan Speed Controller
6. Reset Generators

Tachometers

There are six tachometers, three for each of the two banks of fans. Tachometers are enabled through the Tachometer Configuration Register.

Each TACH input can be programmed to accept fan rotation pulses at one, two, four or eight pulses per revolution. Tachometer output is an 8-bit value indicating the period of one fan revolution:

$$TAC = \frac{225000 \bullet 60}{RPM \bullet DIV}$$

To accommodate slow rise and fall times, edge filtering is inserted at each tachometer input. Open drain/collector outputs are accommodated by pulling up each TACH input with a 10 KΩ resistor.

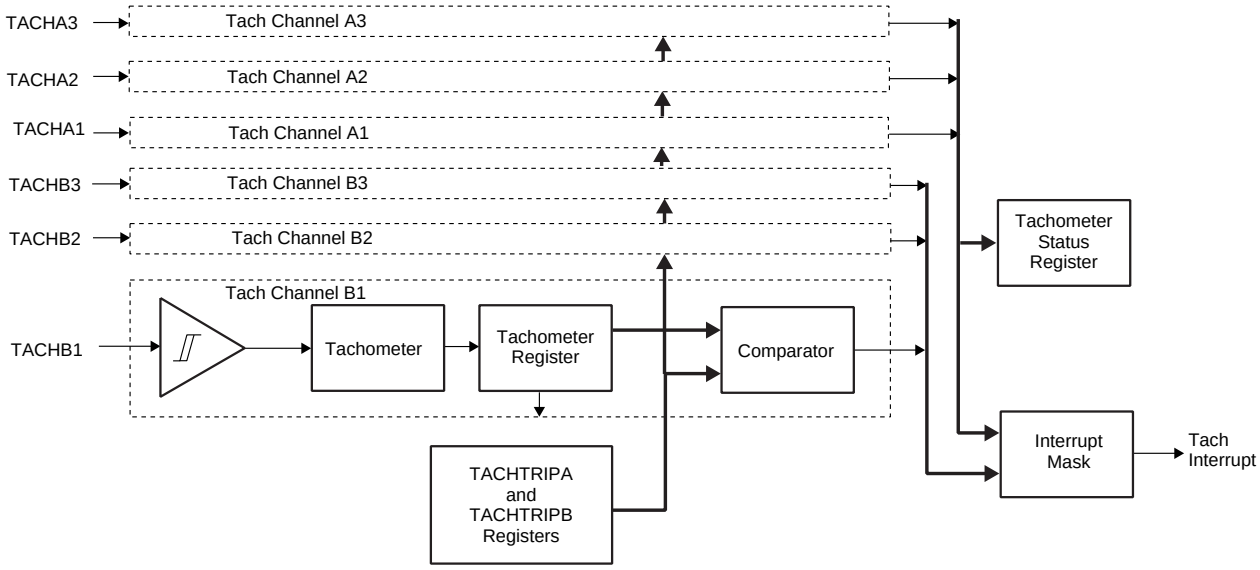


Figure 1. Tachometry

Each tachometer output is compared against a programmable threshold.

1. TACHTRIPA for bank A tachometers
2. TACHTRIPB for bank B tachometers

Threshold Period is set at a fraction (e.g. 110%) of nominal, a level below which airflow may be diminished.

An Error Flag will be set in the Tachometer Status Register under either of the following conditions:

$TAC_{A1\text{-}A3} > TACHTRIP_A$

$TAC_{B1\text{-}B3} > TACHTRIP_B$

If a violation occurs, an interrupt is generated ($\overline{INT}$ =L) to inform BIOS or System Management software that fan registers should be read. After servicing the interrupt, the source can be masked to prevent further interrupts.

Thermometers

Remote and local thermal diode voltages are sensed by the Temperature Processor which sequentially outputs values of the remote and local temperatures. Inputs are derived from a remote diode that is connected by two wires to the input of the processor; and the local diode, which is located on-chip. Output is supplied to the Data Processor which loads the $TL_{7\text{-}0}$ and $TR_{7\text{-}0}$ registers with the digitized local and remote temperatures.

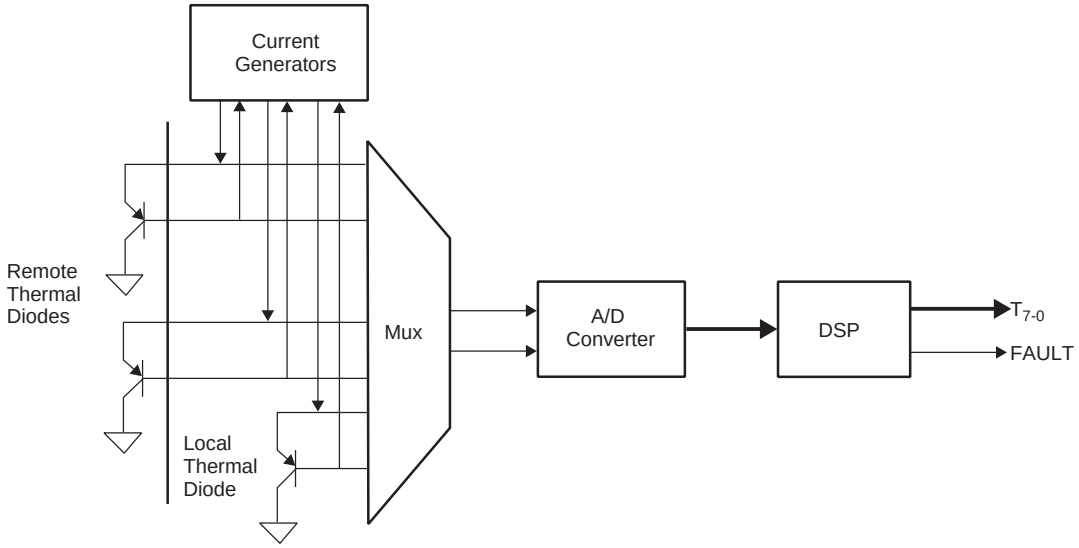


Figure 2. Temperature Processor Block Diagram

A differential multiplexer selects the thermal diode input voltage to be applied to the A/D converter and the bandgap used for the A/D calibration cycle. Voltage of the diode is sensed at two currents:10 and 100µA. During the diode sampling interval, the A/D converter digitizes low and high current samples. DSP averages and subtracts the samples to output an 8-bit temperature that is updated a rate greater than 1Hz. Remote and Local diode temperatures are outputted alternately on the T_{7-0} bus which is connected to the Temperature Registers.

Remote Diode fault sensing is included within the DSP block. If either remote diode voltage indicates either a short or an open circuit, the appropriate FAULT_D1 or FAULT_D2 bit is set in the Interrupt Status Register.

Temperature data format is 8-bit, two's complement with the LSB equivalent to 1.0°C. Range and conversion between °C and equivalent binary and hexadecimal data is exemplified in Table 1.

Table 1. Temperature/Data Conversion/Format

Temperature	Digital Output	
	Binary	Hex
+125°C	0111 1101	0x7D
+25°C	0001 1001	0x19
+1.0°C	0000 0001	0x01
0°C	0000 0000	0x00
-1.0°C	1111 1111	0xFF
-25°C	1110 0111	0xE7
-55°C	1100 1001	0xC9

A block diagram of the processing shared by the thermometer channels is shown in Figure 3.

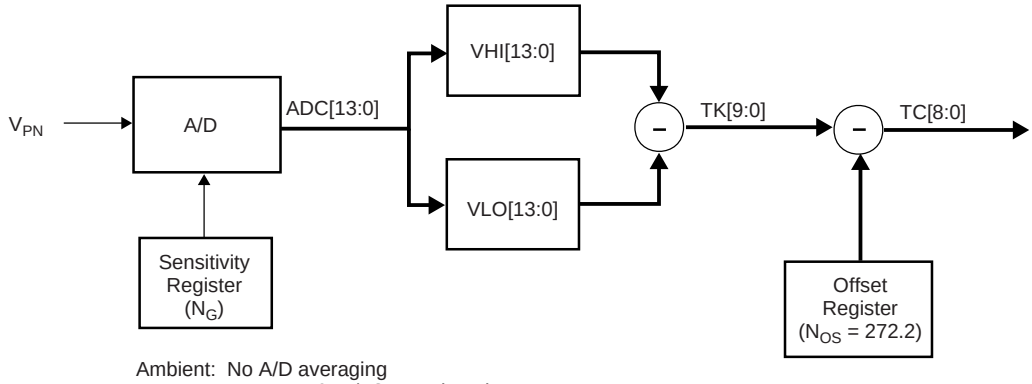


Figure 3. Temperature Processor Architecture

Default response of the Temperature Processor is set to match the expected characteristics of the Intel Pentium thermal diode and the on-chip local diode. By updating the values in the TRSENS, TRSO, TLSENS and TLOS registers sensitivity can be trimmed to accommodate alternate thermal diode characteristics.

Diode low current voltage value V_{LO} is subtracted from the high current value V_{HI} to yield $T_K = \Delta V_D$. T_K is the digitized temperature in °K with a sensitivity of $^1/_2$ °/lsb.

Next, the value 273.2 is subtracted to transform T_K from °K to °C. Diode offsets are trimmed out by adjusting the value of N_{OS}. T_C is truncated to 8-bits prior to storage in the temperature registers.

To minimize the effects of noise, digitized temperatures are averaged over several samples.

$\overline{\text{THERM}}$ Processing

$\overline{\text{THERM}}$ is a bi-directional pin with an open drain output. When the $\overline{\text{THERM}}$ output is asserted L, the $\overline{\text{THERM}}$ input is disabled.

Local temperatures are compared against:

1. $TLHI_{7-0}$ and $TLLO_{7-0}$ values stored in the Limit Registers which bracket the temperature range to be tracked. If a limit is violated, $\overline{\text{INT}}$ = L.
2. Thermal trip points PTL_{7-0} or FTL_{7-0} set at high levels corresponding to a serious overheating problem.

Remote temperatures, TR1 and TR2 are compared against:

1. $TR1HI_{7-0}$, $TR1LO_{7-0}$ $TR2HI_{7-0}$ and $TR2LO_{7-0}$ values stored in the Limit Registers which bracket the temperature range to be tracked. If a limit is violated, $\overline{\text{INT}}$ = L.
2. Thermal Trip points FTR_{7-0} or PTR_{7-0}. If TR_{7-0} > FTR_{7-0} or PTR_{7-0}, the alert output THERM = asserted. Following a violation, the sensed temperature must drop 5°C to clear the trip flag.

Figure 4 depicts the logical flow of the internal and external $\overline{\text{THERM}}$ signals, showing the origins and destinations.

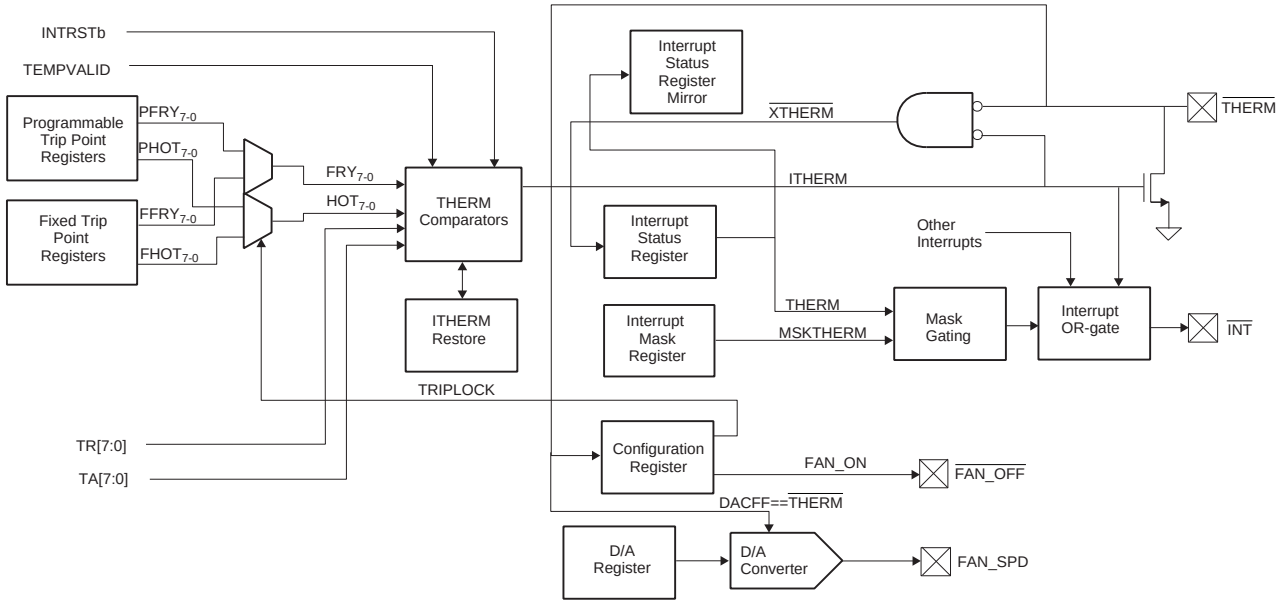


Figure 4. $\overline{\text{THERM}}$ I/O Structure/Detail

As an input, if $\overline{\text{THERM}}$ = L the following events occur:

1. If the mask bit, MSKTHERM = L, output pin, $\overline{\text{INT}}$ = L
2. Configuration Register bit, $\overline{\text{FAN\_OFF}}$ = H.
3. Output pins, $FAN\_SPD_{A,B}$ = 2.5V for maximum fan speed, with register values $SPEEDA_{7-0}$ and $SPEEDB_{7-0}$ unchanged.
4. Interrupt Status Register bit, THERM = H.
5. Interrupt Status Register Mirror bit, MTHERM = H.

As an output, ITHERM = H, causes $\overline{\text{THERM}}$ = L; ITHERM = L, causes $\overline{\text{THERM}}$ = Z, open drain. ITHERM = H, if any of the following conditions occur:

1. If Configuration Register bit, TRIPLOCK = L:
   a) $TL_{7-0} > FTL_{7-0}$.
   b) $TR1_{7-0} > FTR_{7-0}$.
   c) $TR2_{7-0} > FTR_{7-0}$.

2. If Configuration Register bit, TRIPLOCK = H

   a) $TL_{7-0} > PTL_{7-0}$.

   b) $TR1_{7-0} > PTR_{7-0}$.

   c) $TR2_{7-0} > PTR_{7-0}$.

A typical THERM sequence is shown in Figure 5, which depicts the profile of events when TR1 transitions through the PTR trip point threshold. Similar profiles apply to:

1. TR1 with FTR limits
2. TR2 with PTR and FTR trip points
3. and to TL and TR2 with the appr

TRIPLOCK is Temperature Trip Point Lock bit in the Configuration Register. After a Trip Point has been exceeded, to restore the open drain output, $\overline{THERM}$ = Z, the temperature must fall 5°C below the trip point.

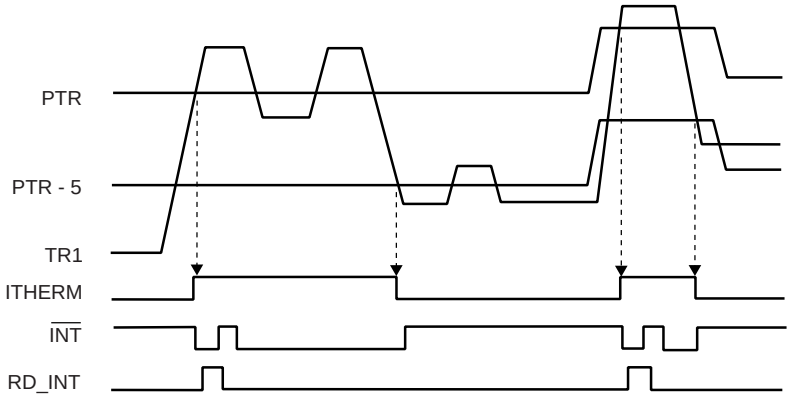


Figure 5. Profile of THERM Driven Events

Voltage Monitoring

In the voltmeter mode, either diode input can become a pair of single-ended voltage inputs. A low pass filter in each input minimizes fluctuations caused by noise riding on the input signals. Voltmeter inputs are optimized for conversion of a nominal 1000mV signal that is converted with a sensitivity of 0.2 lsb/mV.

Voltmeter data format is 8-bit integer. Table 2 shows register values corresponding to selected inputs. By setting the value of VAVE, the number of samples to be averaged can be set to be either 1, 2, 4, 8, 16, 32 or 64.

Table 2. Voltage Conversion

Input (mV)	Voltage Value	
	Decimal	Hex
0	0	0
100	20	14
500	100	64
900	180	B4
1000	200	C8
1100	220	DC
1275	255	FF

One set of high and low limit values, VHI_{7-0} and VLO_{7-0} are shared between the six voltage values. Violation of a limit will set the corresponding flag in the Voltage Error Register. Flag i is set as a result of either of the following conditions:

1. $V_i < V_{LO}$
2. $V_i > V_{HI}$

Where i = 1:6.

If the flag is not masked by the Voltage Error Mask Register, the Interrupt Output, $\overline{INT}$ = L. After the source of the error has been identified, further interrupts can be prevented by masking the source of the error.

Interrupt Processing

$\overline{INT}$ is a hardware interrupt output. $\overline{INT}$ operation is controlled by the Configuration Register bits: INT_EN and INT_CLR bits, which enable and clear the open drain $\overline{INT}$ output. Subject to the setting of the Mask Registers, $\overline{INT}$ =L, if any bit is active in the following registers:

1. Tachometer Status.
2. Voltage Status Register.
3. Temperature Status Register.

Otherwise $\overline{INT}$ = Z, open drain. Figure 6 depicts the logical flow of the interrupt sources to the $\overline{INT}$ output.

For the Tachometer Status Register, if any one of the six fan speed inputs violates the speed boundary, the appropriate $ERROR_{A1-3,B1-3}$ bit is set. Unused tachometer inputs can be disabled by programming in the Tachometer Configuration Register. Unwanted interrupts can be masked by programming the Tachometer Mask Register.

Voltage Status Register bits indicate if any one of the six voltmeter inputs violates the high or low voltage trip levels boundary, causing the appropriate $ERROR\_V_{6-1}$ bit to be set. Unwanted interrupts can be masked by programming the Voltmeter Mask Register.

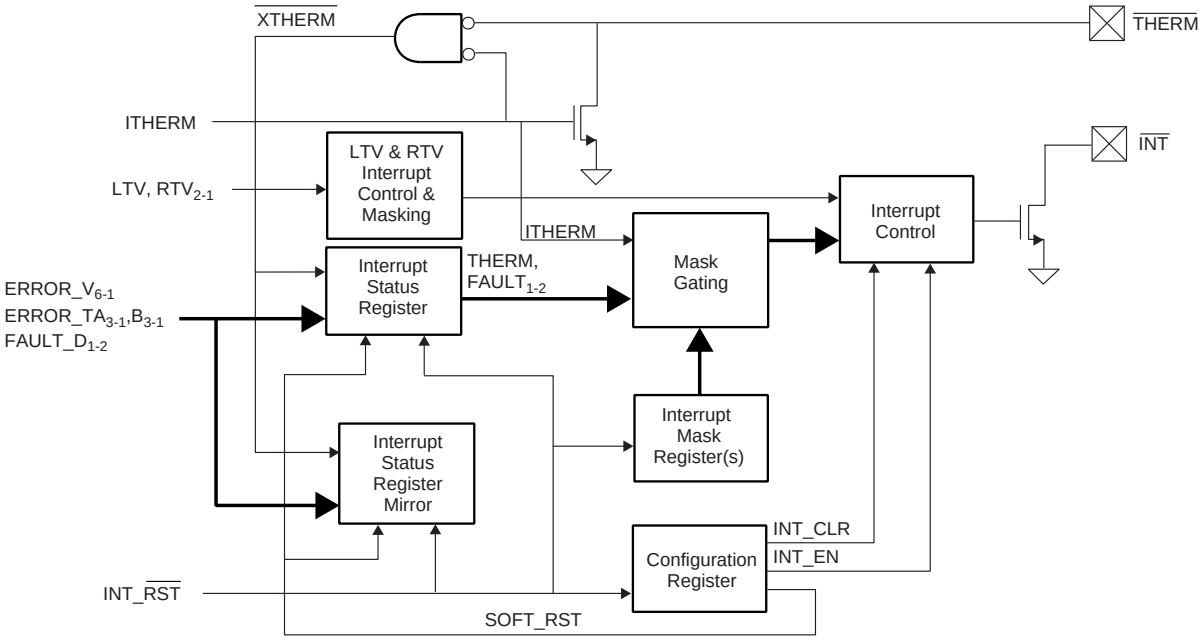


Figure 6. $\overline{INT}$ Output Structure

With Configuration Register bits INT_EN = 1 and INT_CLR = 0, output pin $\overline{INT}$ = L, if any of the following bits are set in the Temperature Interrupt Register:

1. LTV: An local temperature limit is violated indicating that the on-chip temperature falls outside the boundaries established by $TLLO_{7-0}$ and $TLHI_{7-0}$.
2. RTV1: Remote thermal diode 1 temperature limit is violated, indicating that the temperature falls outside the boundaries established by $TRLO_{7-0}$ and $TRHI_{7-0}$.
3. RTV2: Remote thermal diode 2 temperature limit is violated, indicating that the temperature falls outside the boundaries established by $TRLO_{7-0}$ and $TRHI_{7-0}$.
4. THERM: Temperature exceeds an selected automatic trip point (PTL_{7-0}, PTR_{7-0}, FTL_{7-0}, or FTR_{7-0}) causing output $\overline{THERM}$ = L or the $\overline{THERM}$ input = L *even if the THERM bit in the Interrupt Register is masked*.
5. $FAULT\_D_{1-2}$: Remote diode D_{1-2} is either open or short circuit.

Output pin $\overline{INT}$ = Z, clearing the interrupt output, if any of the following events occur:

1. Interrupt Status Register is read, causing this register to be cleared to the default state that is all interrupts cleared. However a THERM or $FAULT_{1-2}$ condition will cause an immediate re-assertion of the interrupt.
2. Configuration Register bit INT_CLR = 1, which is the default condition following an internal reset.
3. Configuration Register bit INT_EN = 0, which is the default condition following an internal reset.

Status of the INT_CLR and INT_EN bits does not impact the contents of the Interrupt Status. Reading the Interrupt Status Registers clears only that register.

Note that setting the $\overline{INT}$ output by exceeding a temperature limit is an edge-driven event. Only when the temperature actually crosses the limit boundary does $\overline{INT}$ transition LOW. An example of interrupts caused by a series of temperature, T transitions across temperature limits is shown in Figure 7.

Temperature limits are fixed for the first series of temperature excursions. Then, for the second series, following the T_{HI1} violation, the T_{HI} limit is raised from T_{HI1} to T_{HI2}. If T_{HI} is reprogrammed from a value above T to a value below T_{HI}, then an interrupt is generated.

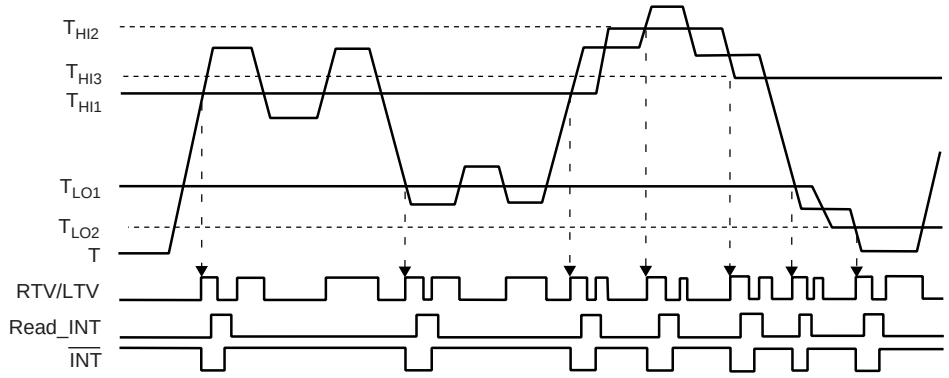


Figure 7. Profile of Temperature Driven Interrupts

LTV and RTV bits operate in conjunction with the $\overline{INT}$ output and Interrupt Status Register as follows:

1. When the temperature exceeds a high limit, the corresponding Interrupt Status Register bit, either LTV or RTV is set.
2. Reading the Interrupt Status Register clears LTV and RTV.
3. Once the high limit has been exceeded, a subsequent transitions through the high level will not cause an interrupt, unless:
   a) The temperature passes through the low limit.
   b) Or, the high temperature limit is changed.
4. If the high temperature limit is changed from a level above the temperature to a level below, then the relevant Interrupt Status Register bit, either LTV or RTV is set.
5. If the temperature falls below a low limit, the corresponding Interrupt Status Register bit, either LTV or RTV is set.
6. Once the low limit has been exceeded, a subsequent transitions through the low level will not cause an interrupt, unless:
   a) The temperature passes through the high limit.
   b) Or, the low temperature limit is changed.

If the low temperature limit is changed from a level below the ambient/remote temperature to a level above, then the LTV/RTV bit is set.

Serial Interface

FMS2704 register access is via a 2-wire I^2C/SMBus compatible interface. Base address is 0x2C + n, where n is an offset defined by the state of the ADD pin: Z, H, L == 0, 1, 2. (see Table 3) State Z corresponds to the ADD pin being open circuit.

Table 3. Serial Port Slave Addresses

ADD	Address
Z	2C
H	2D
L	2E

Two signals comprise the bus: clock (SCL) and bi-directional data (SDA). When receiving and transmitting data through the serial interface, the FMS2704 acts as a slave, responding only to commands by the I^2C/SMBus master.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA may change only when SCL = L. An SDA transition while SCL = H is interpreted as a start or stop signal.

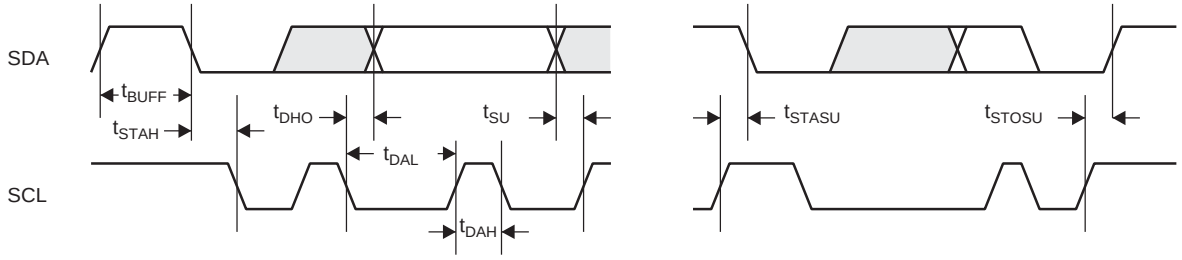


Figure 8. Serial Bus: Read/Write Timing

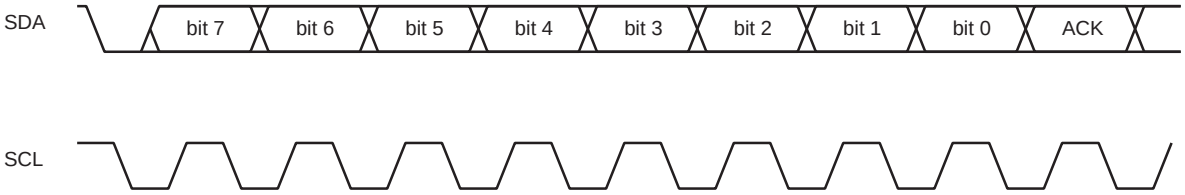


Figure 9. Serial Bus: Typical Byte Transfer

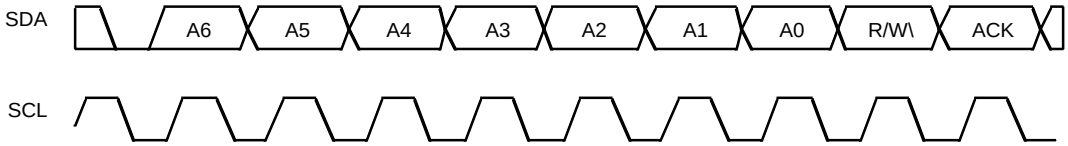


Figure 10. Serial Bus: Slave Address with Read/$\overline{\text{Write}}$ Bit

There are five steps within an I^2C/SMBus cycle:

1. Start signal
2. Slave address byte
3. Pointer register address byte
4. Data byte to read or write
5. Stop signal

When the Serial Bus interface is inactive (SCL = H and SDA = H) communications are initiated by sending a start signal. The start signal (Figure 8, left waveform) is a HIGH-to-LOW transition on SDA while SCL is HIGH. This signal alerts all slaved devices that a data transfer sequence is imminent.

After a start signal, the first eight bits of data that are transferred, comprise a seven bit slave address followed a single R/W bit (Read = H, Write = L). As shown in Figure 9, the R/W bit indicates the direction of data transfer: read from; or write to the slave device. If the transmitted slave address matches the address of the FMS2704 which set by the state of the ADD pin, the FMS2704 acknowledges by pulling SDA LOW on the 9th SCL pulse (see Figure 10). If the addresses do not match, the FMS2704 does not acknowledge.

For each byte of data read or written, the MSB is the first bit of the sequence.

Data Transfer Via Serial Interface

If a slave device, such as the FMS2704 does not acknowledge the master device during a write sequence, SDA remains HIGH so the master can generate a stop signal. During a read sequence, if the master device does not acknowledge (ACK = L), the FMS2704 interprets this as “end of data.” SDA remains HIGH so the master can generate a stop signal.

To write data to a specific FMS2704 control register, three bytes are sent:

1. Write the slave address byte with bit R/$\overline{\text{W}}$ = L.
2. Write the pointer byte.
3. Write to the control register indexed by the pointer.

Data is read from the control registers of the FMS2704 in a similar manner, except that two data transfer operations are required:

4. Write the slave address byte with bit R/$\overline{\text{W}}$ = L.
5. Write the pointer byte.
6. Write the slave address byte with bit R/$\overline{\text{W}}$ = H
7. Read the control register indexed by the pointer.

Preceding each slave write, there must be a start cycle. Following the pointer byte there should be a stop cycle. After the last read, there must be a stop cycle comprising a LOW-to-HIGH transition of SDA while SCL is HIGH. (see Figure 8, right waveform)

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

Serial Interface Read/Write Examples

Examples below show how serial bus cycles can be linked together for multiple register read and write access cycles. For sequential register accesses, each ACK handshake initiates further SCL clock cycles from the master to transfer the next data byte.

Write to one control register

1. Start signal
2. Slave Address byte (R/$\overline{W}$ bit = LOW)
3. Pointer byte
4. Data byte to base address
5. Stop signal

Read from one control register

1. Start signal
2. Slave Address byte (R/$\overline{W}$ bit = LOW)
3. Pointer byte (= base address)
4. Stop signal
5. Start signal
6. Slave Address byte (R/$\overline{W}$ bit = HIGH)
7. Data byte from base address
8. Stop signal

Registers

Based upon setup commands via the Serial Bus, the FMS2704 gathers sensor inputs from the Tachometers, Thermometers and Voltmeters. Measured values are compared against reference values stored in the Trip and Limit registers. Fault conditions set flags in the Interrupt registers and activate $\overline{THERM}$ and $\overline{INT}$ outputs. Sensor and interrupt status are passed to the host via the Serial Bus interface. Host commands set the FMS2704 configuration, interrupt masking and the fan speed.

Following power-up, registers are set to default values. After a 200 msec. power up reset delay, the FMS2704 will begin checking sensor inputs to determine if the temperature in voltages fall within default limits, which can be overridden by changing the values stored in the Value RAM.

If the PTL_{7-0} and PTR_{7-0} values are changed, then the TRIP_LOCK (Temperature Trip Point Lock) bit in the Configuration Register must be set to enable temperature values to be compared against the programmable rather than the fixed trip point values. If the temperature limit values are changed, then the changes are effective immediately. Interrupt masking (register 0x43), enabling (INT_EN bit) and clearing (INT_CLR bit) can be used to disable interrupts during register setup.

Register functions and bit assignments defined in the *Addressable Memory* and *Global Register Definitions* sections.

Temperature register outputs, TR_{7-0} and TA_{7-0} are compared with the limit values $TRHI_{7-0}$, $TRLO_{7-0}$, $TAHI_{7-0}$ and $TALO_{7-0}$ that are stored in the Limit Registers. Out of range TA_{7-0} and TR_{7-0} values set the INT bit in the Interrupt Status Register. TR_{7-0} and TA_{7-0} are also compared with the values in Trip Point Registers, PTL_{7-0} and PTR_{7-0} if these registers have been loaded or FTL_{7-0} and FTR_{7-0}, which contain power up default values.

Fan Speed Outputs

Fan speed outputs FAN_SPDA and FAN_SPDB can be programmed individually to be either 0–2.5V analog output or Pulse Width Modulated Output. Register values are set directly through the Serial Bus by external software or firmware following interrogation to temperature and tachometer values. Also, the fan speed may be derived from the internal registers, SPEEDA and SPEEDB or from the Channel A or Channel B Fan Speed Controllers.

If the A Channel analog output is selected, the output of the ADAC D/A converter is connected to the FAN_SPDA output. If A Channel PWM is selected, then Pulse Width Modulator is connected to the FAN_SPDA output. B channel analog/PWM selection functions similarly.

Reset Generator

The Reset Generator emits a $\overline{RST}$ = L pulse under either of the following conditions:

1. $\overline{STANDBY}$ = L, causing no internal reset, $\overline{INTRST}$.
2. VCCA & VCCD < 4.4V (FMS2704) or
   VCCA & VCCD < 2.9V (FMS2704L),

Following release of the reset stimulus, $\overline{RST}$ = L for a further 200 msec.

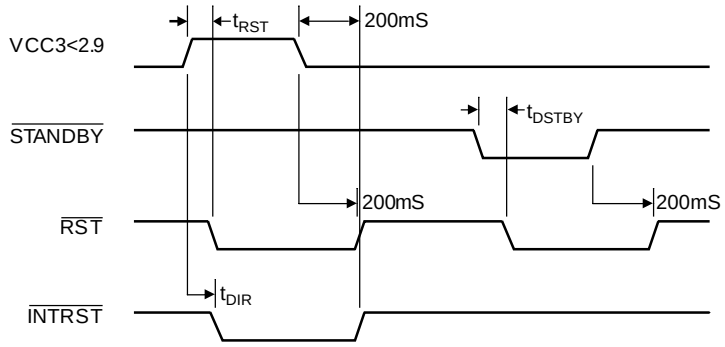


Figure 11. Reset Generator Waveforms

In the standby mode power is minimized by stopping all sensing activities and freezing the tachometer, temperature and voltage register values. When power is initially applied, the Reset Generator instigates five events through internal reset, INTRST:

1. Configuration, Interrupt and Mask registers are reset to default values.
2. THERM Trip Point registers: PTL_{7-0}, PTR_{7-0}, FTL_{7-0}, FTR_{7-0} are set to default values.
3. $SPEEDA_{7-0}$ and $SPEEDB_{7-0}$ registers are set to 0x00.
4. Temperature Processor and Data Processor are reset.
5. Fan Speed Controller is disengaged with output set to zero.

Fan Speed Controllers

If the FAN_CTRL bit is set H, D/A converter fan drive voltages are established as a function of FMS2704 sensor inputs. If the FAN_CTRL bit is set L, the Controller does not influence the D/A register values, which are set through the Serial Bus. There are two identical channels, A and B that can be set up independently to control the A and B fan banks. Figure 12 shows both controllers and the details of the A controller.

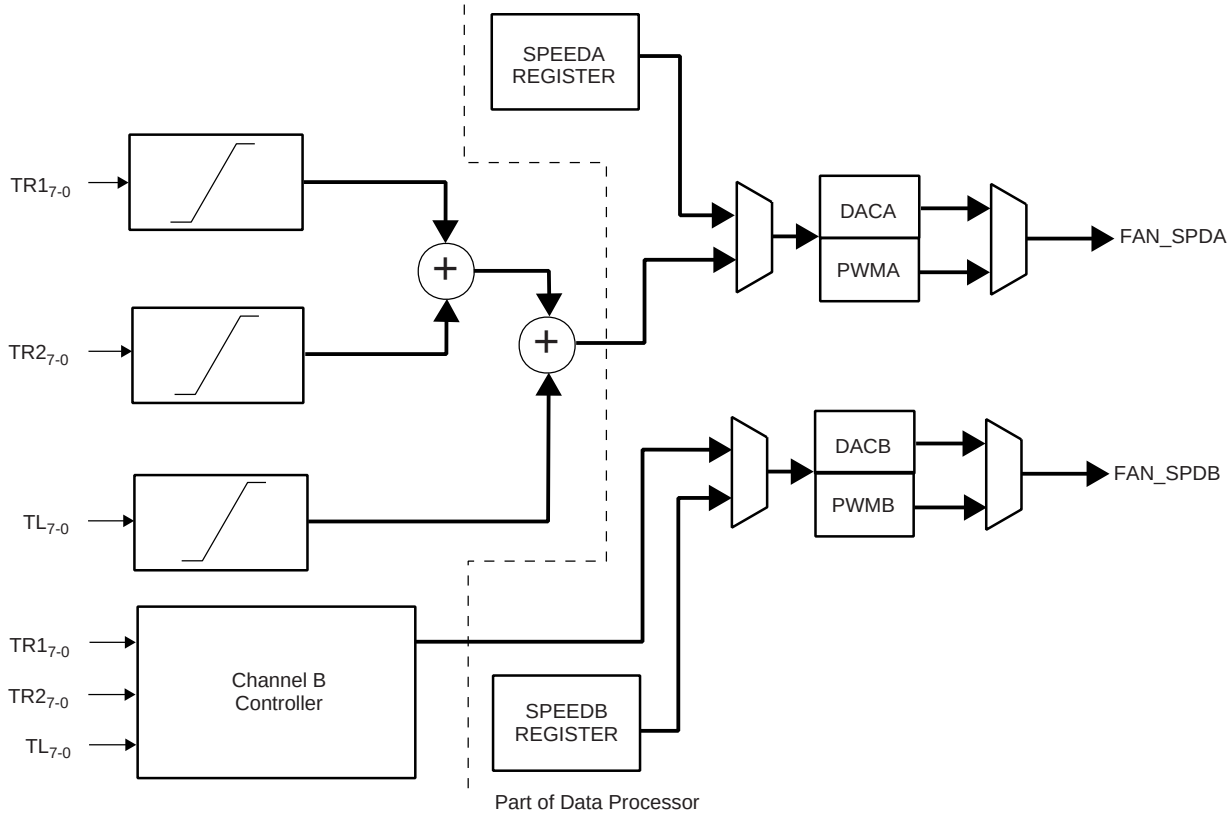


Figure 12. Fan Speed Controller

Fan control is based upon running the fans at slow speed for minimum noise, unless the local temperature rises due to a higher ambient temperature or a remote temperature rises because a CPU is running hot. If remote or local diode temperature rises, then the fan speed is increased. Fan drive is controlled on the basis of:

1. Remote temperatures 1 and 2 (CPU temperatures).
2. Local temperature (FMS2704 die temperature).

A straightforward mode of operation is to control fan speed as a function of one CPU temperature. Another mode is to base primary control upon local temperature, which is sensed to anticipate the extra cooling required to compensate for higher ambient temperature surrounding the enclosure. Secondary control augments cooling by increasing fan speed if the temperature of either CPU begins to rise. If a fan runs low or fails, the fan speed within that bank is automatically increased, while an interrupt is generated to inform the CPU that a fan speed has fallen below threshold.

For each thermometer channel, a piece-wise linear approximation response like that shown in Figure 13 is defined.

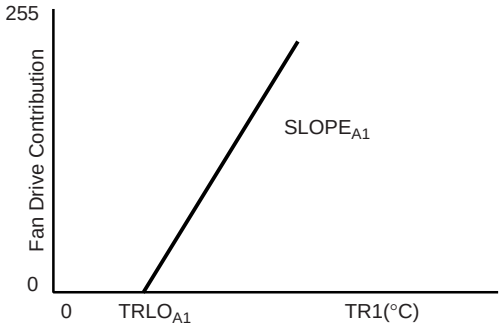


Figure 13. Fan Drive Response

This straight-line segment defines the value to be added to the Channel A fan speed drive for a given temperature. For example setting $TRLO_{A1}$ = 60 and $SLOPE_{A1}$ = 4D hex to define fan speed drive increment of 9.5 lsbs/°C, above 60°C. Below 60°C, the contribution is zero.

To account for multiple temperature inputs, separate segments are defined for the local and remote temperatures. Drive contributions from these segments are added to a minimum fan speed to create a target drive value.

Channel A drive is:

$$DRIVEA = SPEEDLOA + SLOPEAL \cdot (T_L - TLLOA) + SLOPEA1 \cdot (T_{R1} - TRLOA1) + SLOPEA2 \cdot (T_{R2} - TRLOA2)$$

where:

T_L = Local temperature.

T_{R1} = Remote temperature of diode 1.

T_{R2} = Remote temperature of diode 2.

And logic within the FMS2704 applies the following constraints:

$DRIVEA \le 255$

$T_L > TLLOA$

$SLOPEAL*(T_L - TLLO_A) \le 255$

$T_{R1} > TRLOA1$

$SLOPEA1*(T_{R1} - TR_{A1}) \le 255$

$T_{R2} > TRLOA2$

$SLOPEA2*(T_{R2} - TR_{A2}) \le 255$

Channel B drive is:

$$DRIVEB = SPEEDLOB + SLOPEBL \cdot (T_L - TLLOB) + SLOPEB1 \cdot (T_{R1} - TRLOB1) + SLOPEB2 \cdot (T_{R2} - TLLOB2)$$

Essentially, the overall response amounts to summing individual fan speed contributions that have different gains and offsets.

An example with channel A fan drive caused solely by remote diode 1 is shown in Figure 14, which is the result of adding the remote diode 1 segment to minimum fan speed. Using the values from the segment example, if $SPEEDLO_A$ = 16, the SPEED drive rises from 16 at 60°C to a 255 limit at 78°C.

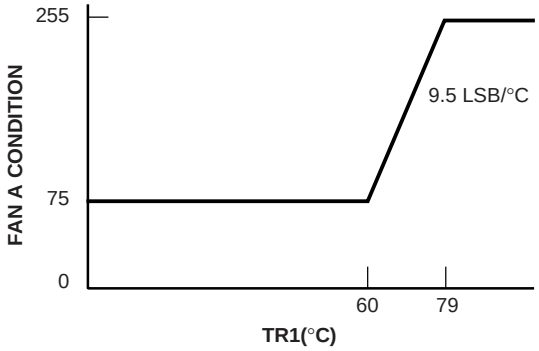


Figure 14. Fan Speed Response

With both remote temperature inputs processed against the same values, fan speed control parameters are established through a set of fourteen registers:

1. $SPEEDLO_A$, $TRLO_{A1}$, $SLOPE_{A1}$, $TRLO_{A2}$, $SLOPE_{A2}$, $TRLO_{AL}$, $SLOPE_{AL}$.
2. $SPEEDLO_B$, $TRLO_{B1}$, $SLOPE_{B1}$, $TRLO_{B2}$, $SLOPE_{B2}$, $TRLO_{B2}$, $SLOPE_{BL}$.

In the slave mode, FAN_SPDA and FAN_SPDB outputs are derived from the SPEEDA and SPEEDB registers.

Format of the values in the registers is as follows:

$SPEEDLO_{A,B}$ is expressed in LSBs of fan drive output. Range is 0–255 corresponding to 0–2.5V DAC output or 0–100% PWM on the $FANSPD_{A,B}$ outputs.

TRLOA1, TRLOA2, TRLOB1 and TRLOB2 must be unsigned integer °C values.

$SLOPE_{AL,BL,A1-2,B1-2}$ is expressed as a 5-bit integer plus a fraction. $SLOPE_{7-3}$ is the integer. $SLOPE_{2-0}$ is the fraction in 1/8'th degrees. For example, the slope 13.5 is coded as 6C ($SLOPE_{7-3}$ = 13, $SLOPE_{2-0}$ = $^1/_2$).

A typical Fan Speed Controller register set up is shown in Table 4.

Table 4. Example Controller Register Values

Register	Address	Decimal	Hex
SPEEDALO	80	96	60
SLOPEAL	82	0	00
TRLOA1	83	60	3C
SLOPEA1	84	64	40
SLOPEA2	86	0	00
FAN_CTRL	8E	5	05
VOLTA	44	1	01

With these register values, Fan Controller A is selected with an analog voltage output (rather than PWM). Below 60°C, the fan idles at 38% (96/255) maximum speed. Above 60°C, fan drive increases at 8 LSB/°C (0.3%/°C) until the fan drive is 255 at 80°C.

Since $SLOPE_{AL}$ and $SLOPE_{A2}$ values are zero, neither local temperature, T_L nor remote diode 2 temperature, T_{R2} impact the value of drive A, which is a solely dependant upon temperature TR1.

Equivalent Circuits

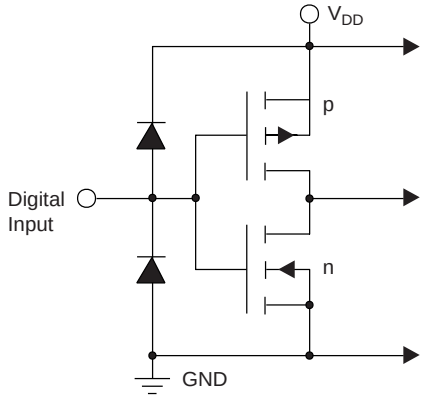


Figure 15. Equivalent Digital Input Circuit

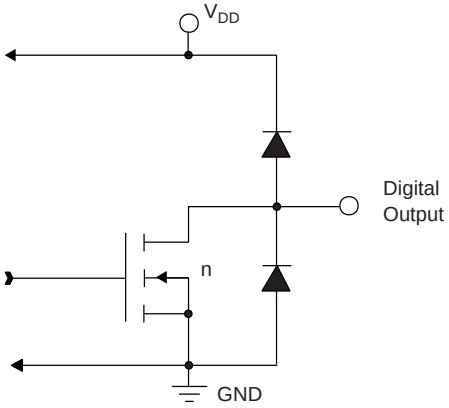


Figure 18. Equivalent Open Drain Output Circuit

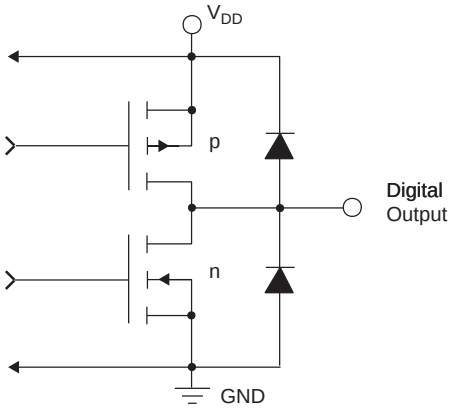


Figure 16. Equivalent Digital and D/A Output Circuit

Figure 19. Equivalent D/A Output Circuit

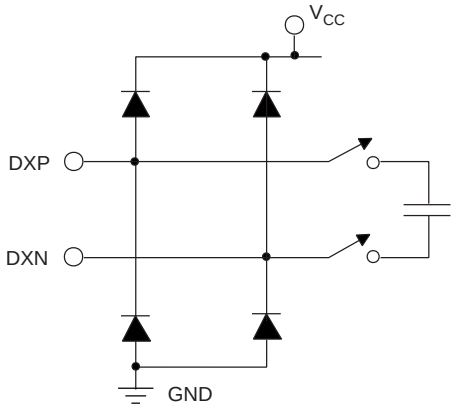


Figure 17. Equivalent Remote Diode Interface Circuit

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Unit
Power Supply Voltages				
V_{CC} (Measured to GND)	-0.5	3.3/5.0	5.75	V
Digital Inputs				
3.3/5.0V logic applied voltage (Measured to GND)[2]	-0.3		5.75	V
Forced current[3, 4]	-5.0		5.0	mA
Analog Inputs				
Applied Voltage (Measured to GND)[2]	-0.5		5.75	V
Forced current[3, 4]	-10.0		10.0	mA
Digital Outputs				
Applied voltage (Measured to GND)[2]	-0.5		5.75	V

Parameter	Min	Typ	Max	Unit
Forced current[3, 4]	-6.0		6.0	mA
Forced current[3, 4]	-8.0		8.0	mA
Short circuit duration (single output in HIGH state to ground)			1	second
Temperature				
Operating, Ambient	-40		125	°C
Junction			150	°C
Lead Soldering (10 seconds)			300	°C
Vapor Phase Soldering (1 minute)			220	°C
Storage	-65		150	°C
Electrostatic Discharge[5]			±150	V

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.
5. EIAJ test method.

Operating Conditions

Parameter		Min	Nom	Max	Units
V_{CC}	Digital Power Supply Voltage		3.3/5.0		V
T_A	Ambient Temperature, Still Air	0		85	°C

Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
Power Supply Currents						
I_{VCC}	Supply Current	Operating Standby		15	20	mA
		$TACH_{A1-3, B1-3}$ Active		10		mA
		Standby, $TACH_{A1-3, B1-3}$ = H		7		mA
Digital Inputs/Outputs						
C_I	Input Capacitance			5	10	pF
C_O	Output Capacitance			10		pF
I_{IH}	Input Current, HIGH		-1	0.005		µA
I_{IL}	Input Current, LOW			0.005	+1	µA
I_{ILR}	Input Current, LOW, Master Reset	$\overline{STANDBY}$ = L		200	+1	µA
V_{IH}	Input Voltage, HIGH		2.0			V
V_{IL}	Input Voltage, LOW				0.8	V
I_{OZH}	Output Current, HIGH, open drain			-0.1	100	µA
I_{OH}	Output Current, HIGH				-2	µA
I_{OL}	Output Current, LOW				3	mA
V_{OH}	Output Voltage, HIGH	I_{OH} = max.	2.4			V
V_{OL}	Output Voltage, LOW (V_{DD3})	I_{OL} = max.			0.4	V
Serial Bus I/O						
V_{SMIH}	Input Voltage, HIGH		2.1			V
V_{SMIL}	Input Voltage, LOW				0.8	V
V_{SMOL}	Output Voltage, LOW	I_{SMOL} = max.			0.4	V
I_{SMOH}	Output Current, HIGH			-0.1	-100	µA
I_{SMOL}	Output Current, HIGH				4	mA
Diode Inputs						
I_{DH}	Source Current, High		80	100	120	µA
I_{DL}	Source Current, Low		8	10	12	µA
Analog Output						
V_{AH}	Output Voltage, high	$SPEEDA/B_{7-0}$ = 0xFF		2.5		V
V_{AL}	Output Voltage, low	$SPEEDA/B_{7-0}$ = 0x00		0		V
I_{AH}	Output Current , source			2		mA
I_{AL}	Output Current , sink			1		mA

Switching Characteristics

Parameter		Conditions	Min	Typ[1]	Max	Unit
Digital Inputs						
t_{DI}	Delay, input to register					
Reset Generators						
t_{DR}	Delay, $\overline{STANDBY}$ ↓ to $\overline{RST}$ = L					ns
t_{WR}	Pulsewidth, $\overline{STANDBY}$ ↑ to $\overline{RST}$ = H		180		500	ms
t_{DVR}	Delay, V_{CC} < 2.9/4.4 V to $\overline{RST}$ output					ns
t_{DVW}	Pulsewidth, $\overline{RST}$ after V_{CC} > 2.9/4.4 V		140		500	ms
Serial Bus Interface						
t_{DAL}	SCL Pulse Width, LOW			4.7		µs
t_{DAH}	SCL Pulse Width, HIGH			4.0		µs
t_{STAH}	SDA Start Hold Time			4.0		µs
t_{STASU}	SCL to SDA Setup Time (Stop)			4.0		µs
t_{STOSU}	SCL to SDA Setup Time (Start)			4.7		µs
t_{BUFF}	SDA Stop Hold Time Setup			4.7		µs
t_{DSU}	SDA to SCL Data Setup Time			250		ns
t_{DHO}	SDA to SCL Data Hold Time			300		ns

Notes:
1. ↓ is a H to L transition.
2. ↑ is a L to H transition.

System Performance Characteristics

Parameter		Conditions	Min	Typ[1]	Max	Unit
Thermometer						
	Remote Accuracy	-40°C ≤ T_R ≤+125°C		±5		°C
		+60°C ≤ T_R ≤ +100°C		±3		°C
	Local Accuracy	0°C ≤ T_A ≤ +85°C		±5		°C
		20°C ≤ T_A ≤ +50°C		±3		°C
Tachometer						
	Accuracy			±1		%
Voltmeter						
	Accuracy			±1		%
	Resolution			8		bits
A/D Converter						
E_{TUADC}	Error, Total Unadjusted			±1		%
E_{LDADC}	Differential Linearity Error			±1		LSB
PSS	Power Supply Sensitivity			±1		%/V
t_C	Total Monitoring Cycle Time	Remote and Local		1.0	1.4	Sec.
D/A Converter Output						
E_{TUDAC}	Error, Total Unadjusted		-3		+3	%
E_{LDDAC}	Differential Linearity Error		-1		+1	LSB

System Performance Characteristics (continued)

Parameter		Conditions	Min	Typ[1]	Max	Unit
Reset Generators						
V_{RES}	Threshold Voltage	FMS2704		4.4		V
		FMS2704L		2.9		V
t_{RES}	Reset Interval			200		msec.

Notes:
1. Unless stated otherwise, values shown in Typ. column are typical for V_{CC} = 3.3/5.0V and T_A = 25°C.

Applications Information

Before illustrating some applications with a few examples, below are several guidelines that should be adopted to optimize performance of the FMS2704.

Thermal Diode Connections

When connecting a bipolar transistor configured as a thermal diode, sensing the base-emitter junction with the collector disconnected is not recommended. Intrinsic base resistance will induce an error causing the indicated temperature to be high. Instead connect the transistor in either of the configurations shown in Figure 20:

1. PNP: Collector connected to ground, with DXP connected to the emitter and DXN connected to the base.
2. NPN: Collector connected to base, with DXN connected to the emitter and DXP connected to the base.

Within the FMS2704, there is a return to ground through the DXN pin which conducts the base current of a PNP transistor or the emitter current from an NPN transistor.

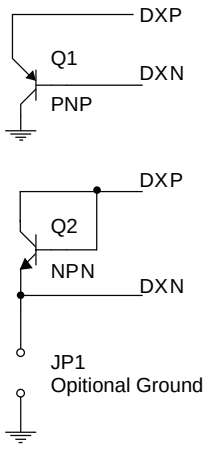


Figure 20. Thermal Diode Connections

Cleanly route the DXP1, DXN1 and DXP2, DXN2 analog traces as pairs over the ground plane. Segregate $DX_{P2\text{-}1,N2\text{-}1}$ traces from digital traces and areas of noise.

Parasitic voltages and leakage can cause errors. Voltage sensitivity is 200µV/°C. 1µA current leakage can cause a 4% change in sensitivity that corresponds to a 12°C error at room temperature.

Fan Control

Whether setting the fan speed through the SMBus or using the internal controller, the fan speed should be constrained between a value corresponding to stall speed and normal rated speed. Stall speed is typically 30% of normal speed.

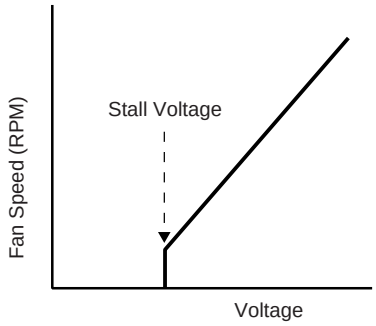


Figure 21. Fan Speed verses Drive Voltage

General

Power is supplied to the V_{CCA} and V_{CCD} pins, which should be de-coupled to ground through local 0.1µF chip capacitors. To minimize the effects of noise, locate the FMS2704 over a ground plane.

Input pin $\overline{\text{STANDBY}}$ and bi-directional pin $\overline{\text{THERM}}$, should be biased to VCCD through a pull-up resistor to prevent spurious triggering. Tachometer inputs are internally biased to VCCD.

Serial Bus pins SCL and SDA require pull-up resistors along the bus but not necessarily local to the FMS2704. ADD must be set H, L or open to match the FMS2704 address to the assigned Serial Bus address.

Recommended ceramic resonator to be connected across the OSC_{2-1} pins is a Murata CSTCC358-TC or equivalent. This resonator includes capacitors that form the resonant circuit of a Colpitts oscillator. If a resonator without internal capacitors is used, external capacitors should be connected as shown in Figure 22.

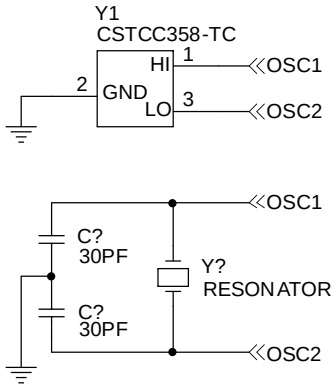


Figure 22. Schematic, Ceramic Resonator Configurations

Example Applications Circuits

Several applications are depicted in the schematics below.

Figure 23 shows how the FMS2704 can be used to set the speed of two fans while monitoring the rotation rates with the tachometer inputs. Fan speed is set by programming the SPEEDA and SPEEDB registers. Drive to the P-channel MOSFETs is set to be PWM.

Figure 24 shows the FMS2704 used as a Fan Speed Controller. Fan Drive increases as the temperature of the thermal diode increases. There are two separate controllers, one for each fan. PNP transistors comprising the diodes may be embedded within processor silicon such as a Pentium II or III.

Figure 25 shows an FMS2704 driving two banks of three fans while monitoring the speed of each fan.

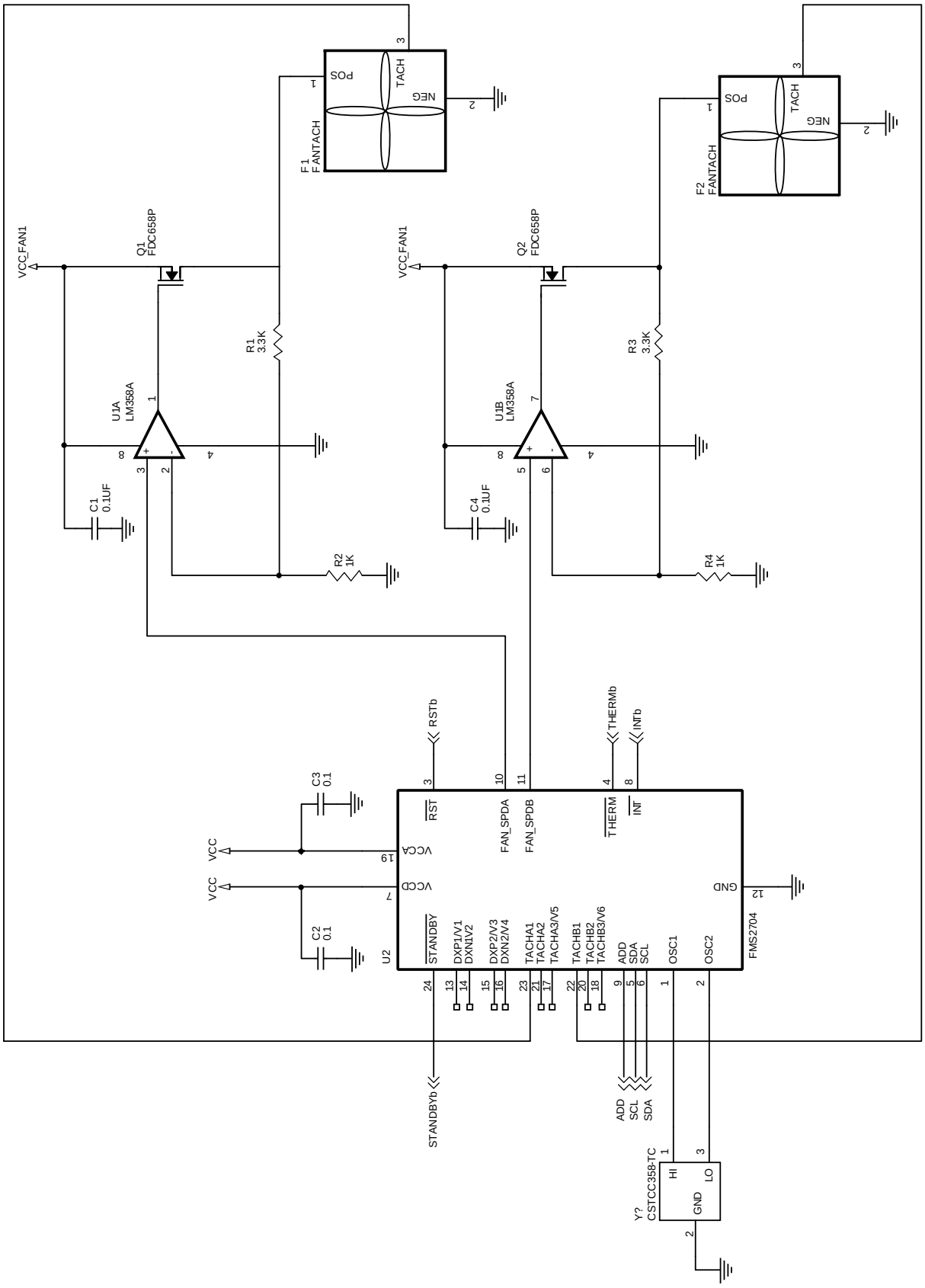


Figure 23. FMS2704 Reference Schematic, Dual Analog Fan Drive with Tachometers

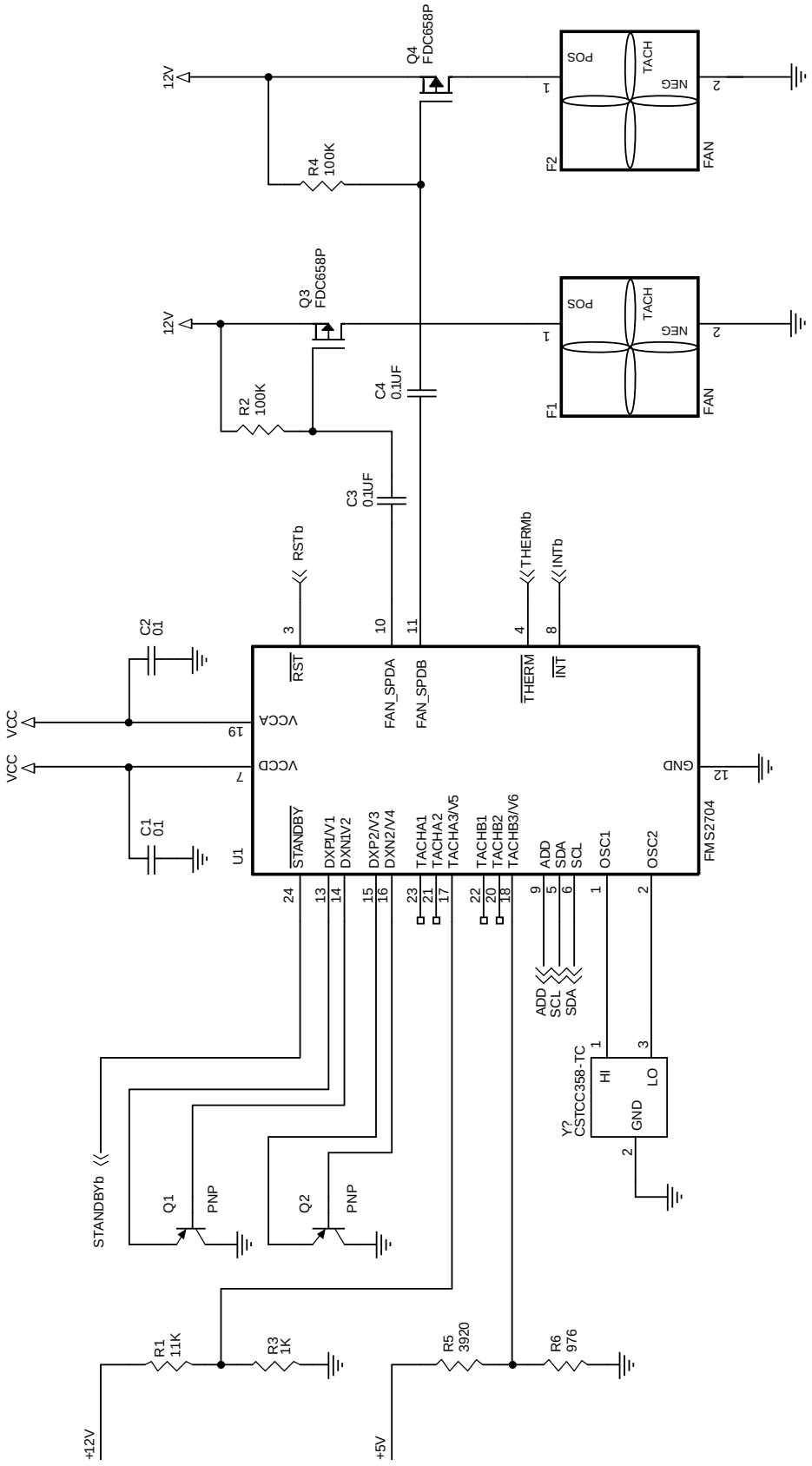


Figure 24. FMS2704 Reference Schematic, Dual PWM Fan Speed Controller with Voltage Monitoring

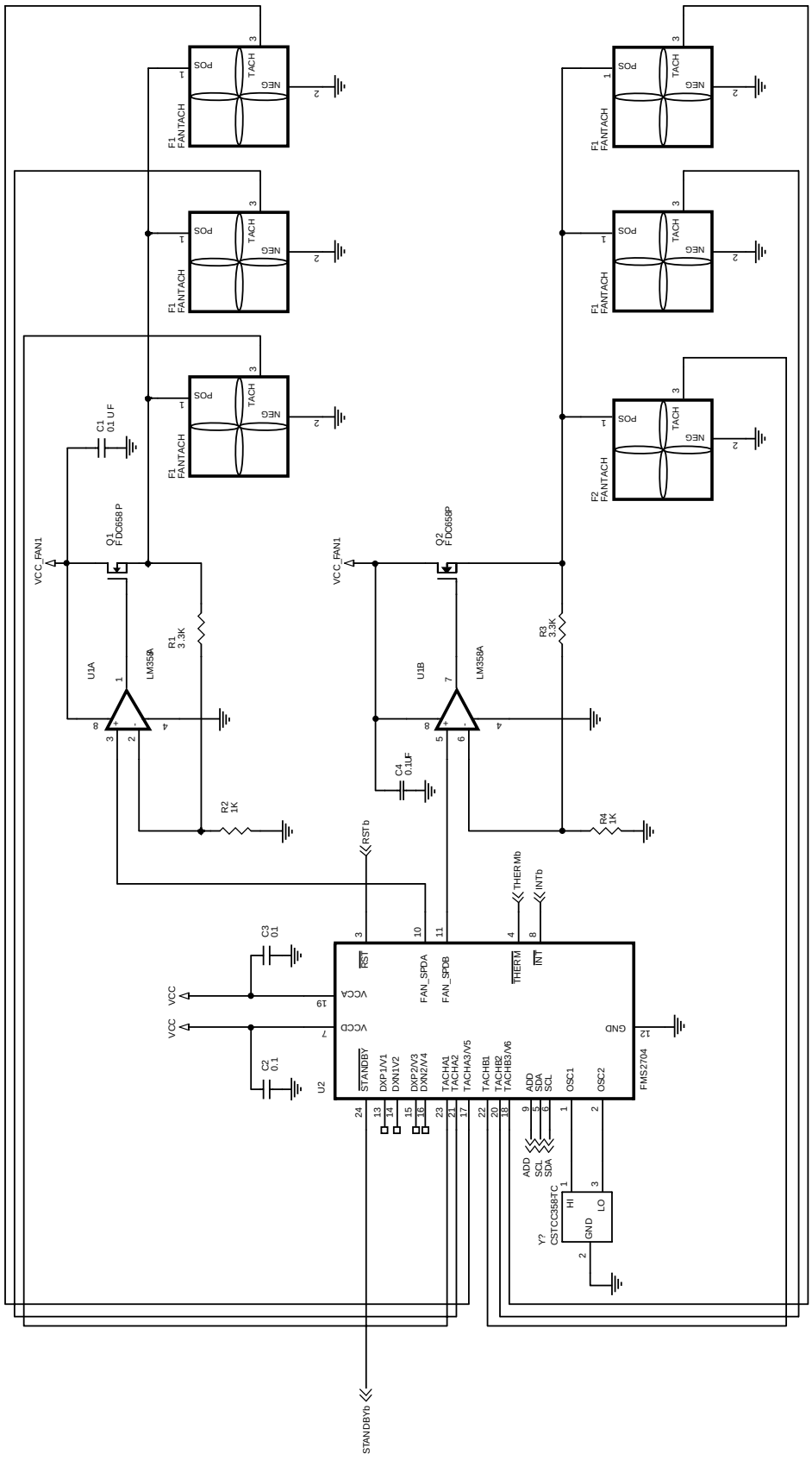


Figure 25. FMS2704 Reference Schematic, Dual Triple Fan Drive, Six Tachometers

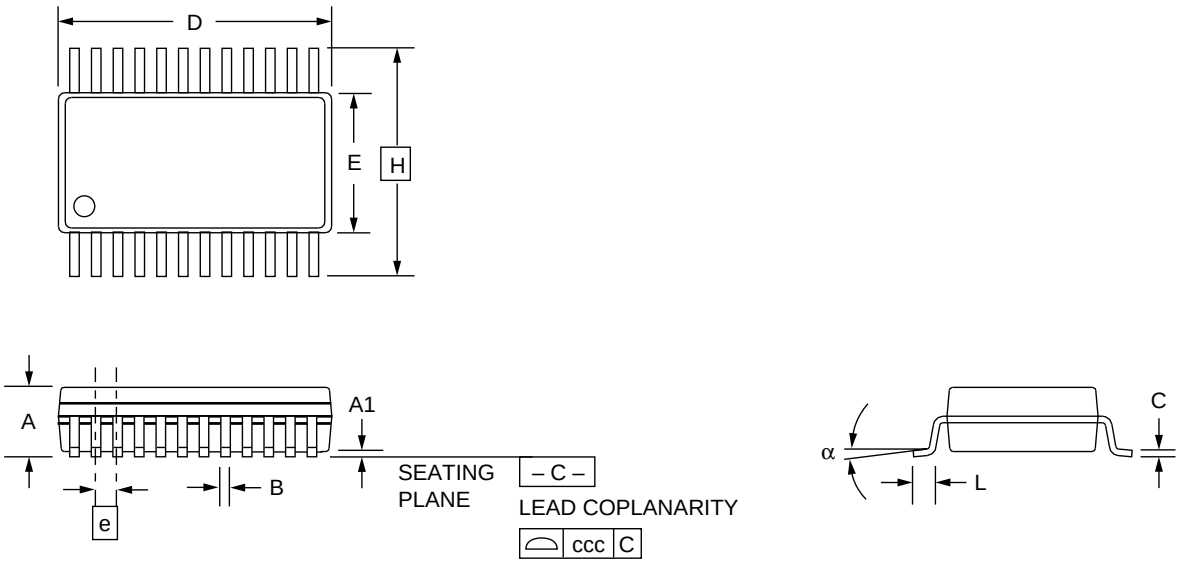
Mechanical Dimensions

24-Lead TSSOP (T1) Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.047	—	1.20	
A1	.002	.006	0.05	0.15	
B	.007	.012	0.19	0.30	
C	.004	.008	0.09	0.20	
D	.308	.316	7.70	7.90	2
E	.172	.180	4.30	4.50	2
e	.026 BSC		0.65 BSC		
H	.256 BSC		6.40 BSC		
L	.018	.030	0.45	0.75	3
N	24		24		5
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .006 inch (0.15mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. Symbol "N" is the maximum number of terminals.



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
FMS2704T1C	0°C to 85°C	Commercial	24 Lead TSSOP	2704T1
FMS2704LT1C	0°C to 85°C	Commercial	24 Lead TSSOP	2704LT1