FMS7209

Spread Spectrum Clock for Motherboards

Features

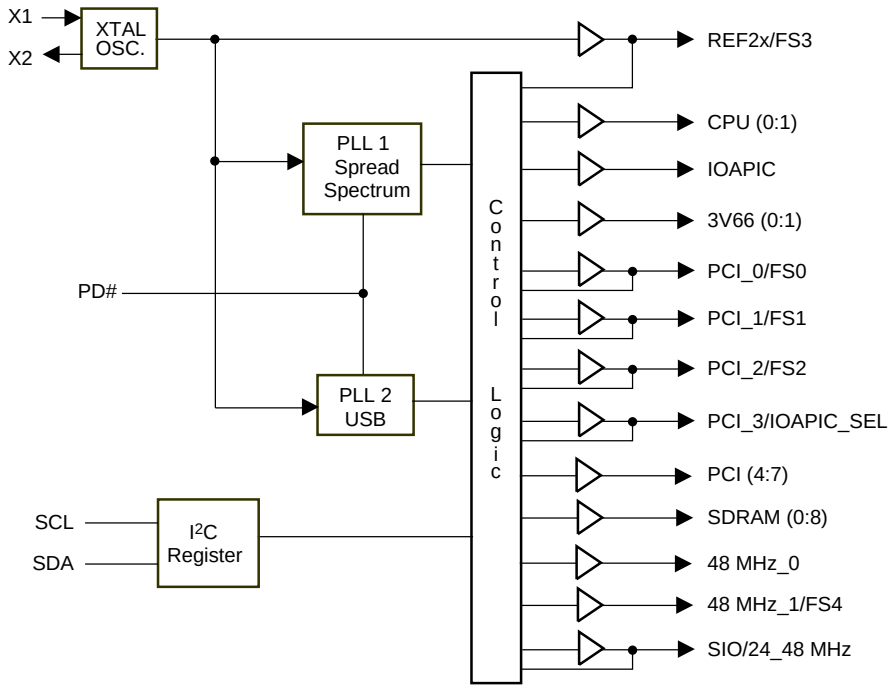
- Employs Fairchild's proprietary Spread Spectrum Technology
- Reduces measured EMI by as much as 10dB
- Supports up to 200 MHz
- I^2C programmable
- Two skew-controlled copies of the CPU clock
- Two copies of 3V66 clock
- One copy of selectable 24 or 48 MHz clock
- Two copies 48MHz clock
- One copy IOAPIC
- One copy REF 14.318MHz clock (3.3V)
- Eight copies PCI clock
- Nine copies of SDRAM clock
- Power down capability

Description

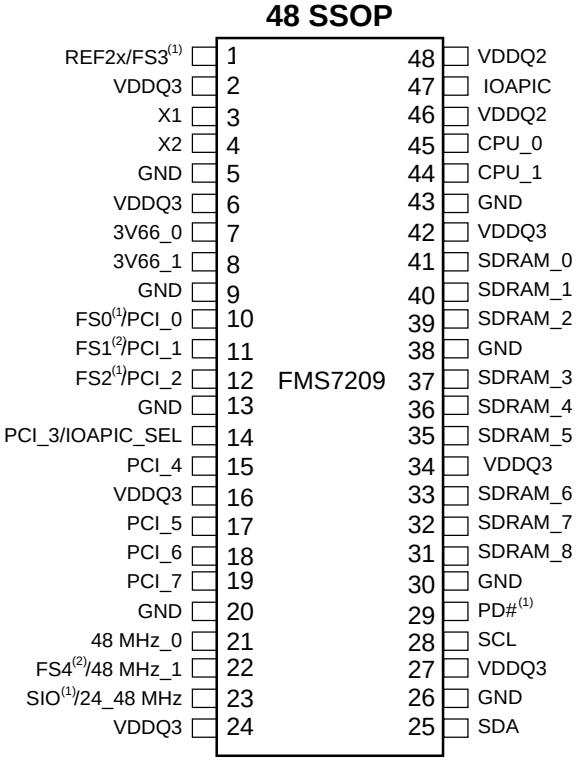
The FMS7209 is a clock synthesizer for motherboard applications. The clock frequencies can be set with the 5 select pins or be set via the I^2C interface.

Advanced Information

Block Diagram



Pin Assignments



Note:

1. Internal 250K Ω pull up resistor. Design should not rely on internal pull-ups.
2. Internal 250K Ω pull down resistor. Design should not rely on internal pull-ups.

Advanced Information

Pin Description

Pin Name	Pin #	Pin Type	Pin Function Description
REF2X/FS3	1	OUT/IN	**I/O Dual function REF2X & FS3:** REF2X is a REF output with double drive strength. FS3 is a latched input that determines device-operating frequency as describe in frequency selection Table 1. Internal pull up.
VDDQ3	2,6,16,24, 27,34,42	Power	**Power connection:** Power supply for core logic, PLL circuitry, SDRAM outputs, PCI outputs, reference, 48 & 24 MHz outputs. Connect to 3.3 Volts
X1	3	IN	**Crystal connection:** An input connection for an external 14.318 MHz crystal. 18 pF internal cap.
X2	4	OUT	**Crystal Connection or External Reference Frequency:** This pin has dual functions. It can be used as an external 14.318 MHz crystal connection or as an external reference frequency input
GND	5,9,13,20, 26,30,38,43	Power	**Ground connection:** Connect all ground pins to the common system ground plane.
3V66 (0:1)	7,8	OUT	**66MHz Clock Output:** 3.3 Volts 66 MHz clocks. The operating frequency is controlled by FS 0:4 (see Table 1).
PCI_0/FS0	10	OUT/IN	**PCI Clock 0/ Frequency Select 0:** PCI Clock 0 is a fixed clock where its frequency is determined by the Frequency Select. FS0 is a latched input that determines device-operating frequency as describe in Frequency Selection Table 1. Internal pull up.
PCI_1/FS1	11	OUT/IN	**PCI clock 1/ Frequency Select 1:** PCI Clock 1 is a output clock where its frequency is determined by the Frequency Select. FS1 is a latched input that determines device-operating frequency as describe in Frequency Selection Table 1. Internal pull up.
PCI_2/FS2	12	OUT/IN	**PCI clock 2/ Frequency Select 2:** PCI Clock 2 is a clock where its frequency is determined by the Frequency Select. FS2 is a latched input that determines device-operating frequency as describe in Frequency Selection Table 1. Internal pull up.
PCI_3/ IOAPIC_SEL	14	OUT/IN	**PCI clock 3/IOAPIC Select:** PCI Clock 3 is a clock where its frequency is determined by the Frequency Select. IOAPIC Select is a latched input that determines IOAPIC operating frequency as described in Frequency Selection Table 1. Internal pull up..
PCI (4:7)	15,17, 18,19	OUT	**PCI clock outputs 4 through 7:** Are PCI output clocks and their frequency is determined by the Frequency Select. See Table 1.
48 MHz_0	21	OUT	**48 MHz clock outputs:** 3.3 volts 48 MHz clock outputs.
48 MHz_1/ FS4	22	OUT/IN	**48 MHz / Frequency Select 4:** 3.3 volts 48 MHz clock outputs. FS4 is a latched input that determines device-operating frequency as describe in Frequency Selection Table 1. Internal pull up.
24_48MHz/ SIO	23	OUT/IN	**Clock Output for Super I/O:** SIO (super I/O) is a latched input. When connected high, the output frequency is 24 MHz. When connected low, the output frequency is 48 MHz. Internal pull up.
SDA	25	IN/OUT	Data pin for I^2C circuitry.
SCL	28	IN	Clock pin for I^2C circuitry.
PD#	29	IN	**Power down Control:** When low, the PLL circuitry shuts off. When high, device is in normal conditions. It has internal pull up.
SDRAM (0:8)	41,40,39, 37,36,35, 33,32,31	OUT	**SDRAM Clock Outputs** 3.3 volt SDRAM outputs. The frequency is determined by FS0: FS4. See Table 1.
CPU (0:1)	44,45	OUT	**CPU output clocks:** The frequency is determined by FS0: FS4. See Table 1. VDDQ2 controls output Voltage.

Advanced Information

Pin Description (continued)

Pin Name	Pin #	Pin Type	Pin Function Description
VDDQ2	46, 48	PWR	**Power connection:** Power supply for all CPU outputs. Connect to 2.5 or 3.3 Volts
IOAPIC	47	OUT	**Synchronous APIC Clock Outputs:** Clock outputs running synchronous to PCI clocks. VDDQ2 controls output Voltage

Table 1. Frequency Selection Table

FS4	FS3	FS2	FS1	FS0	CPU (MHz)	SDRAM (MHz)	CPU/ SDRAM	3V66 (MHz)	PCI (MHz)	IOAPIC_ SEL=1 (MHz)	IOAPIC_ SEL=0 (MHz)
0	0	0	0	0	83.3	124.85	2/3	83.30	41.65	20.83	41.65
0	0	0	0	1	90	90	1	60.00	30.00	15.00	30.00
0	0	0	1	0	75	12.5	2/3	75.00	37.50	18.75	37.50
0	0	0	1	1	72	108	2/3	72.00	36.00	18.00	36.00
0	0	1	0	0	89.07	133.6	2/3	89.07	44.53	22.27	44.53
0	0	1	0	1	95.25	95.25	1	63.50	31.75	15.88	31.75
0	0	1	1	0	121	121	1	80.67	40.33	20.17	40.33
0	0	1	1	1	124	124	1	82.67	41.33	20.67	41.33
0	1	0	0	0	119	119	1	79.33	39.67	19.83	39.67
0	1	0	0	1	114	114	1	76.00	38.00	19.00	38.00
0	1	0	1	0	110	110	1	73.33	36.67	18.33	36.67
0	1	0	1	1	105	105	1	70.00	35.00	17.50	35.00
0	1	1	0	0	66.8	100.2	2/3	66.80	33.40	16.70	33.40
0	1	1	0	1	100.2	100.2	1	66.80	33.40	16.70	33.40
0	1	1	1	0	133.6	133.6	1	66.80	33.40	16.70	33.40
0	1	1	1	1	133.6	100.2	4/3	66.80	33.40	16.70	33.40
1	0	0	0	0	135	101.25	4/3	67.50	33.75	16.88	33.75
1	0	0	0	1	125	125	1	83.33	41.67	20.83	41.67
1	0	0	1	0	127	127	1	84.67	42.33	21.17	42.33
1	0	0	1	1	130	130	1	86.67	43.33	21.67	43.33
1	0	1	0	0	140	140	1	70.00	35.00	17.50	35.00
1	0	1	0	1	136	136	1	68.00	34.00	17.00	34.00
1	0	1	1	0	166	166.00	1	83.00	41.50	20.75	41.50
1	0	1	1	1	155	155	1	77.50	38.75	19.38	38.75
1	1	0	0	0	150	112.5	4/3	75.00	37.50	18.75	37.50
1	1	0	0	1	117	117	1	78.00	39.00	19.50	39.00
1	1	0	1	0	107	107	1	71.33	35.67	17.83	35.67
1	1	0	1	1	100.9	100.9	1	67.27	33.63	16.82	33.63
1	1	1	0	0	145	108.75	4/3	72.50	36.25	18.13	36.25
1	1	1	0	1	140	105	4/3	70.00	35.00	17.50	35.00
1	1	1	1	0	138	103.5	4/3	69.00	34.50	17.25	34.50
1	1	1	1	1	137	102.75	4/3	68.50	34.25	17.13	34.25

Advanced Information

Functional Description

I/O Pin Operation

Dual Purpose I/O pins such as pin 1 REF2X/FS3, act as logic input upon power up. This allows the determination of assigned device function. For example, FS3 along with the other four select pins will determine the clock frequencies as shown in Table 1. A short time after power up, the Logic State is latched and the pin becomes a clock output pin. For example, pin 10 becomes a PCI clock output. This feature reduces device pin count by combining clock outputs with input select pins.

An external 10k ohm "strapping" resistor should be connected between the I/O pin and V_{DD} or GND. A connection to ground sets a "0" bit and a connection to V_{DD} sets a "1" bit. See Figure 1.

Upon power up, the first 2mS of operation is used for input logic selection. The clock output pins are tri-stated, allowing the output strapping resistor on the I/O pin to pull the pin and its associated capacitive clock load to either a logic high or low state. At the end of the 2mS period, the established logic "0" or "1" condition of the I/O pin is then latched. Next the output buffer is enabled which converts the I/O pin into an operating clock output. The 2mS timer is started when V_{DD} (3.3V) reaches 2.0V. Turning the V_{DD} off and then back on again can only reset the input bits.

It should be noted that the strapping resistors have no significant effect on clock output signal integrity. The drive impedance of clock output is 20 ohms (nominal) which is minimally affected by the 10kohm strap to ground or V_{DD}. As with the series termination resistor, the output strapping resistor should be placed as close to the I/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or V_{DD} should be kept less than two inches in length to prevent system noise coupling during input logic sampling.

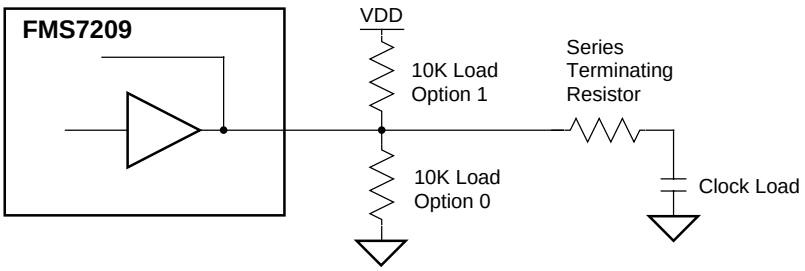


Figure 1. Input Logic Selection through Resistor Load Option

Advanced Information

Serial Data Interface

The FMS7209 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the FMS7209 initializes with default register settings, therefore, the use of this serial data interface is optional. The serial interface is read and writeable only (to the clock chip) and is the dedicated function of device pins SDA and SCL. In motherboard applications, SDA and SCL are typically driven by two logic outputs of the chipset. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions. Table 2 summarizes the control functions of the serial data interface.

Table 2. Serial Data Interface Control Functions Summary

Control Function	Description	Common Application
Clock Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held low.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused PCI slots.
Clock Frequency Selection	Provides CPU, PCI, 3V66 & SDRAM frequencies. Frequency is changed in a smooth and controlled fashion.	For alternate microprocessors and power management options. Smooth frequency transition allows CPU frequency change under normal system operation.
Output Tristate	Puts all clock outputs into a high impedance state.	Production PCB testing.
Test Mode	All clock outputs toggle in relation to X1 input, internal PLL is bypassed. Refer to Table 4.	Production PCB testing.
Reserved	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.

Advanced Information

I²C Register Operation

The FMS7209 is programmed by writing 10 bytes of eight bits each. See Table 3 for byte order.

Table 3. Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the FMS7209 to accept the bits in Data Bytes 3-6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the FMS7209 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Don't Care	Unused by the FMS7209, therefore, bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Don't Care	Unused by the FMS7209, therefore, bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	See Table 4	The data bits in these bytes set internal FMS7209 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to Table 4, Data Byte Serial Configuration Map.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3		
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		

Advanced Information

Writing Data Bytes

Each bit of the 10 data byte controls a particular device function except for the “reserved bits". Bit 7, the MSB, is written first. See Table 4 for bit descriptions of Data Bytes 0-6.

Table 5 shows additional frequency selections that are programmable via the serial data interface.

Table 4. Data Bytes 0-6 serial configuration Map

Bit(s)	Affected pin		Control Function	Bit Control		Default
	Pin No.	Pin name		0	1	
Data Byte 0						
7	—	—	Reserved	—	—	0
6	1	REF2x/FS3	Reserved	—	—	0
5	—	—	Reserved	—	—	0
4	—	—	Reserved	—	—	0
3	—	—	Reserved	—	—	0
2	23	24/48 MHz	Clock output disabled	Low	Active	1
1	21, 22	48 MHz	Clock output disabled	Low	Active	1
0	31	SDRAM_8	Clock output disabled	Low	Active	1
Data Byte 1						
7	32	SDRAM_7	Clock output disabled	Low	Active	1
6	33	SDRAM_6	Clock output disabled	Low	Active	1
5	35	SDRAM_5	Clock output disabled	Low	Active	1
4	36	SDRAM_4	Clock output disabled	Low	Active	1
3	37	SDRAM_3	Clock output disabled	Low	Active	1
2	39	SDRAM_2	Clock output disabled	Low	Active	1
1	40	SDRAM_1	Clock output disabled	Low	Active	1
0	41	SDRAM_0	Clock output disabled	Low	Active	1
Data Byte 2						
7	19	PCI_7	Clock output disabled	Low	Active	1
6	18	PCI_6	Clock output disabled	Low	Active	1
5	17	PCI_5	Clock output disabled	Low	Active	1
4	15	PCI_4	Clock output disabled	Low	Active	1
3	14	PCI_3	Clock output disabled	Low	Active	1
2	13	PCI_2	Clock output disabled	Low	Active	1
1	11	PCI_1	Clock output disabled	Low	Active	1
0	10	PCI_0	Clock output disabled	Low	Active	1
Data Byte 3						
7	—	—	Reserved	—	—	0
6	7	3V66_0	Clock output disabled	Low	Active	1
5	8	3V66_1	Clock output disabled	Low	Active	1
4	—	—	Reserved		—	0
3	47	IOAPIC	Clock output disabled	Low	Active	1
2	44	CPU_1	Clock output disabled	Low	Active	1
1	43	CPU_0	Clock output disabled	Low	Active	1

Advanced Information

Table 4. Data Bytes 0-6 serial configuration Map (continued)

Bit(s)	Affected pin		Control Function	Bit Control		Default
	Pin No.	Pin name		0	1	
0	—	—	Reserved	—	—	0
Data Byte 4						
7	—	SEL_3	See Table 4	—	—	0
6	—	SEL_2	See Table 4	—	—	0
5	—	SEL_1	See Table 4	—	—	0
4	—	SEL_0	See Table 4	—	—	0
3	—	—	Hardware/Software Frequency select	Hardware	Software	0
2	—	SEL_4	See Table 4	—	—	0
1	—	SEL_5	See Table 4	—	—	0
0	—	—	Reserved	—	—	0
Data Byte 5						
7	—	—	0 = ±0.5%, Center Spread Modulation 1 = ±0.75%, Center Spread Modulation	±0.5%	±0.75%	0
6	—	—	Reserved	—	—	0
5	—	—	Reserved	—	—	0
4	—	—	Reserved	—	—	0
3	—	—	Reserved	—	—	0
2	—	—	Reserved	—	—	0
1	—	—	0 = Normal 1 = Spread Spectrum Enable	Normal	Spread	0
0	—	—	Reserved	—	—	0
Data Byte 6						
7	—	—	Reserved	—	—	0
6	—	—	Reserved	—	—	0
5	—	—	Reserved	—	—	0
4	—	—	Reserved	—	—	0
3	—	—	Reserved	—	—	0
2	—	—	Reserved	—	—	0
1	—	—	Reserved	—	—	0
0	—	—	Reserved	—	—	0

Advanced Information

Table 5. Frequency Selection through I^2C Interface

SEL5	SEL4	SEL3	SEL2	SEL0	CPU (MHz)	SDRAM (MHz)	3V66 (MHz)	PCI (MHz)	IOAPIC_ SEL=1 (MHz)	IOAPIC_ SEL=0 (MHz)
0	0	0	0	0	83.3	124.95	83.30	41.65	20.83	41.65
0	0	0	0	1	90	90	60.00	30	15.00	30.00
0	0	0	1	0	75	112.5	75.00	37.5	18.75	37.50
0	0	0	1	1	72	108	72.00	36	18.0	36.00
0	0	0	0	0	89.07	133.6	89.07	44.53	22.27	44.53
0	0	0	0	1	95.25	95.25	63.50	31.75	15.88	31.75
0	0	0	1	0	121	121	80.67	40.33	20.17	40.33
0	0	0	1	1	124	124	82.67	41.33	20.87	41.33
0	0	1	0	0	119	119	79.33	39.67	19.83	39.67
0	0	1	0	1	114	114	76.00	38.00	19.00	38.00
0	0	1	1	0	110	110	73.33	36.67	18.33	36.67
0	0	1	1	1	105	105	70.00	35.00	17.50	35.00
0	0	1	0	0	66.8	100.2	66.80	33.40	16.70	33.40
0	0	1	0	1	100.2	100.2	66.80	33.40	16.70	33.40
0	0	1	1	0	133.6	133.6	66.80	33.40	16.70	33.40
0	0	1	1	1	133.6	100.2	66.80	33.40	16.70	33.40
0	1	0	0	0	135	101.25	87.50	33.75	16.88	33.75
0	1	0	0	1	125	125	83.33	41.67	20.83	41.67
0	1	0	1	0	127	127	84.67	42.33	21.17	42.33
0	1	0	1	1	130	130	86.67	43.33	21.67	43.33
0	1	0	0	0	140	140	70.00	35.00	17.50	35.00
0	1	0	0	1	136	136	68.00	34.00	17.00	34.00
0	1	0	1	0	166	166.00	83.00	41.50	20.75	41.50
0	1	0	1	1	155	155	77.50	38.75	19.38	38.75
0	1	1	0	0	150	112.5	75.00	37.50	18.75	37.50
0	1	1	0	1	117	117	78.00	39.00	19.50	39.00
0	1	1	1	0	107	107	71.33	35.67	17.83	35.67
0	1	1	1	1	100.9	100.9	67.27	33.63	16.82	33.63
0	1	1	0	0	145	108.75	72.50	36.25	18.13	36.25
0	1	1	0	1	140	105	70.00	35.00	17.50	35.00
0	1	1	1	0	138	103.5	69.00	34.50	17.25	34.50
0	1	1	1	1	137	102.75	68.50	34.25	17.13	34.25
1	0	0	0	0	136	102.00	68.00	34.00	17.00	34.00
1	0	0	0	1	138	138.00	69.00	34.50	17.25	34.50
1	0	0	1	0	139	104.25	69.50	34.75	17.38	34.75
1	0	0	1	1	141	141.00	70.50	35.25	17.63	35.25
1	0	0	0	0	142	142.00	71.00	35.50	17.75	35.50
1	0	0	0	1	142	106.50	71.00	35.50	17.75	36.50
1	0	0	1	0	143	143.00	71.50	35.75	17.88	35.75
1	0	0	1	1	143	107.25	71.50	35.75	17.88	35.75

Table 5. Frequency Selection through I^2C Interface (continued)

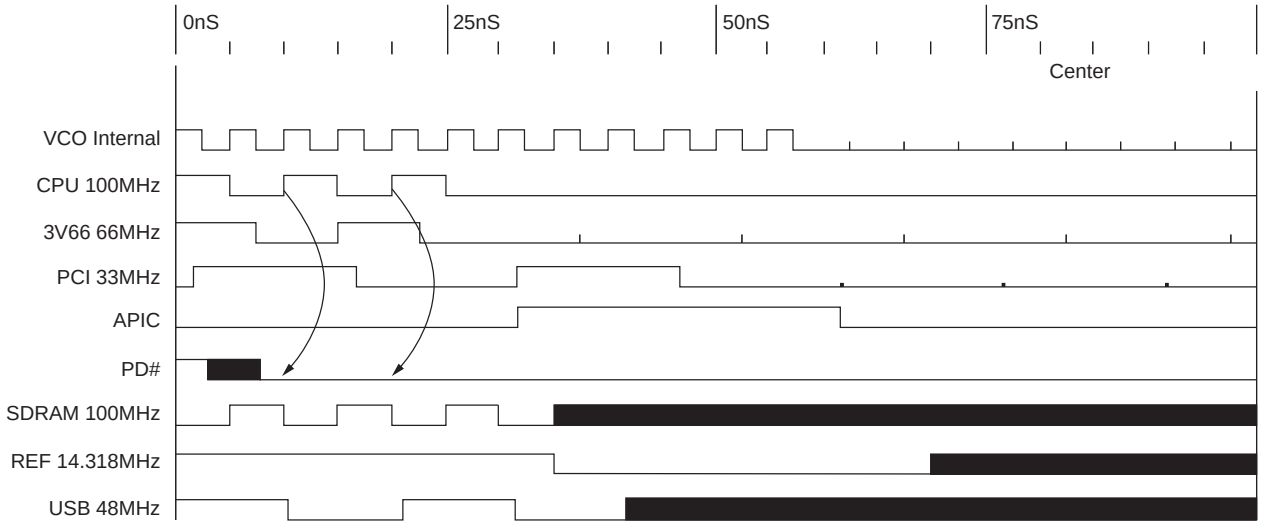
SEL5	SEL4	SEL3	SEL2	SEL0	CPU (MHz)	SDRAM (MHz)	3V66 (MHz)	PCI (MHz)	IOAPIC_ SEL=1 (MHz)	IOAPIC_ SEL=0 (MHz)
1	0	1	0	0	144	144.00	72.00	36.00	18.00	36.00
1	0	1	0	1	144	108.00	72.00	36.00	18.00	36.00
1	0	1	1	0	146	146	73.00	36.50	18.25	36.50
1	0	1	1	1	146	109.50	73.00	36.50	18.25	36.50
1	0	1	0	0	147	147	73.50	36.75	18.38	36.75
1	0	1	0	1	147	110.25	73.50	36.75	18.38	36.75
1	0	1	1	0	148	148.00	74.00	37.00	18.50	37.00
1	0	1	1	1	148	111.00	74.00	37.00	18.50	37.00
1	1	0	0	0	149	111.75	74.50	37.25	18.83	37.25
1	1	0	0	1	152	152.00	76.00	38.00	19.00	38.00
1	1	0	1	0	153	114.75	76.50	38.25	19.13	28.25
1	1	0	1	1	166	156.00	78.00	39.00	19.50	39.00
1	1	0	0	0	157	117.75	78.50	39.25	19.63	39.25
1	1	0	0	1	158	158.00	79.00	39.50	19.76	39.50
1	1	0	1	0	159	119.25	79.50	39.75	19.88	39.75
1	1	0	1	1	160	160.00	80.00	40.00	20.00	40.00
1	1	1	0	0	162	121.5	81.00	40.50	20.25	40.50
1	1	1	0	1	164	164.00	82.00	41.00	20.50	41.00
1	1	1	1	0	170	170.00	85.00	42.50	21.25	42.50
1	1	1	1	1	175	175	87.5	43.75	21.88	43.75
1	1	1	0	0	180	90	60	30	15	30
1	1	1	0	1	185	92.5	81.87	30.83	15.42	30.83
1	1	1	1	0	190	126.67	63.33	31.67	15.83	31.67
1	1	1	1	1	200.4	133.60	66.80	33.40	16.70	33.40

Advanced Information

Advanced Information

Power Down Timing Diagram

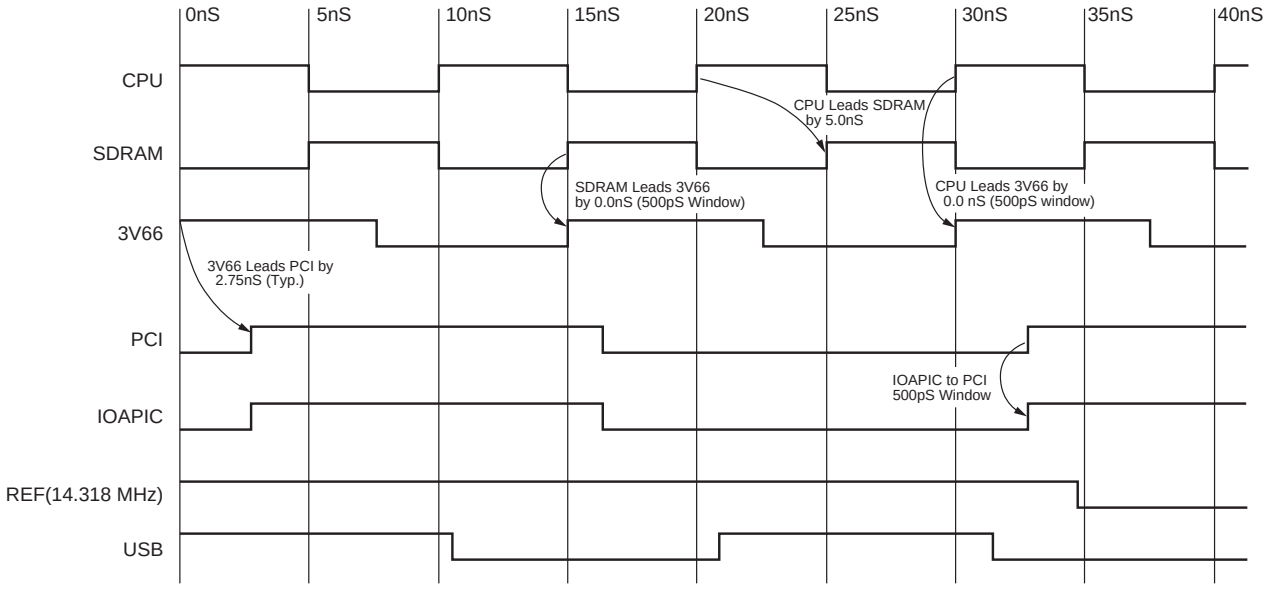
Power down pin is used to shut off clocks cleanly before shutting off power to the device. It is asynchrononous active low input. When it is in a low state all clocks will be driven to a low value and held before turning off the VCO's and the input crystal.



Notes:

1. Once the PD# signal is sampled low for two consecutive rising edges of CPU clock, clocks of interest will be held low on the next high to low transition.
2. PD# is an asynchronous input and metastable conitions could exist. This signal is synchronized inside FMS7209.
3. The shaded sections on the SDRAM, REF, and USB clocks indicate don't care states.
4. Diagrams shown with respect to 100MHz. Similar operation when CPU is 66MHz.

Group Timing Diagram @ 100 MHz



Absolute Maximum Rating

Symbol	Parameter	Ratings	Units
V_{DD}, V_{IN}	Voltage on any pin with respect to ground	-0.5 to 7.0	V
T_{STG}	Storage Temperature	-65 to 150	°C
T_B	Ambient Temperature	-55 to 125	°C
T_A	Operating Temperature	0 to 70	°C
ESD_{PROT}	Input ESD protection	2 (min)	KV

Stresses greater than those listed in the table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may effect reliability.

Electrical Characteristics—Common parameters

T_A = 0 to 70°C; Supply Voltage 3.3 V ±0.5% (unless otherwise stated)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Voltage	V_{IH}		2.0		V_{DD}+ 0.3	V
Input Low Current	I_{IL}	V_{IN} = 0; inputs with no pull-up resistors	-5		5	µA
		V_{IN} = 0; inputs with pull-up resistors			-50	µA
Input High Current	I_{IH}	V_{IN} = V_{DD}; No pull down	-5		5	µA
		V_{IN} = V_{DD}; With pull down			50	µA
Input Capacitance(1)	C_{IN}	All except X1 and X2.			5	pF
		X1 and X2 Pins		18		pF
Output Capacitance(1)	C_{OUT}				6	pF
Input Pin Inductance(1)	L_{IN}				7	nH
Crystal Input Threshold(1)	V_{TH}	V_{DD} = 3.3V		1.5		V
Supply Current	I_{DD}	Freq = 100 M; All outputs loaded			280	mA
	I_{DDL}	Freq = 100 M; All outputs loaded			100	mA
Power down Current	I_{PD}	PD# = GND			10	mA
Clock Stabilization(1)	T_{STAB}	From V_{DD} = 3.3 V to 1% Target			3	mS

Note:

1. Guaranteed by design, not subject to 100% production testing.

Advanced Information

Electrical Characteristics—Group Timing Relationships

T_A = 0 to 70°C; V_{DD} = 3.3V ±0.5%, V_{DDL} = 2.5V ±0.5% (unless otherwise stated)
CPU & IOAPIC C_L = 20 pF; SDRAM & PCI C_L = 30 pF

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
CPU to 3V66(1,2)	$T_{CPU-3V66}$	CPU Freq= 66 MHz; (CPU leads)	7.0	7.5	8.0	nS
SDRAM to CPU(1,2)	T_{CPU-SD}	CPU Freq=66 MHz (SDRAM leads)	2.0	2.5	3.0	nS
SDRAM to 3V66(1,2,3)	$T_{SD-3V66}$	CPU Freq= 66 MHz	0		500	pS
CPU to 3V66(1,2)	$T_{CPU-3V66}$	CPU Freq= 100MHz; (CPU leads)	-		500	pS
CPU to SDRAM(1,2)	T_{CPU-SD}	CPU Freq= 100 MHz (CPU leads)	4.5	5.0	5.5	nS
SDRAM to 3V66(1,2,3)	$T_{SD-3V66}$	CPU Freq= 100 MHz	0		500	pS
3V66 to PCI (1,2)	$T_{3V66-PCI}$	CPU Freq=66 &100 MHz, (3V66 leads)	1.5	2.75	4.0	nS
IOPIC to PCI (1,2,3)	$T_{IOAPIC-PCI}$	CPU Freq= 66 & 100 MHz	0		500	pS

Notes:
1. Guaranteed by design, not subject to 100% production testing.
2. IOAPIC & CPU VTH =1.25 V; SDRAM & 3V66 VTH= 1.5V
3. This specification is 500 pS window, which is defined between the earliest, and the latest clock.

Electrical Characteristics—CPU outputs

T_A = 0 to 70°C; V_{DDL} = 2.5V ±0.5%; C_L = 10 - 20 pF (unless otherwise stated)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Low Voltage	V_{OL}	I_{OL} = 1 mA	-		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.0			V
Output Low Current	I_{OL}	V_{OL} = 1.2 V	27		93	mA
Output High Current	I_{OH}	V_{OH} = 1.0 V	-27		-105	mA
Rise Time(1)	T_R	0.4 to 2.0 V	0.4		1.6	nS
Fall Time(1)	T_F	2.0 to 0.4 V	0.4		1.6	nS
Duty Cycle(1)	D_T	V_{TH} = 1.25 V	45		55	%
Jitter (Cycle-Cycle)(1)	T_{JIT}	V_{TH} = 1.25 V	-		250	pS
Skew(1)	T_{SK}	V_{TH} = 1.25 V	-		175	pS
AC Output Impedance(1)	Z_O			20		Ω

Note:
1. Guaranteed by design, not subject to 100% production testing.

Advanced Information

Electrical Characteristics—IOAPIC output

T_A= 0 to 70°C; V_{DDL}=2.5V ±0.5%; C_L= 10–20 pF (unless otherwise stated)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Low Voltage	V_{OL}	I_{OL} = 1 mA	-		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.0			V
Output Low Current	I_{OL}	V_{OL} = 1.2 V	27		93	mA
Output High Current	I_{OH}	V_{OH} = 1.0 V	-27		-105	mA
Rise Time(1)	T_R	0.4 to 2.0 V	0.4		1.6	nS
Fall Time(1)	T_F	2.0 to 0.4 V	0.4		1.6	nS
Duty Cycle(1)	D_T	V_{TH} = 1.25 V	45		55	%
Jitter (Cycle-Cycle)(1)	T_{JIT}	V_{TH} = 1.25 V	-		500	pS
AC Output Impedance(1)	Z_O			15		Ω

Note:

1. Guaranteed by design, not subject to 100% production testing.

Electrical Characteristics—PCI outputs

T_A = 0 to 70°C; Supply Voltage V_{DD} = 3.3V ±0.5%; C_L = 10–30 pF (unless otherwise stated)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Low Voltage	V_{OL}	I_{OL} = 1 mA	-		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V
Output Low Current	I_{OL}	V_{OL} = 1.95 V	30		178	mA
Output High Current	I_{OH}	V_{OH} = 1.0 V	-33		-184	mA
Rise Time(1)	T_R	0.8 to 2.0 V	0.5		2.0	nS
Fall Time(1)	T_F	2.0 to 0.8 V	0.5		2.0	nS
Duty Cycle(1)	D_T	V_{TH} = 1.5 V	45		55	%
Jitter (Cycle-Cycle)(1)	T_{JIT}	V_{TH} = 1.5 V	-		500	pS
Skew(1)	T_{SK}	V_{TH} = 1.5 V			500	pS
AC Output Impedance(1)	Z_O			30		Ω

Note:

1. Guaranteed by design, not subject to 100% production testing.

Advanced Information

Electrical Characteristics—3V66 outputs

T_A = 0 to 70°C; V_{DD} = 3.3V ±0.5%; C_L = 10 – 30 pF (unless otherwise stated)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Low Voltage	V_{OL}	I_{OL} = 1 mA	-		0.5	V
Output High Voltage	V_{OH}	I_{OH} = -1 mA	3.1			V
Output Low Current	I_{OL}	V_{OL} = 1.95 V	30		178	mA
Output High Current	I_{OH}	V_{OH} =1.0 V	-33		-184	mA
Rise Time(1)	T_R	0.4 to 2.4 V	0.5		2.0	nS
Fall Time(1)	T_F	2.4 to 0.4 V	0.5		2.0	nS
Duty Cycle(1)	D_T	V_{TH} = 1.5 V	45		55	%
Jitter (Cycle-Cycle)(1)	T_{JIT}	V_{TH} = 1.5 V	-		500	pS
Skew(1)	T_{SK}	V_{TH} = 1.5 V	-		175	pS
AC Output Impedance(1)	Z_O			30		Ω

Note:

1. Guaranteed by design, not subject to 100% production testing.

Electrical Characteristics—REF outputs

T_A = 0 to 70°C; V_{DD} = 3.3V ±0.5%; C_L = 10 – 20 pF (unless otherwise stated)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Low Voltage	V_{OL}	I_{OL} = 1 mA	-		0.5	V
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V
Output Low Current	I_{OL}	V_{OL} =1.5 V	25		76	mA
Output High Current	I_{OH}	V_{OH} =1.5 V	-94		-27	mA
Rise Time(1)	T_R	0.8 to 2.0 V	-		1.6	nS
Fall Time(1)	T_F	2.0 to 0.8 V	-		1.6	nS
Duty Cycle(1)	D_T	V_{TH} = 1.5 V	45		55	%
Jitter (Cycle-Cycle)(1)	T_{JIT}	V_{TH} = 1.5 V	-		1000	pS
AC Output Impedance(1)	Z_O			30		Ω

Note:

1. Guaranteed by design, not subject to 100% production testing.

Advanced Information

Electrical Characteristics—48/24 MHz outputs

T_A = 0 to 70°C; V_{DD} = 3.3V ±0.5%; C_L = 10 – 20 pF (unless otherwise stated)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Low Voltage	V_{OL}	I_{OL} = 1 mA	-		0.5	V
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V
Output Low Current	I_{OL}	V_{OL} =1.5 V	25		76	mA
Output High Current	I_{OH}	V_{OH} =1.5 V	-94		-27	mA
Rise Time(1)	T_R	0.4 to 2.4 V	1.0		4.0	nS
Fall Time(1)	T_F	2.4 to 0.4 V	1.0		4.0	nS
Duty Cycle(1)	D_T	V_{TH} = 1.5 V	45		55	%
Jitter (Cycle-Cycle)(1)	T_{JIT}	V_{TH} = 1.5 V	-		500	pS
Skew(1)	T_{SK}	V_{TH} = 1.5 V	-		250	pS
AC Output Impedance(1)	Z_O			40		Ω

Note:

1. Guaranteed by design, not subject to 100% production testing.

Electrical Characteristics—SDRAM outputs

T_A = 0 to 70°C; V_{DD} = 3.3V ±0.5%; C_L = 20 – 30 pF (unless otherwise stated)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Low Voltage	V_{OL}	I_{OL} = 1 mA	-		0.5	V
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V
Output Low Current	I_{OL}	V_{OL} = 2.0 V	72		184	mA
Output High Current	I_{OH}	V_{OH} =1.0 V	-54		-157	mA
Rise Time(1)	T_R	0.4 to 2.4 V	0.4		1.6	nS
Fall Time(1)	T_F	2.4 to 0.4 V	0.4		1.6	nS
Duty Cycle(1)	D_T	V_{TH} = 1.5 V	45		55	%
Jitter (Cycle-Cycle)(1)	T_{JIT}	V_{TH} = 1.5 V	-		250	pS
Skew(1)	T_{SK}	V_{TH} = 1.5 V	-		250	pS
AC Output Impedance(1)	Z_O			40		Ω

Note:

1. Guaranteed by design, not subject to 100% production testing.

Advanced Information

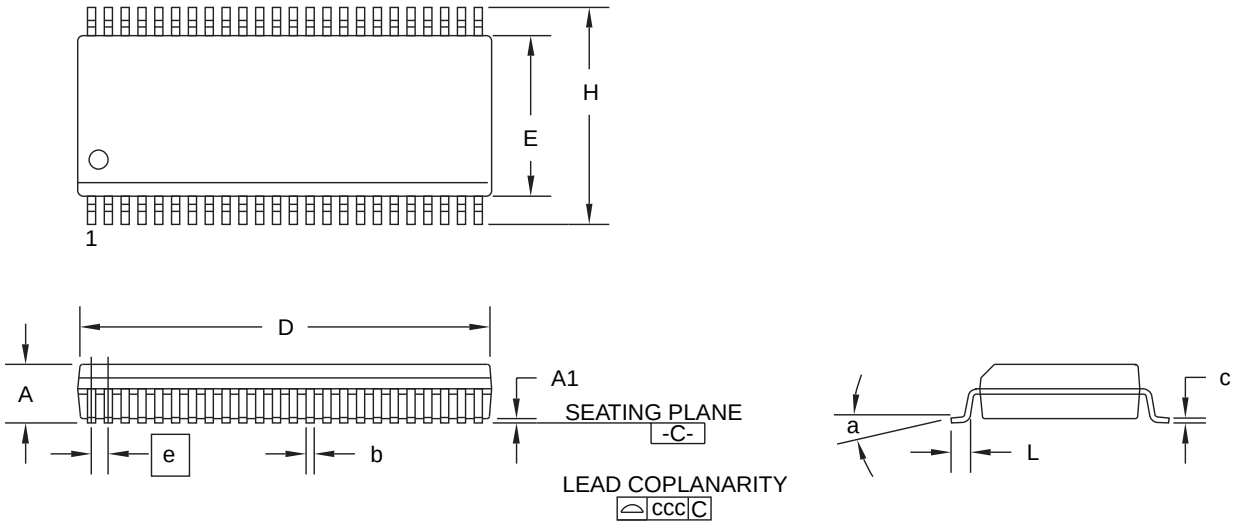
Mechanical Dimensions

48 pin SSOP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.095	.110	2.41	2.79	
A1	.008	.016	0.20	0.41	
b	.008	.0135	0.20	0.34	5
c	.005	.010	0.13	0.25	5
D	.620	.630	15.75	16.00	2, 4
H	.395	.420	10.03	10.67	
E	.291	.299	7.39	7.59	2
e	.025 BSC		0.64 BSC		
L	.020	.040	0.51	1.02	3
N	48		48		6
a	0°	8°	0°	8°	
ccc	---	.004	---	0.13	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
2. "D" and "E1" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "b" & "c" dimensions include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



Advanced Information

Ordering Information

Product Number	Package
FMS7209MEA	48 pin SSOP

Advanced Information