HA19214NT

High Speed 10-bit A/D Converter

HA19214 is a monolithic bipolar LSI for serial-parallel 10-bit analog to digital conversion which includes track and hold circuit for analog input. Digital output level is compatible with HS-CMOS, and clock input level is compatible with LS-TTL and HS-CMOS.
It is designed for video signal processing and for data conversion of video signal to computer input.

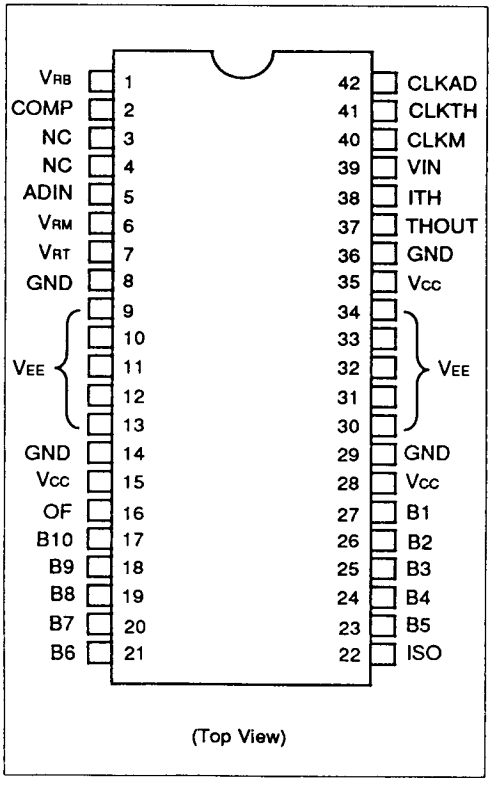
Features

- 10-bit resolution (Overflow Included)
- Maximum conversion rate: 20Msps (typ.)
- Power Dissipation: 900mW (typ.)
- Track and hold circuit (T/H circuit) included
- Operation power supply: +5V, –5V
- Clock input level: compatible with LS-TTL and HS-CMOS
- Digital output level: compatible with HS-CMOS
- 42-pin Plastic Shrink DIP

Applications

- Digital video processing, including digital TV, digital VCR.

Pin Arrangement



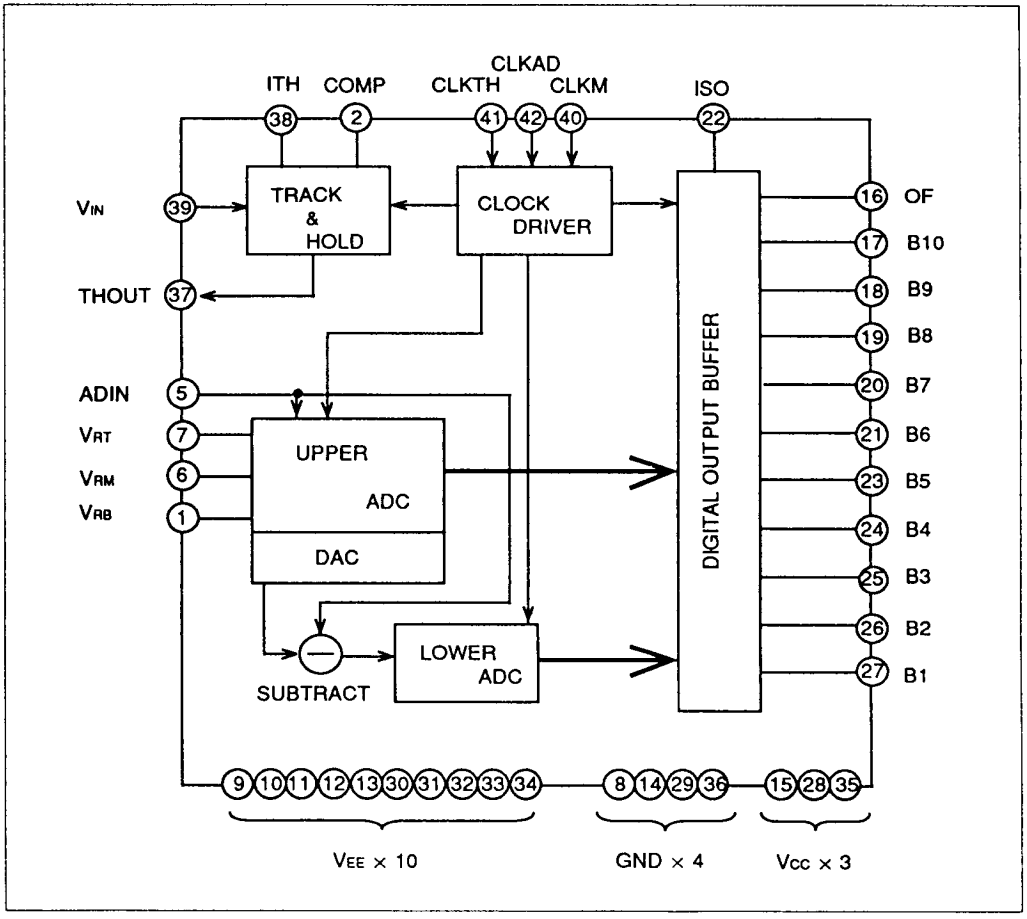
Ordering Information

Type No.	Package
HA19214NT	DP-42TS

Pin Functions

No.	Symbol	Function	Description
1	V_{RB}	Reference voltage input (low level)	–2V is applied from outside
2	COMP	Phase compensation pin	Connect 0.1 µF to V_{EE}
3	NC	No connection	
4	NC	No connection	
5	ADIN	ADC analog input	Connect to THOUT pin 37
6	V_{RM}	Reference voltage correction input	
7	V_{RT}	Reference voltage input (high level)	Connect 39Ω and 0.1µF to GND
8	GND	Ground	
9 to 13	V_{EE}	Power supply (–5V)	
14	GND	Ground	
15	Vcc	Power supply (+5V)	
16	OF	Digital output	Overflow output
17	B10	Digital output	MSB
18	B9	Digital output	
19	B8	Digital output	
20	B7	Digital output	
21	B6	Digital output	
22	ISO	Output current setting input	Connect 2-3kΩ to Vcc, 0.1µF to GND
23	B5	Digital output	
24	B4	Digital output	
25	B3	Digital output	
26	B2	Digital output	
27	B1	Digital output	LSB
28	Vcc	Power supply voltage (+5V)	
29	GND	Ground	
30 to 34	V_{EE}	Power supply voltage (–5V)	
35	Vcc	Power supply voltage (+5V)	
36	GND	Ground	
37	THOUT	T/H output	Connect to ADIN pin 5
38	ITH	T/H bias setting	Connect 13.5kΩ and 0.1µF to Ground
39	VIN	T/H analog input	Input range: 0 to +2V
40	CLKM	Clock threshold input	Apply logic threshold level (+1.5 to +2.5V)
41	CLKTH	Clock input for T/H	TTL or CMOS level
42	CLKAD	Clock input for ADC	TTL or CMOS level

Block Diagram



Absolute Maximum Ratings (Ta=25°C, unless otherwise specified.)

Item	Symbol	Rating	Unit
Power Supply voltage	V_{CC}	+6.0	V
	V_{EE}	−6.0	V
Clock input voltage	V_{CLK}	0 to +V_{CC}	V
Power Supply current	I_{CC}	+140	mA
	I_{EE}	−170	mA
Power dissipation	P_T	1.3	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Electrical Characteristics (Ta=25°C, V_{CC}=5.0V, V_{EE}=−5.0V, V_{RB}=−2.0 V, unless otherwise specified.)

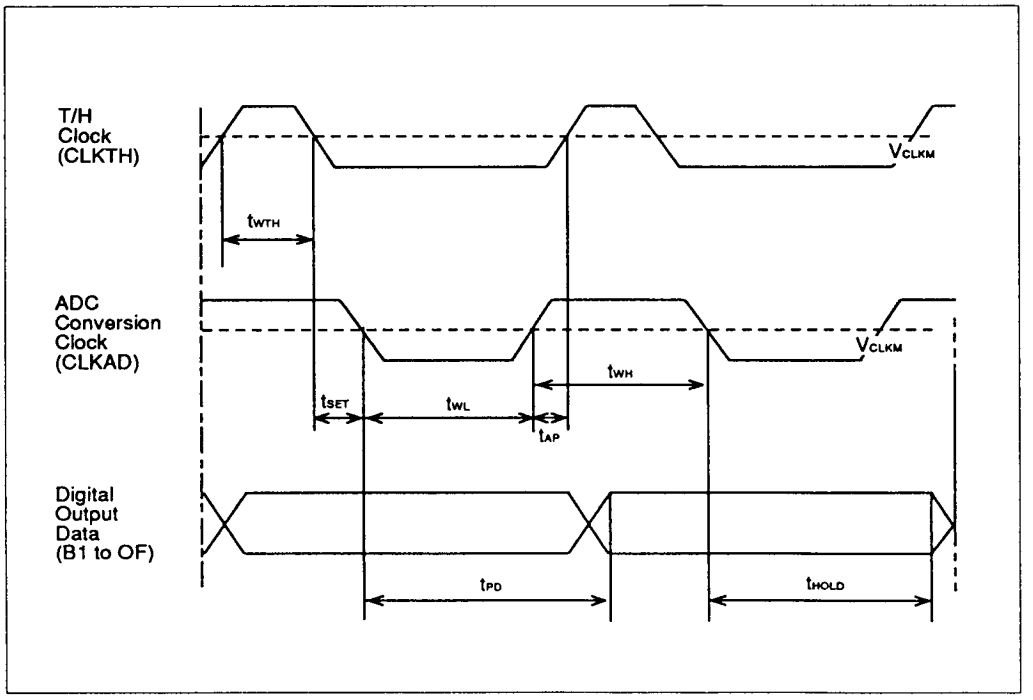
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Operating power supply voltage	V_{CC}	4.75	5.00	5.25	V	
	V_{EE}	−5.25	−5.00	−4.75	V	
Power supply current	I_{CC}	—	90	115	mA	V_{IN} = 2.1V, V_{CLKM} = 1.5V,
	I_{EE}	−140	−110	—	mA	V_{CLKSH} = 2V, V_{CLKAD} = 2V
Reference current	I_{RT}	0.70	1.00	1.30	mA	V_{IN} = 0 to 2V
	I_{RB}	−1.75	−2.50	−3.25	mA	V_{IN} = 0 to 2V
Analog input current (T/H)	Iin (T/H)	—	100	250	µA	V_{IN} = 0 to 2V V_{CLKTH} = 2V, V_{CLKM} = 1.5V
Clock input current	I_{IH} (CLKAD)	0.17	0.30	0.40	mA	V_{CLKAD} = 2.7V V_{CLKM} = 1.5V
	I_{IH} (CLKTH)	0.17	0.30	0.40	mA	V_{CLKTH} = 2.7V V_{CLKM} = 1.5V
	I_{IL} (CLKAD)	0.10	0.17	0.22	mA	V_{CLKAD} = 0.4V V_{CLKM} = 1.5V
	I_{IL} (CLKTH)	0.10	0.17	0.22	mA	V_{CLKTH} = 0.4V V_{CLKM} = 1.5V
Clock input impedance	Z_{CLKM}	6.5	9.0	11.5	kΩ	V_{CLKM} = 1.5V to 2.5V

Electrical Characteristics (Ta=25°C, V_{CC}=5.0V, V_{EE}=–5.0V, V_{RB}=–2.0 V, unless otherwise specified.) (cont)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Clock VTH voltage setting range	V_{CLKM}	1.5	—	2.5	V	
T/H level shift voltage	V_{SHIFT}	–2.25	–2.00	–1.75	V	V_{IN} = 0 to 2V
T/H reference pin voltage	V_{ITH}	–1.50	–1.40	–1.30	V	
Digital output voltage	V_{OH1}	3.90	4.10	—	V	I_{OH} = –0.4mA
	V_{OH2}	3.75	3.95	—	V	I_{OH} = –2.0mA
	V_{OL}	—	750	850	mV	I_{OL} = 0.4mA, I_{SO} = 2mA
Digital output current	I_{OL}	1.70	1.90	2.10	mA	I_{SO} = 2mA
Integral linearity	I_{NL}	—	2.5	4.0	LSB p-p*1	f_{CLK} = 15Msps
Differential linearity	D_{NL}	—	±0.8	±1.5	LSB *2	f_{CLK} = 15Msps
Max conversion rate	f_{CLK} (MAX)	15	20	—	Msps	50% duty cycle
ADC clock pulse width	t_{WH} (MIN)	—	25	33	ns	f_{CLK} = 15Msps fin = 6MHz, V_{IN} = 1.8Vpp
	t_{WL} (MIN)	—	25	31	ns	
T/H clock pulse width	t_{WSH} (MIN)	—	13	18	ns	
T/H settling time	t_{SET} (MIN)	—	8	15	ns	
Lower ADC acquisition time	t_{AP} (MIN)	—	–5	0	ns	
Digital output delay time	t_{PD}	—	40	55	ns	
Digital output holding time	t_{HOLD}	5	10	—	ns	
Analog input band width	fin (MIN)	6	8	—	MHz	V_{IN} = 1.8Vp-p f_{CLK} = 15Msps
Differential gain	DG	—	(1.0)	—	%	
Differential phase	DP	—	(0.5)	—	deg	
Signal to noise ratio	SNR	—	55	—	dB	fin = 1MHz
			52	—	dB	fin = 5MHz

Notes: *1. Measure peak to peak (p-p) for the maximum positive value and the maximum negative value of the linearity error.
*2. Measure maximum positive and maximum negative values from the linearity error between neighboring codes.

Timing Chart



Circuit Example