HITACHI

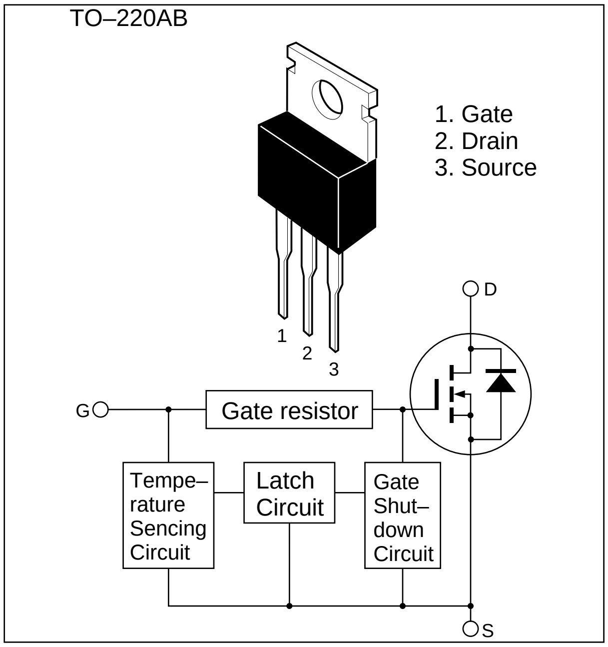
ADE–208–353 B (Z)

THERMAL FET HAF2001

Silicon N Channel MOS FET Series

HITACHI

3rd. Edition
July 1996



Application

Power switching
Over temperature shut–down capability

Features

This FET has the over temperature shut–down capability sensing to the junction temperature. This FET has the built–in over temperature shut–down circuit in the gate area. And this ciruit operation to shut–down the gate voltage in case of high junction temperature like applying over power consumption, over curretn etc.

- Logic level operation (4 to 6 V Gate drive)
- High endurance capability against to the short circuit
- Built–in the over temperature shut–down circuit
- Latch type shut–down operation (Need 0 voltage recovery)

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS+}	16	V
Gate to source voltage	V_{GSS-}	–2.8	V
Drain current	I_D	20	A
Drain peak current	$I_{D(pulse)}{}^*$	40	A
Body–drain diode reverse drain current	I_{DR}	20	A
Channel dissipation	Pch**	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10µs, duty cycle < 1 %
** Value at Tc = 25°C

Table 2 Typical Operation Characteristics

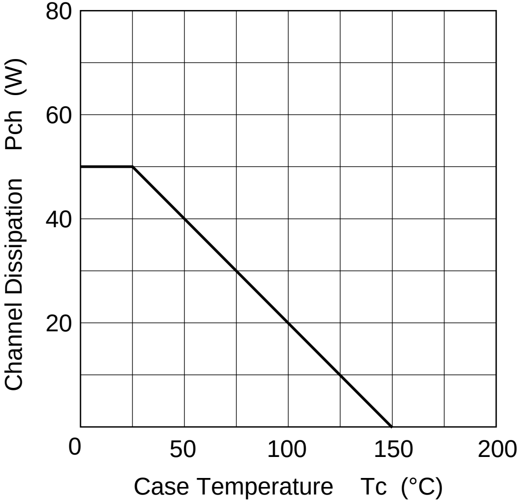
Item	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test conditions**
Input voltage	V_{IH}	3.5	—	—	V	
	V_{IL}	—	—	1.2	V	
Input current (Gate non shut down)	I_{IH}	—	—	100	µA	V_i = 8 V, V_{DS} = 0
	I_{IL}	—	—	50	µA	V_i = 3.5 V, V_{DS} = 0
	I_I	—	—	1	µA	V_i = 1.2 V, V_{DS} = 0
Input current (Gate shut down)	$I_{IH(sd)1}$	—	0.8	—	mA	V_i = 8 V, V_{DS} = 0
	$I_{IH(sd)2}$	—	0.35	—	mA	V_i = 3.5 V, V_{DS} = 0
Shut down temperature	T_{sd}	—	175	—	°C	Channel temperature

Table 3 Electrical Characteristics (Ta = 25°C)

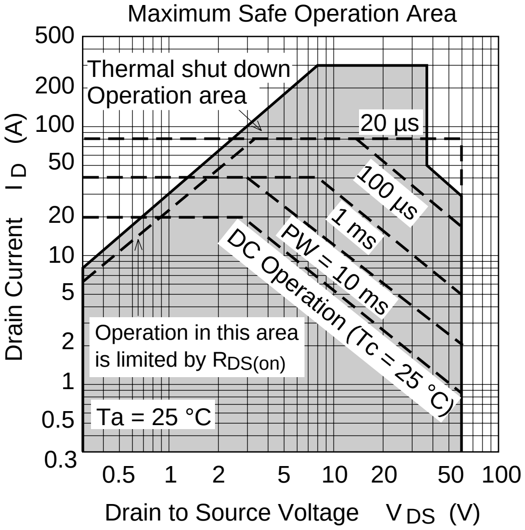
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain current	I_{D1}	10	—	—	A	V_{GS} = 3.5 V, V_{DS} = 10 V
Drain current	I_{D2}	—	—	10	mA	V_{GS} = 1.2 V, V_{DS} = 10 V
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$ +	16	—	—	V	I_G = 100 µA, V_{DS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$ –	–2.8	—	—	V	I_G = –100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS} + 1	—	—	100	µA	V_{GS} = 8 V, V_{DS} = 0
	I_{GSS} + 2	—	—	50	µA	V_{GS} = 3.5 V, V_{DS} = 0
	I_{GSS} + 3	—	—	1	µA	V_{GS} = 1.2 V, V_{DS} = 0
	I_{GSS} –	—	—	–100	µA	V_{GS} = –2.4 V, V_{DS} = 0
Input current (shut down)	$I_{GS(op)1}$	—	0.8	—	mA	V_{GS} = 8 V, V_{DS} = 0
	$I_{GS(op)2}$	—	0.35	—	mA	V_{GS} = 3.5 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cut off voltage	$V_{GS(off)}$	1.0	—	2.25	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	50	65	mΩ	I_D = 10 A , V_{GS} = 4 V*
	$R_{DS(on)}$	—	30	43	mΩ	I_D = 10 A , V_{GS} = 10 V*
Forward transfer admittance	$\lvert y_{fs} \rvert$	6	12	—	S	I_D = 10 A* V_{DS} = 10 V
Output capacitance	Coss	—	630	—	pF	V_{DS} = 10 V , V_{GS} = 0 f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	7.5	—	µs	I_D = 5 A
Rise time	t_r	—	29	—	µs	V_{GS} = 5 V
Turn–off delay time	$t_{d(off)}$	—	34	—	µs	R_L = 6 Ω
Fall time	t_f	—	26	—	µs	
Body–drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 20 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	110	—	ns	I_F = 20 A, V_{GS} = 0, diF / dt = 50 A / µs
Over load shut down operation time (Note 1)	t_{os1}	—	1.8	—	ms	V_{GS} = 5 V, V_{DD} = 12 V
	t_{os2}	—	0.7	—	ms	V_{GS} = 5 V, V_{DD} = 24 V

(Note 1) Including the junction temperature taise of the over loaded condition. * Pulse Test

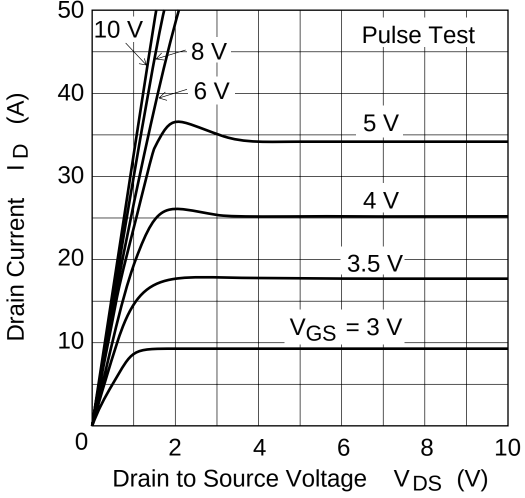
Power vs. Temperature Derating



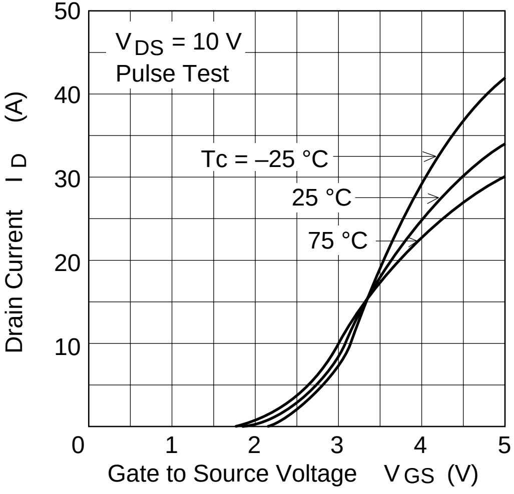
Maximum Safe Operation Area

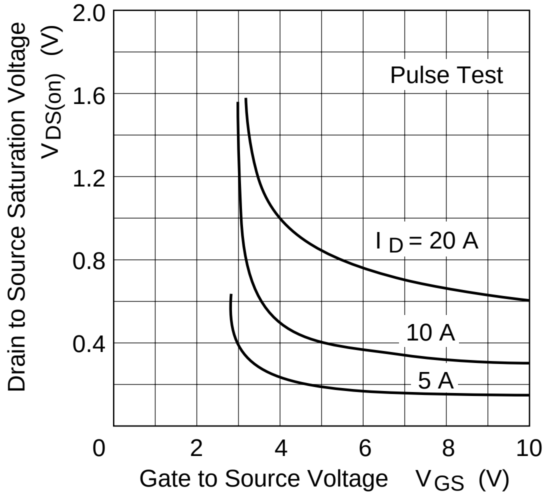


Typical Output Characteristics

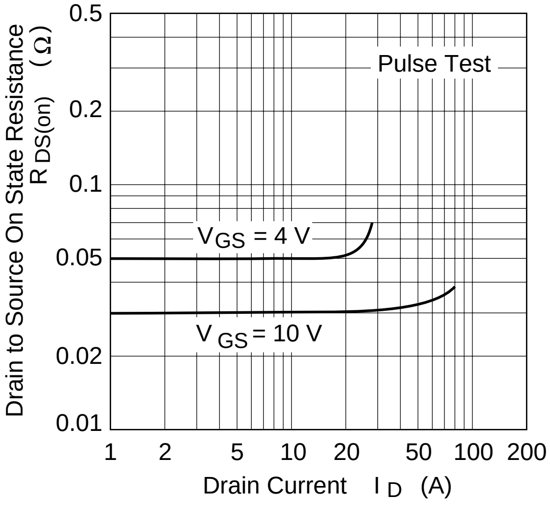


Typical Transfer Characteristics

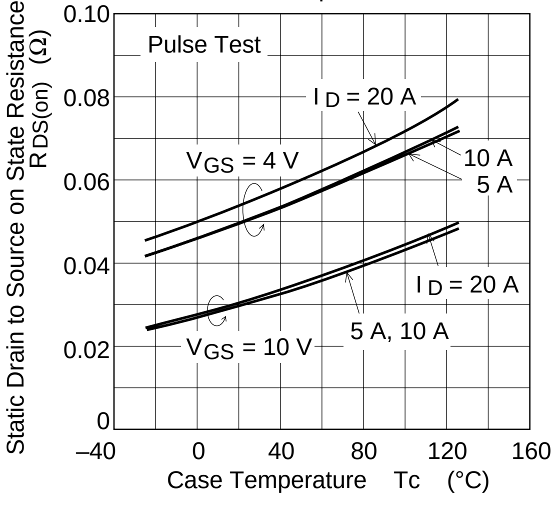




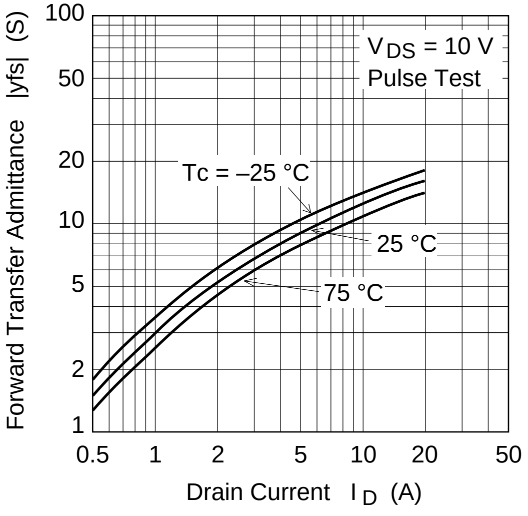
Drain to Source Saturation Voltage vs. Gate to Source Voltage



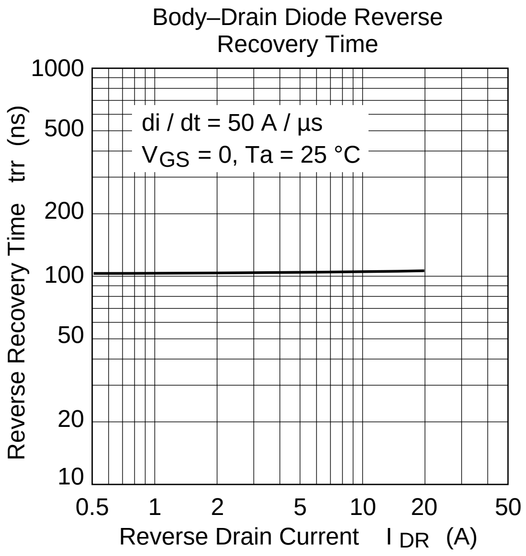
Static Drain to Source State Resistance vs. Drain Current



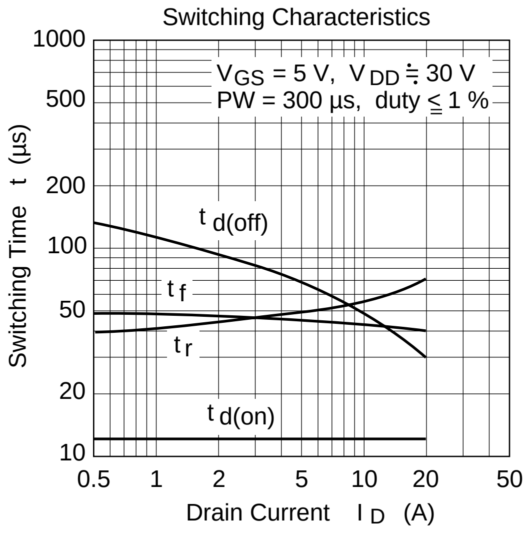
Static Drain to Source on State Resistance vs. Temperature



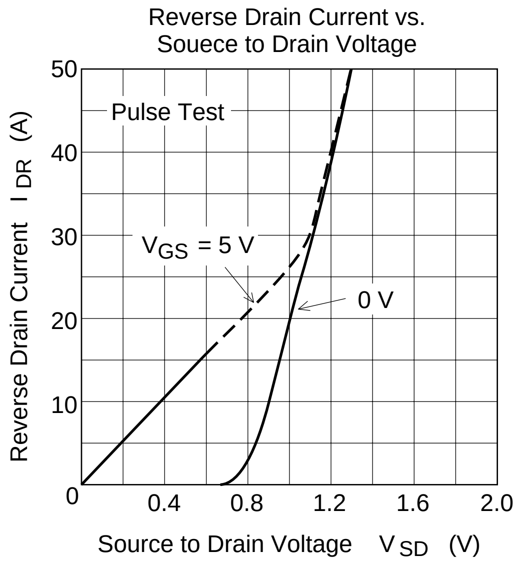
Forward Transfer Admittance vs. Drain Current



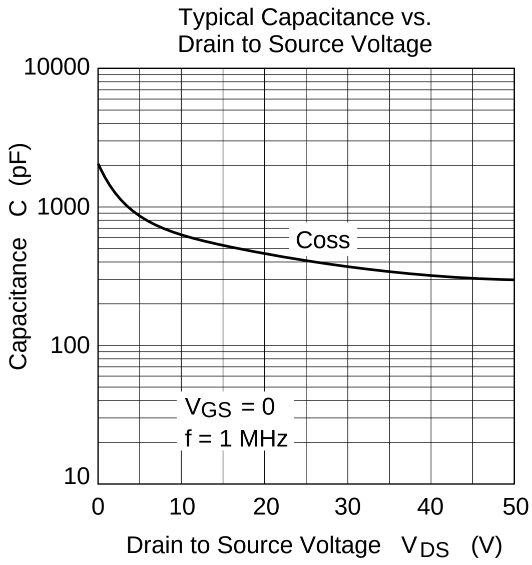
Body–Drain Diode Reverse Recovery Time



Switching Characteristics

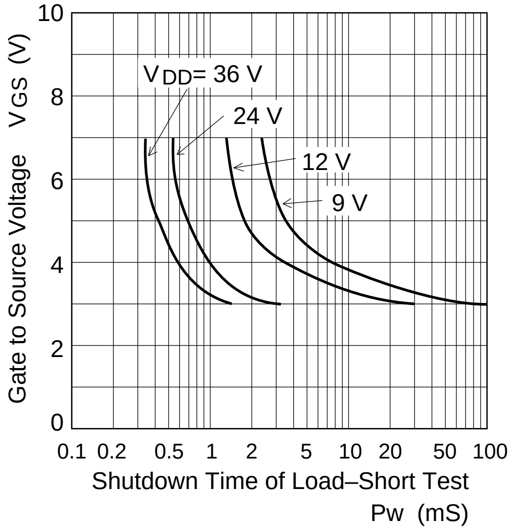


Reverse Drain Current vs. Souece to Drain Voltage

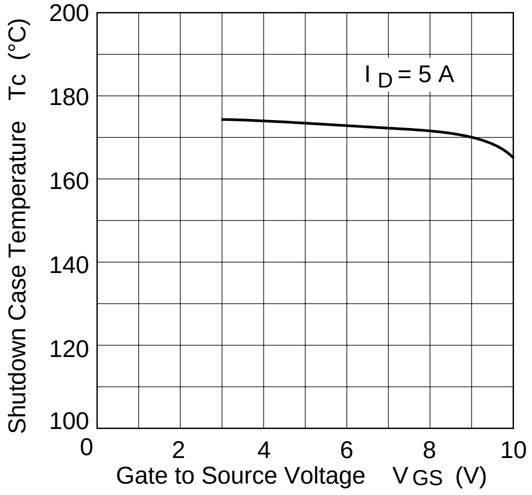


Typical Capacitance vs. Drain to Source Voltage

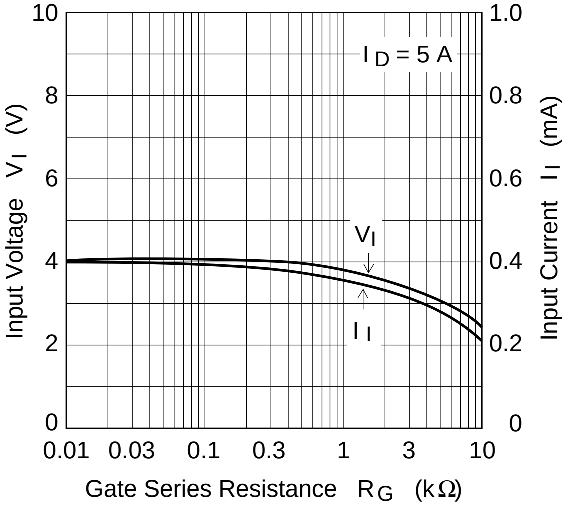
Gate to Source Voltage vs.
Shutdown Time of Load–Short Test



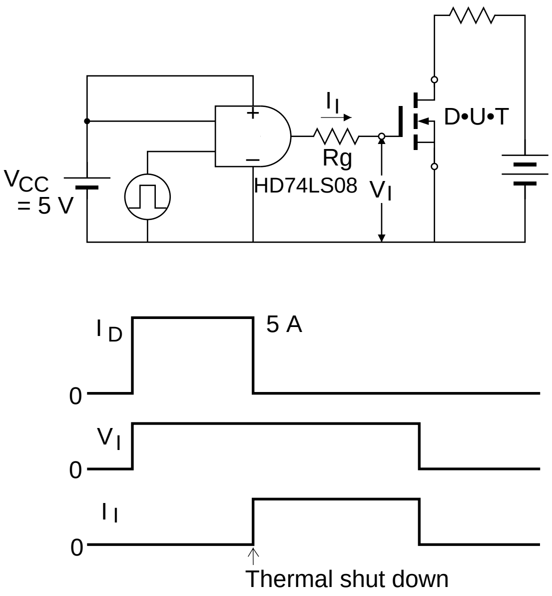
Shutdown Case Temperature vs.
Gate to Source Voltage



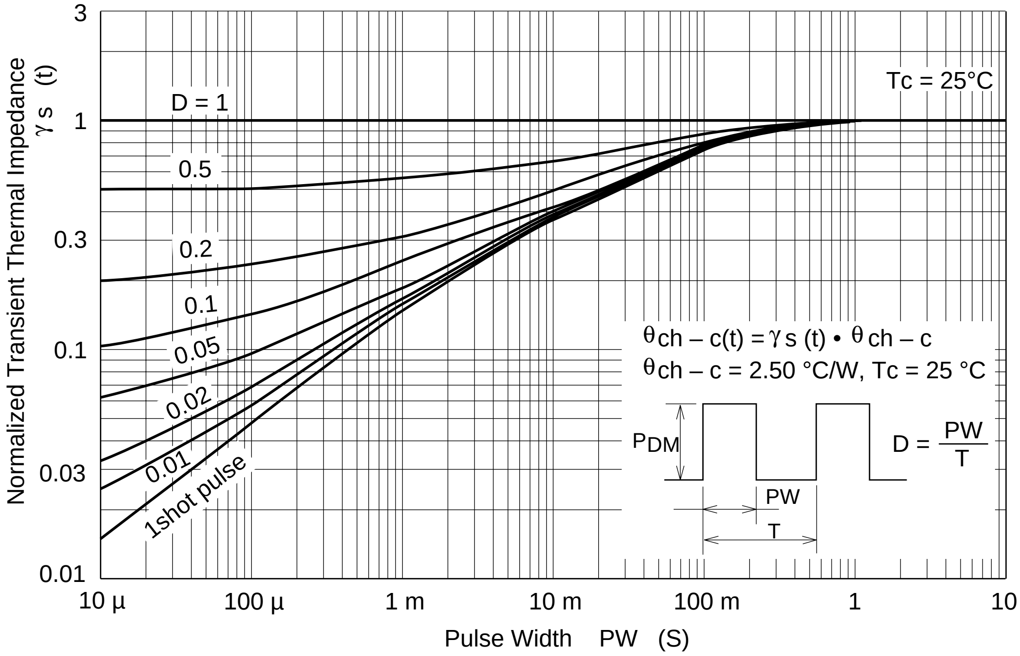
TTL Drive Characteristics



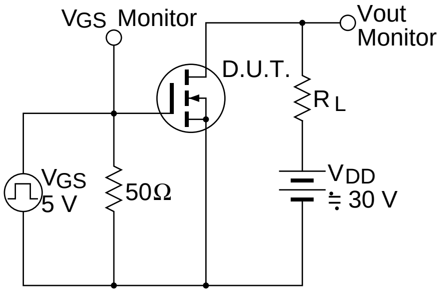
Test Circuit



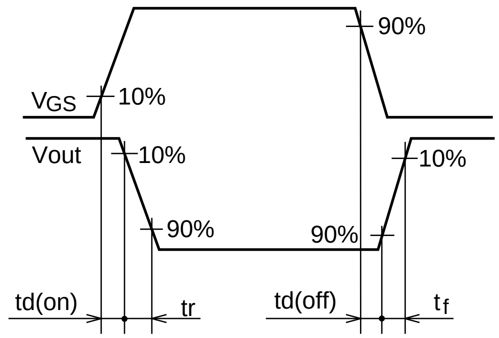
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



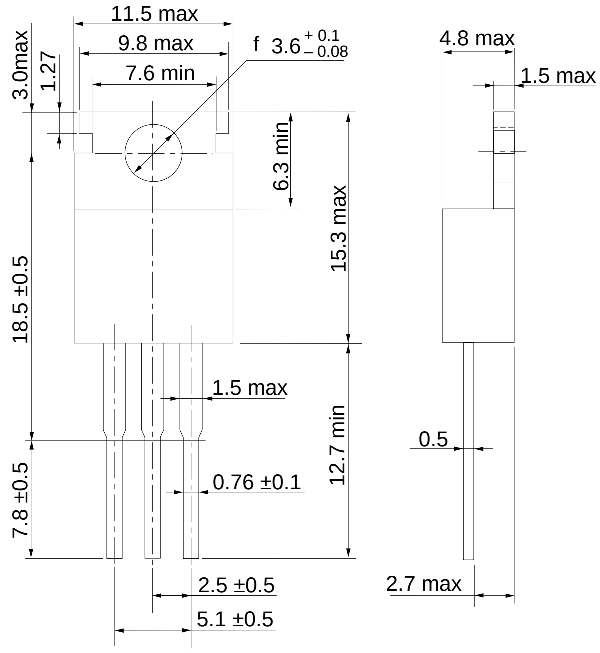
Waveform

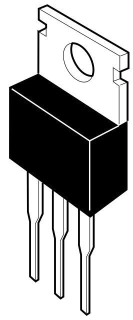


Package Dimensions

Unit : mm

- HDPAK





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EIAJ	SC–46
JEDEC	—