

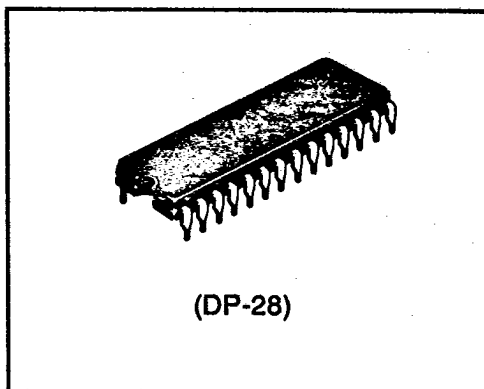
HD44007A

Sync Signal Generator for TV Cameras (NTSC, PAL/SECAM)

T-77-17

Functions

- Four times chroma sub-carrier oscillator frequency
- (B-Y) and (R-Y) chroma sub-carrier output circuit
- Active filter genlock phase detector
- Horizontal programmable logic array
- Vertical programmable logic array
- Horizontal/vertical programmable logic array



(DP-28)

Ordering Information

Type No.	Package
HD44007A	DP-28



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477

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T-77-17

Pin Description

Pin No.	Function	Note	Max Output Current
1	SC. BLK	Identification pulse for SECAM	+250 μ A
2	ID. P	Identification pulse for SECAM	+250 μ A
3	260 f _H /282 f _H osc	In	
4	260 f _H /282 f _H osc	Out	
5	Filter	Out	
6	Filter	In	
7	VD		$\pm$ 250 μ A
8	Camera HD		$\pm$ 500 μ A
9	Clamp P		$\pm$ 500 μ A
10	Composite BLK		$\pm$ 500 μ A
11	Burst flag P		$\pm$ 100 μ A
12	Beam BLK		$\pm$ 500 μ A
13	Black gate P		$\pm$ 500 μ A
14	V _{DD}	6.3 V to 7.0 V, typ 7.7 V	
15	HD		$\pm$ 500 μ A
16	Selector input	High level for NTSC, low level for PAL and SECAM	
17	External HD in	H genlock input	
18	Delayed HD		$\pm$ 500 μ A
19	Delayed VD in/out	In/out, output: V _{OH} $\geq$ 0.8 V _{DD} , V _{OL} = 0.5 V _{DD} , input threshold 0.25 V _{DD}	-500 μ A
20	Line SW in/out	In/out, pull-up resistor built-in	+250 μ A
21	Composite Sync		
22	Filter	In	
23	Filter	Out	
24	4 f _{SC} osc	In	
25	4 f _{SC} osc	Out	
26	SC (90°/270°)	For NTSC, 90° only (high level at pin 16)	$\pm$ 100 μ A
27	SC (180°)		$\pm$ 100 μ A
28	GND		

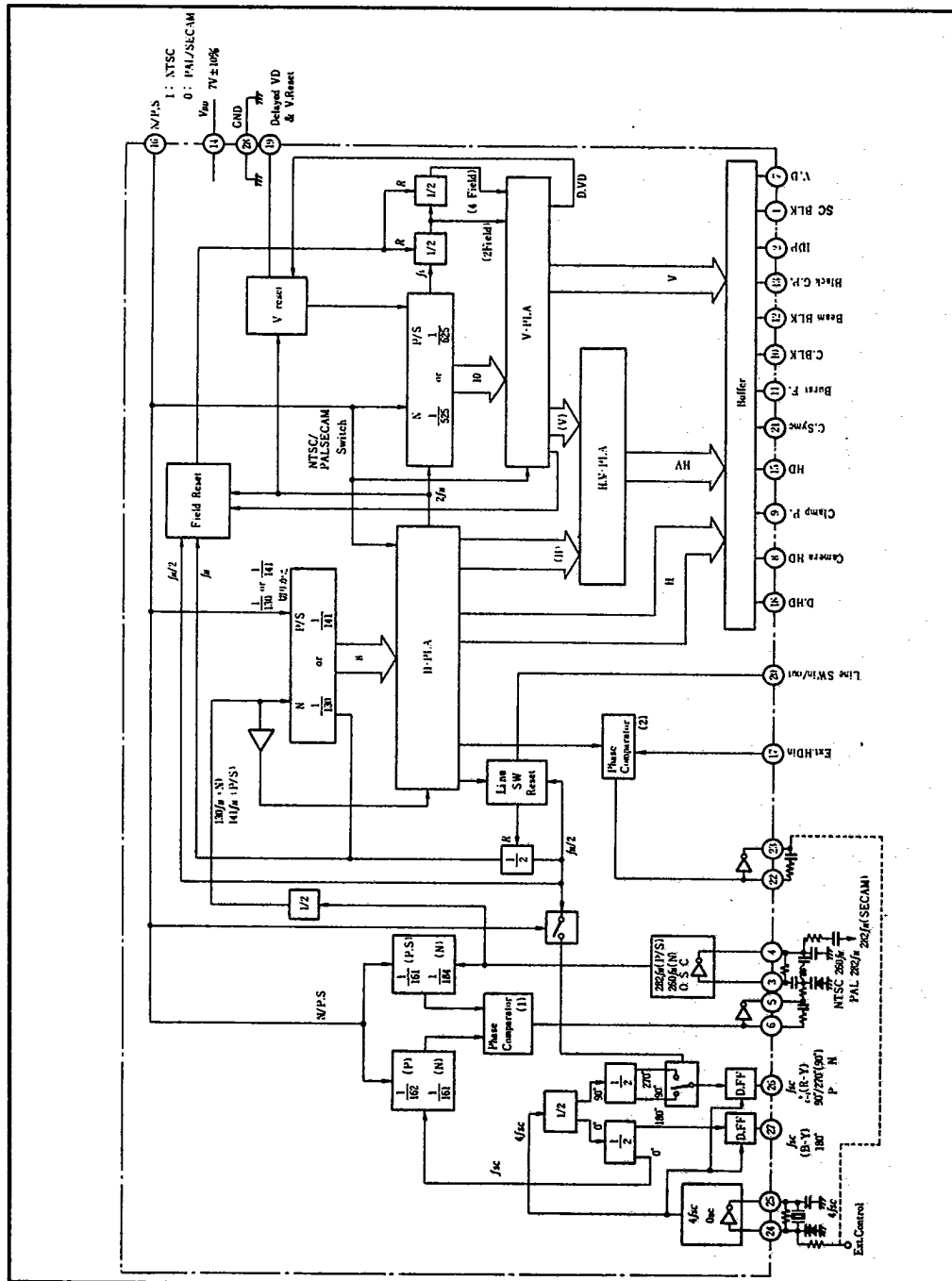


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Block Diagram



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Operations

Interleave (external HS input, pin 17 and phase comparator 2 are not used.) See figures 1 and 2.

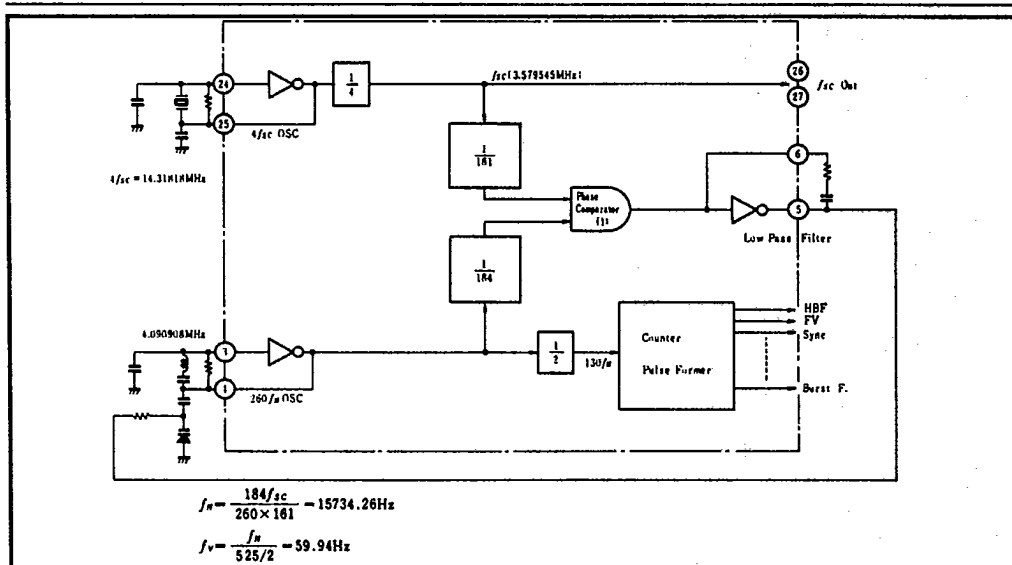


Figure 1 NTSC

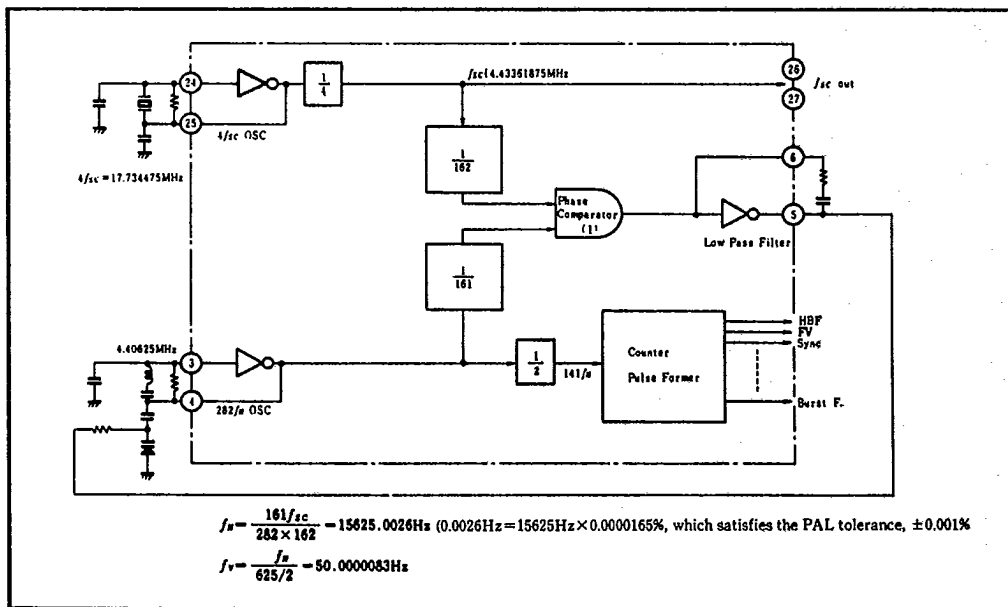


Figure 2 PAL, SECAM



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Genlock

In genlock mode, the operating principles of NTSC and PAL/SECAM are the same, so only NTSC is described below. See figure 3.

Phase comparator 1 is not used. See figure 4.

T-77-17

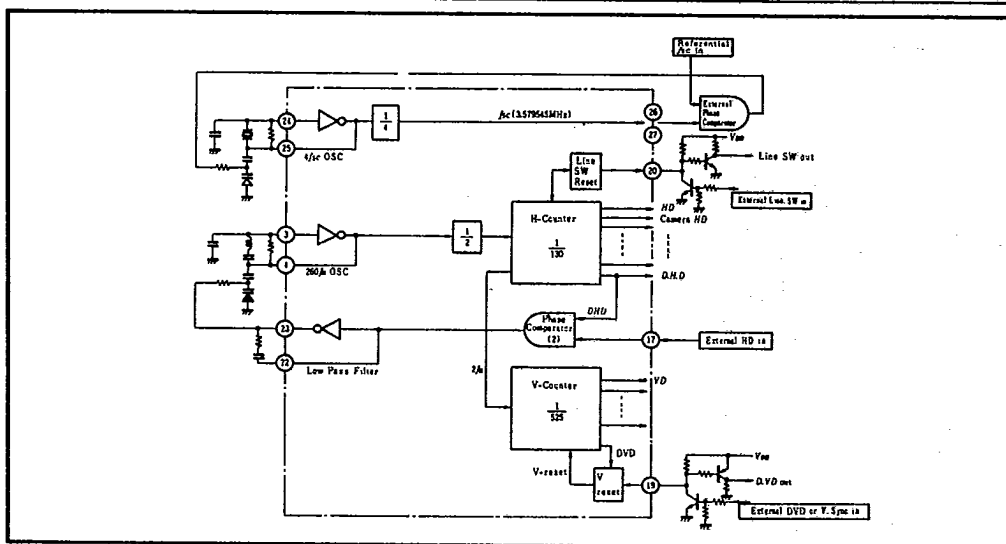


Figure 3 Genlock in Color Cameras

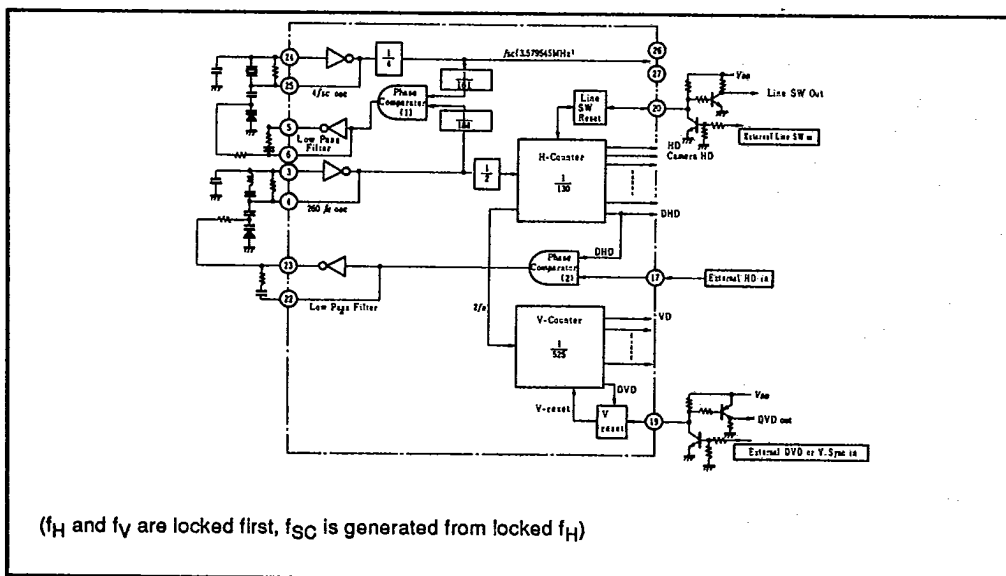


Figure 4 Genlock in B/W Cameras



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481

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T-77-17

Special Input/Output Terminals

Pin 20 is for line SW input and output (figure 5). Figure 6 shows the internal circuit and IC operation. The LC oscillator uses a CMOS inverter and crystal oscillator. There is no internal DC

feedback resistor, so an external resistor for feedback should be connected, as in figure 7.

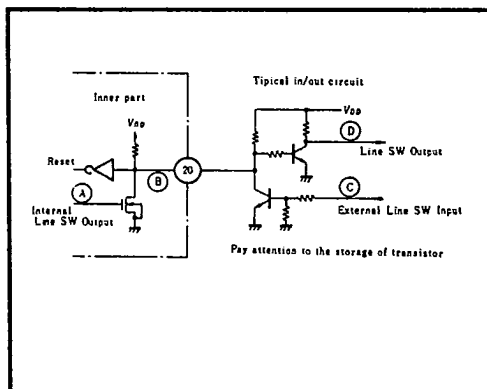


Figure 5 Pin 20 (Line SW In/Out)

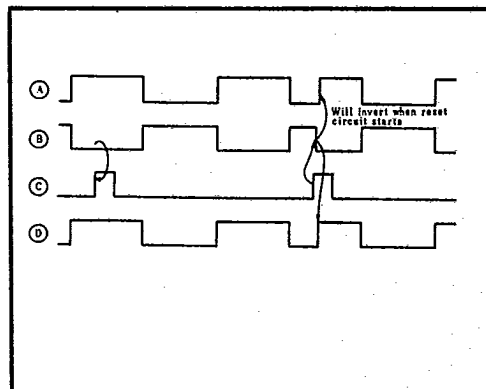
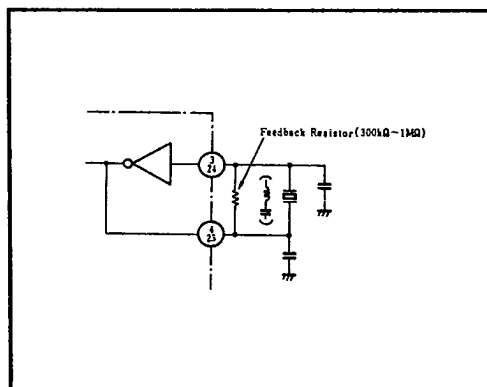


Figure 6 Internal Circuit and IC Operation

Figure 7 Pins 3, 4 and 24, 25 ($260 f_H/282 f_H$ osc, $4 f_{SC}$ osc)

Pin 19 is for VD output and V reset input. Figure 8 shows the internal circuit and IC operation. Output impedance is $500\ \Omega$ to $2\ \text{k}\Omega$ when pin 19 output is $V_{DD}/2$.

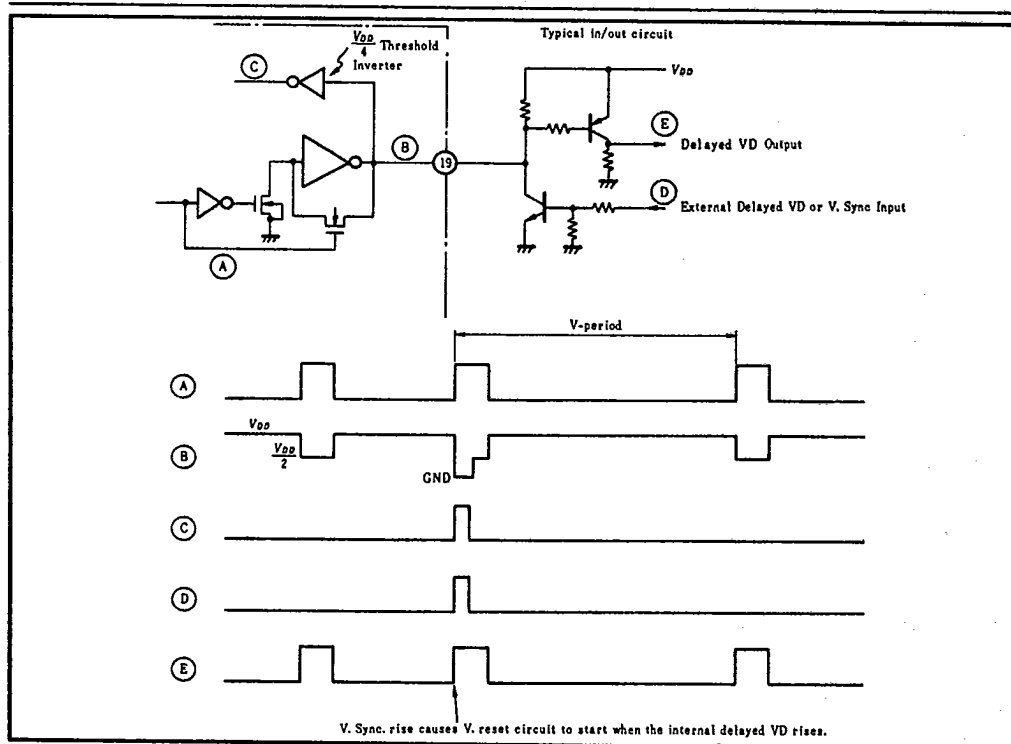


Figure 8 Pin 19, Delayed VD In/Out



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HD44007A**T-77-17****Absolute Maximum Ratings** ($T_a = 25^\circ\text{C}$)

Item	Symbol	Rating	Unit
Supply Voltage	V_{DD}	10	V
Input Voltage	V_{IN}	-0.3 to $V_{DD} + 0.3$	V
Power Dissipation ($T_a = 85^\circ\text{C}$)	P_T	450	mW
Operating Temperature	T_{opr}	-30 to +85	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +125	$^\circ\text{C}$

Electrical Characteristics ($T_a = 25^\circ\text{C}$)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Operating Supply Voltage	V_{DD}	6.3	7.0	7.7	V	
Supply Current	I_{DD}	—	—	40	mA	Output pins open, under oscillation
Input Voltage	V_{IH}	0.8 V _{p-p}	—	$V_{DD} + 0.3$	V	Pins 16, 17, and 20
	V_{IL}	-0.3	—	0.2 V_{DD}	V	
Input Threshold Voltage	V_{IH}	0.2 V_{DD}	0.25 V_{DD}	0.3 V_{DD}	V	Pin 19
Output Voltage	V_{OH}	0.8 V_{DD}	—	—	V	Pins 11, 26, and 27, $I_{OH} = -100 \mu\text{A}$
		0.8 V_{DD}	—	—	V	Pins 1, 2, and 7, $I_{OH} = -250 \mu\text{A}$
		0.8 V_{DD}	—	—	V	Pins 8, 9, 10, 12, 13, 15, 18, 19 and 21, $I_{OH} = -500 \mu\text{A}$
	V_{OL}	—	—	0.2 V_{DD}	V	Pins 11, 26, and 27, $I_{OL} = 100 \mu\text{A}$
		—	—	0.2 V_{DD}	V	Pins 1, 2, 7, and 20, $I_{OL} = 250 \mu\text{A}$
		—	—	0.2 V_{DD}	V	Pins 8, 9, 10, 12, 13, 15, 18, and 21, $I_{OL} = 500 \mu\text{A}$
		0.4 V_{DD}	0.5 V_{DD}	0.6 V_{DD}	V	Pin 19, open
Output Impedance	Z_{out}	500	1000	2000	Ω	Low output level at pin 19
Pull-Up Resistance	I_R	-200	-100	-50	μA	High output level at pin 20, pin 20 grounded



HD44007A

T-77-17

Electrical Characteristics (cont)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Maximum Clock Pulse Frequency	$f_{C \max}$	20	—	—	MHz	$V_{DD} = 6.3 \text{ V}$, 20 MHz crystal resonator between pins 24 and 25, output at pins 26 and 27 (20/4 = 5 MHz output)
Maximum Divider Operating Frequency	$f_{D \max}$	5.0	—	—	MHz	$V_{DD} = 6.3 \text{ V}$, LC between pins 3 and 4, normal oscillation frequency at output terminal
Pin 26 Output Phase Angle (NTSC)	ϕ_N	88	90	92	deg	Pin 26 output phase referred to 180° (= pin 27 output phase), pin 16: V_{DD} , $V_{DD} = 6.3\text{--}7.7 \text{ V}$
Pin 26 Output Phase Angle (PAL 1)	ϕ_{P1}	88	90	92	deg	Pin 26 output phase referred to 180° (= pin 27 output phase), pin 16: GND, high level line output
Pin 26 Output Phase Angle (PAL 2)	ϕ_{P2}	268	270	272	deg	Pin 26 output phase referred to 180° (= pin 27 output phase), pin 16: GND, low level line output



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485

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T-77-17

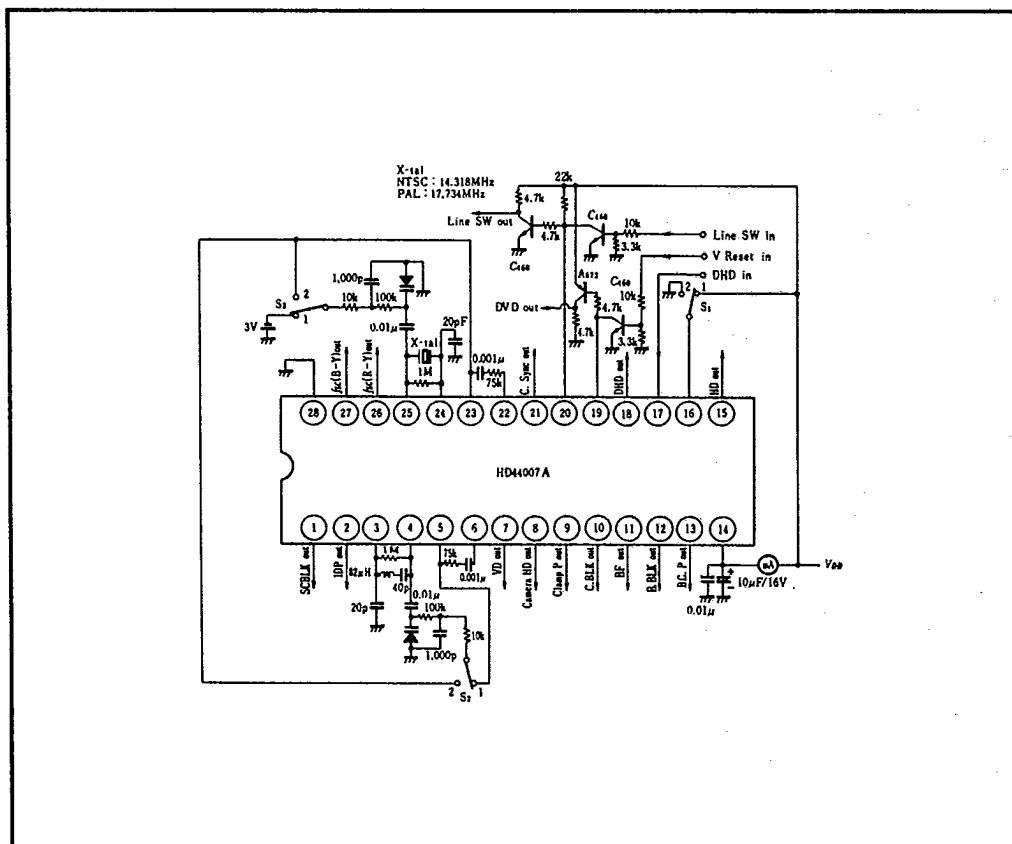


Figure 9 Test Circuit

Table 1 Test Circuit

	S ₂	S ₃
Interleave	1	1
Genlock	2	2

	S ₁	x-tal
NTSC	1	14.318 MHz
PAL/SECAM	2	17.734 MHz



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Timing Charts

T-77-17

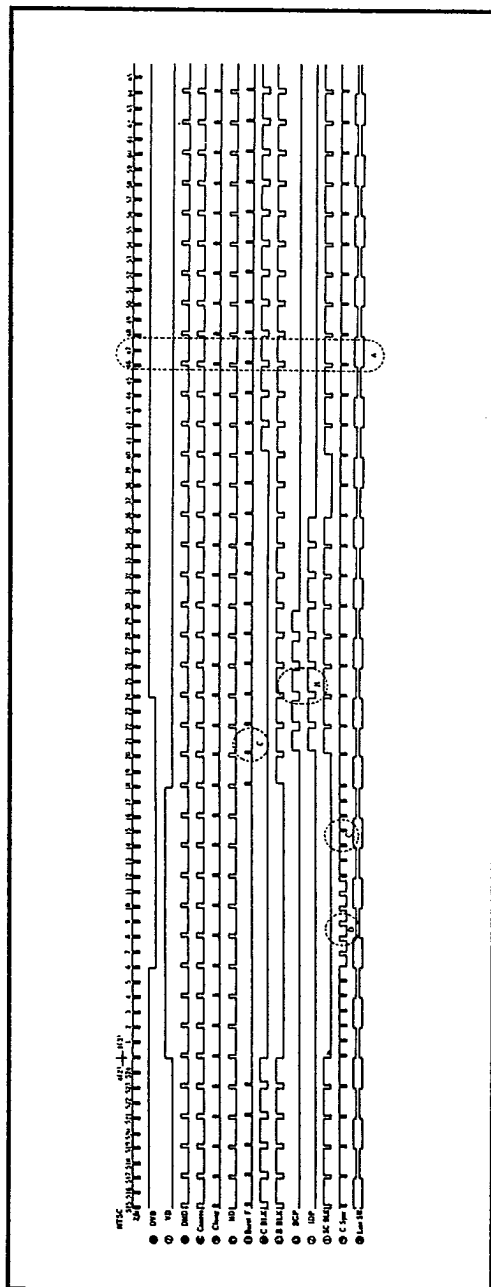


Figure 10 Timing Chart 1

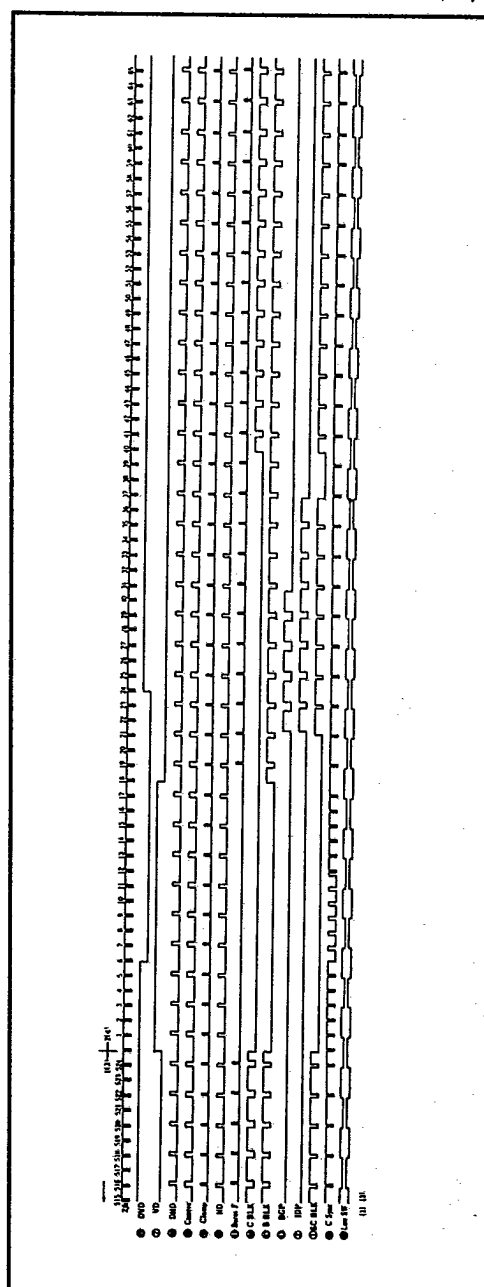


Figure 11 Timing Chart 2



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487

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T-77-17

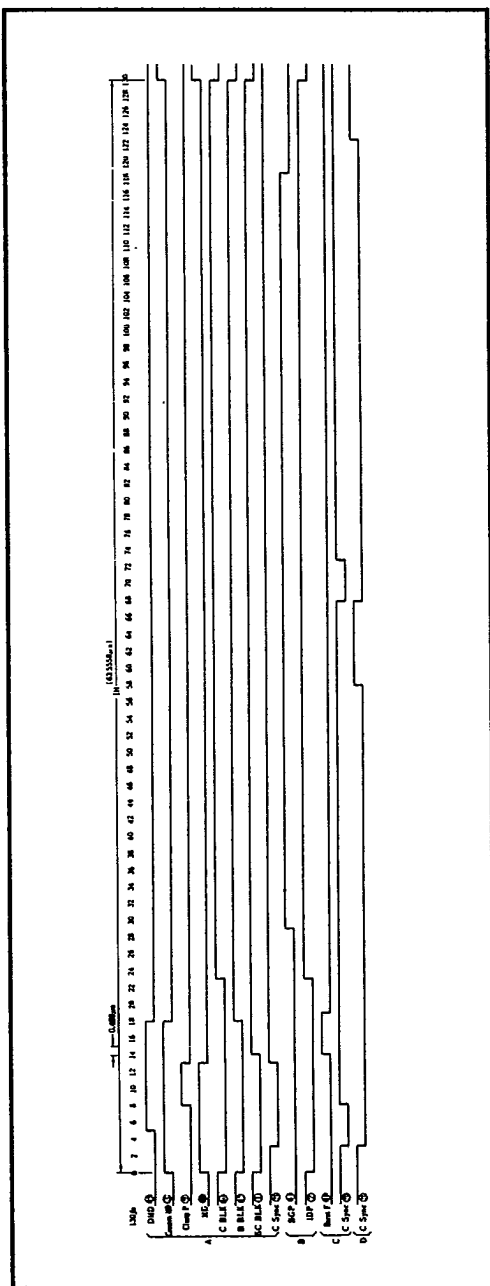


Figure 12 Timing Chart 3

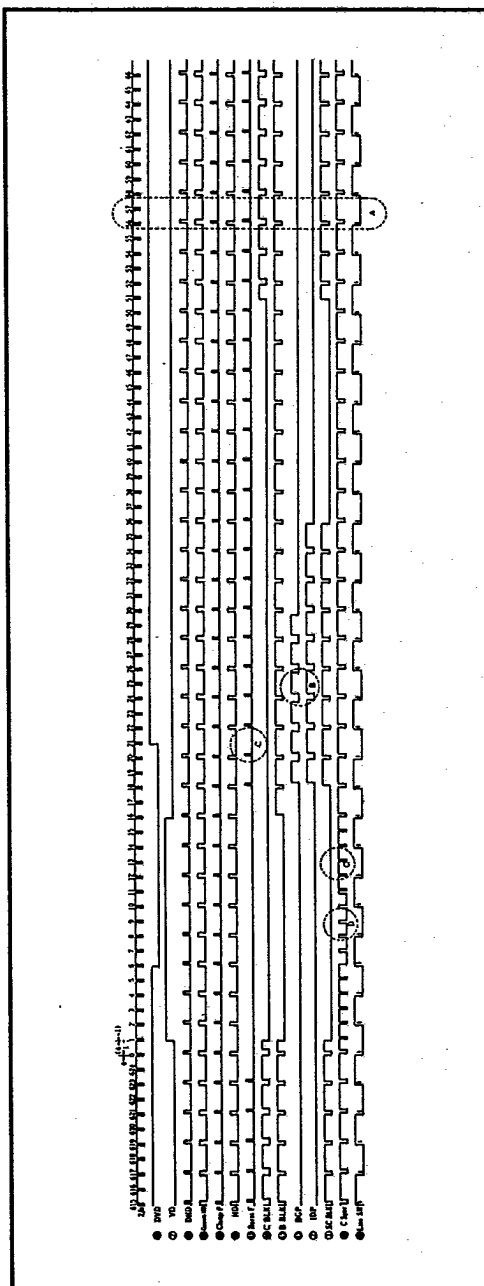


Figure 13 Timing Chart 4



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T-77-17

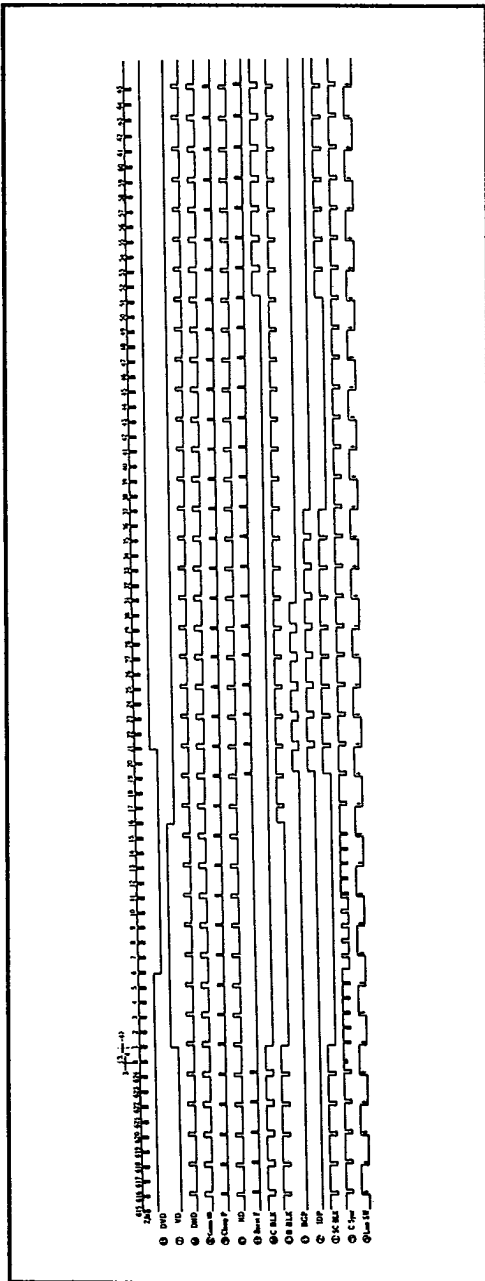


Figure 16 Timing Chart 7

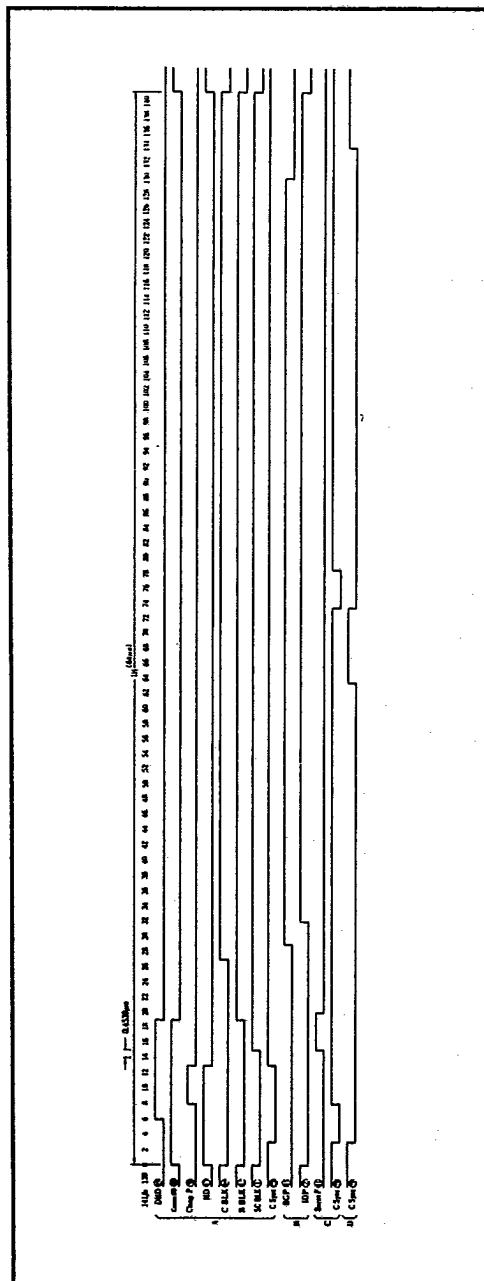


Figure 17 Timing Chart 8



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