HD64645/HD64646

LCTC (LCD Timing Controller)

HITACHI

ADE-207-276(Z)
'99.9
Rev. 0.0

Description

The HD64645/HD64646 LCTC is a control LSI for large size dot matrix liquid crystal displays. The LCTC is software compatible with the HD6845 CRTC, since its programming method of internal registers and memory addresses is based on the CRTC. A display system can be easily converted from a CRT to an LCD.

The HD64646 LCTC is a modified version of the HD64645 LCTC with different LCD interface timing.

The LCTC offers a variety of functions and performance features such as vertical and horizontal scrolling, and various types of character attribute functions such as reverse video, blinking, nondisplay (white or black), and an OR function for simple superimposition of character and graphic displays. The LCTC also provides DRAM refresh address output.

A compact LCD system with a large screen can be configured by connecting the LCTC with the HD66110ST (column driver) and the HD66113T (common driver) by utilizing 4-bit × 2 data outputs. Power dissipation has been lowered by adopting the CMOS process.

Features

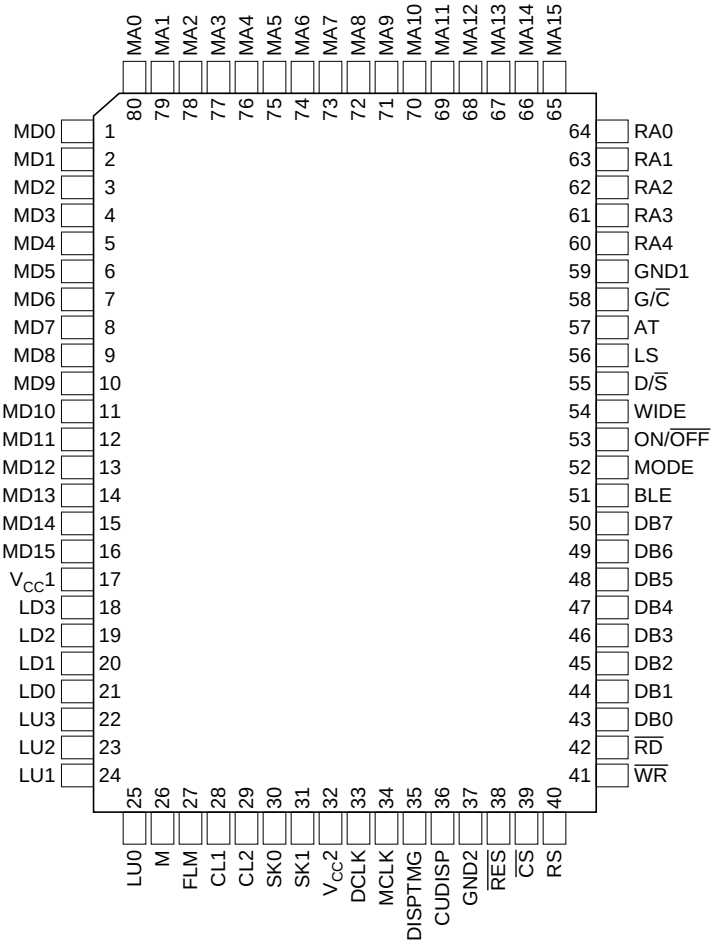
- Software compatible with the HD6845 CRTC
- Programmable screen size
  - — Up to 1024 dots (height)
  - — Up to 4096 dots (width)
- High-speed data transfer
  - — Up to 20 Mbits/s in character mode
  - — Up to 40 Mbits/s in graphic mode
- Selectable single or dual screen configuration
- Programmable multiplexing duty ratio: static to 1/512 duty cycle
- Programmable character font
  - — 1-32 dots (height)
  - — 8 dots (width)

- Versatile character attributes: reverse video, blinking, nondisplay (white), nondisplay (black)
- OR function: superimposing characters and graphics display
- Cursor with programmable height, blink rate, display position, and on/off switch
- Vertical Smooth Scrolling and horizontal scrolling by the character
- Versatile display modes programmable by mode register or external pins: display on/off, graphic or character, normal or wide, attributes, and blink enable
- Refresh address output for dynamic RAM
- 4- or 8-bit parallel data transfer between LCTC and LCD driver
- Recommended LCD driver
  - HD66110ST and HD66120 (segment)
  - HD66113T and HD66115T (common)
- CPU interface
  - 80 family
- CMOS process
- Single +5 V ±10%

Ordering Information

Type No.	Package
HD64645F	80-pin plastic QFP (FP-80)
HD64646FS	80-pin plastic QFP (FP-80B)

Pin Arrangement



(Top view)

Pin Description

Symbol	Pin Number	I/O	Name
$V_{cc}1$, $V_{cc}2$	17, 32	—	V_{cc}
GND1, GND2	37, 59	—	Ground
LU0–LU3	22–25	O	LCD up panel data 0–3
LD0–LD3	18–21	O	LCD down panel data 0–3
CL1	28	O	Clock one
CL2	29	O	Clock two
FLM	27	O	First line marker
M	26	O	M
MA0–MA15	65–80	O	Memory address 0–15
RA0–RA4	60–64	O	Raster address 0–4
MD0–MD7	1–8	I	Memory Data 0–7
MD8–MD15	9–16	I	Memory Data 8–15
DB0–DB7	43–50	I/O	Data bus 0–7
$\overline{CS}$	39	I	Chip select
$\overline{WR}$	41	I	Write
$\overline{RD}$	42	I	Read
RS	40	I	Register select
$\overline{RES}$	38	I	Reset
DCLK	33	I	D clock
MCLK	34	O	M clock
DISPTMG	35	O	Display timing
CUDISP	36	O	Cursor display
SK0	30	I	Skew 0
SK1	31	I	Skew 1
ON/$\overline{OFF}$	53	I	On/off
BLE	51	I	Blink enable
AT	57	I	Attribute
G/$\overline{C}$	58	I	Graphic/character
WIDE	54	I	Wide
LS	56	I	Large screen
D/$\overline{S}$	55	I	Dual/single
MODE	52	I	Mode

Pin Functions

Power Supply ($V_{CC}1$, $V_{CC}2$, GND)

Power Supply Pin (+5 V): Connect $V_{CC}1$ and $V_{CC}2$ with +5V power supply circuit.

Ground Pin (0 V): Connect GND1 and GND2 with 0V.

LCD Interface

LCD Up Panel Data (LU0–LU3), LCD Down Panel Data (LD0–LD3): LU0–LU3 and LD0–LD3 output LCD data as shown in Table 1.

Clock One (CL1): CL1 supplies timing clocks for display data latch.

Clock Two (CL2): CL2 supplies timing clock for display data shift.

First Line Marker (FLM): FLM supplies first line marker.

M (M): M converts liquid crystal drive output to AC.

Memory Interface

Memory Address (MA0–MA15): MA0–MA15 supply the display memory address.

Raster Address (RA0–RA4): RA0–RA4 supply the raster address.

Memory Data (MD0–MD7): MD0–MD7 receive the character dot data or bit-mapped data.

Memory Data (MD8–MD15): MD8–MD15 receive attribute code data or bit-mapped data.

MPU Interface

Data Bus (DB0–DB7): DB0–DB7 send/receive data as a three-state I/O common bus.

Chip Select ($\overline{CS}$): $\overline{CS}$ selects a chip. Low level enables MPU read/write of the LCTC internal registers.

Write ($\overline{WR}$): $\overline{WR}$ receives MPU write strobe.

Read ($\overline{RD}$): $\overline{RD}$ receives MPU read strobe.

Register Select (RS): RS selects registers. (Refer to Table 4.)

Reset ($\overline{RES}$): $\overline{RES}$ performs external reset of the LCTC. Low level of $\overline{RES}$ stops and zero-clears the LCTC internal counter. No register contents are affected.

Timing Signal

D Clock (DCLK): DCLK inputs the system clock.

M Clock (MCLK): MCLK indicates memory cycle; DCLK is divided by four.

Display Timing (DISPTMG): DISPTMG high indicates that the LCTC is reading display data.

Cursor Display (CUDISP): CUDISP supplies cursor display timing; connect with MD12 in character mode.

Skew 0 (SK0)/Skew 1 (SK1): SK0 and SK1 control skew timing. Refer to Table 2.

Mode Select

The mode select pins ON/$\overline{\text{OFF}}$, BLE, AT, G/$\overline{\text{C}}$, and WIDE are ORed with the mode register (R22) to determine the mode.

On/Off (ON/$\overline{\text{OFF}}$): ON/$\overline{\text{OFF}}$ switches display on and off (high = display on).

Blink Enable (BLE): BLE high level enables attribute code "blinking" (MD13) and provides normal/blank blinking of specified characters for 32 frames each.

Attribute (AT): AT controls character attribute functions.

Graphic/Character (G/$\overline{\text{C}}$): G/$\overline{\text{C}}$ switches between graphic and character display mode (graphic display when high).

Wide (WIDE): WIDE switches between normal and wide display mode (high = wide display, low = normal display).

Large Screen (LS): LS controls a large screen. LS high provides a data transfer rate of 40 Mbits/s for a graphic display. Also used to specify 8-bit LCD interface mode. For more details, refer to Table 10.

Dual/Single (D/$\overline{\text{S}}$): D/$\overline{\text{S}}$ switches between single and dual screen display (dual screen display when high).

Mode (MODE): MODE controls easy mode. MODE high sets duty ratio, maximum number of rasters, cursor start/end rasters, etc. (Refer to Table 8.)

Table 1 LCD Up Panel Data and LCD Down Panel Data

	Single Screen		
Pin Name	**4-Bit Data**	**8-Bit Data**	**Dual Screen**
LU0–LU3	Data output	Data output	Data output for upper screen
LD0–LD3	Disconnected	Data output	Data output for lower screen

Table 2 Skew Signals

SK0	SK1	Skew Function
0	0	No skew
1	0	1-character time skew
0	1	2-character time skew
1	1	Prohibited combination

Function Overview

Main Features of HD64645/HD64646

Main features of the LCTC are:

- High-resolution liquid crystal display screen control (up to 720 × 512 dots)
- Software compatible with HD6845 (CRTC)
- Built-in character attribute control circuit

Table 3 shows how the LCTC can be used.

Table 3 Functions, Application, and Configuration

Classification	Item	Description
Functions	Screen format	• Programmable horizontal scanning cycle by the character clock period • Programmable multiplexing duty ratio from static up to 1/512 • Programmable number of vertical displayed characters • Programmable number of rasters per character row (number of vertical dots within a character row + space between character rows)
	Cursor control	• Programmable cursor display position, corresponding to RAM address • Programmable cursor height by setting display start/end rasters • Programmable blink rate, 1/32 or 1/64 frame rate
	Memory rewriting	• Time for rewriting memory set either by specifying number of horizontal total characters or by cycle steal utilizing MCLK
	Memory addressing	• 16-bit memory address output, up to 64 kbytes $\times$ 2 memory accessible • DRAM refresh address output
	Paging and scrolling	• Paging by updating start address • Horizontal scrolling by the character, by setting horizontal virtual screen width • Vertical smooth scrolling by updating display start raster
	Character attributes	• Reverse video, blinking, nondisplay (white or black), display ON/OFF
Application	CRTC compatible	• Facilitates system replacement of CRT display with LCD
	OR function	• Enables superimposing display of character screen and graphic screen
Configuration	LCTC configuration	• Single 5 V power supply • I/O TTL compatible except $\overline{\text{RES}}$, MODE, SK0, SK1 • Bus connectable with 80 family • CMOS process • Internal logic fully static • 80-pin flat plastic package

Differences between HD64645 and HD64646

Figure 1 and Figure 2 show the relation between display data transfer period, when display data shift clock CL2 changes, and display data latch clock CL1. Figure 1 shows the case without skew function and Figure 2 shows the case with skew function.

In Figure 1, high period between CL2 and CL1 of HD64645 overlap. HD64646 has no overlap like HD64645, and except for this overlap, HD64646 is the same as HD64645 functionally.

Also for the skew function, phase relation between CL1 and CL2 changes. As Figure 2 shows, data transfer period and CL1 high period of HD64646 never overlap with the skew function.

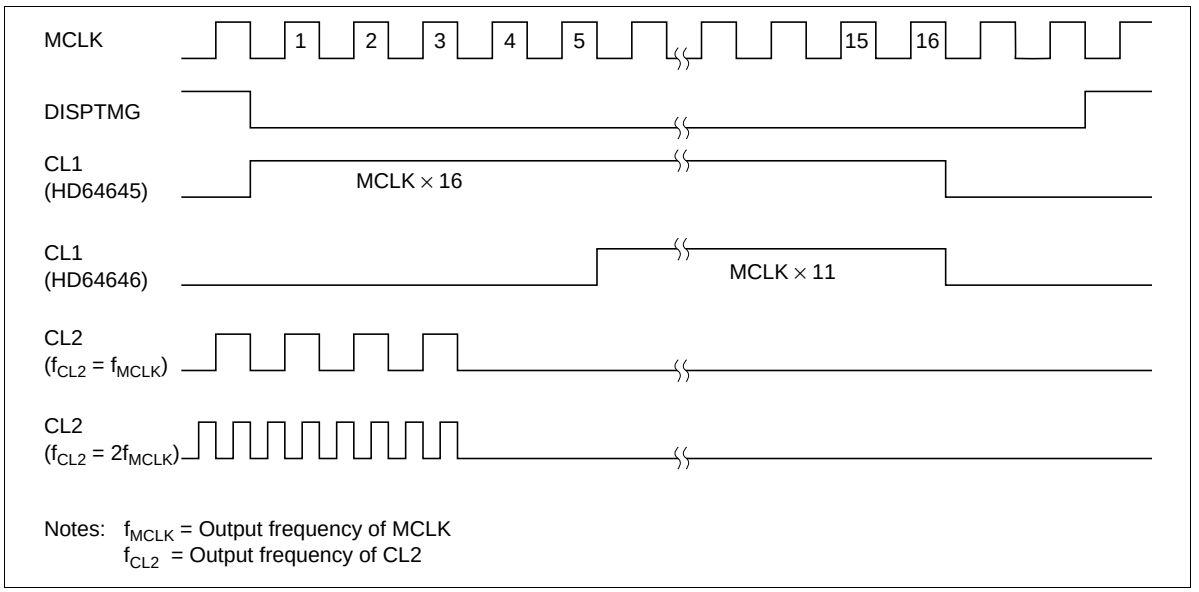


Figure 1 Differences between HD64645 and HD64646 (No Skew)

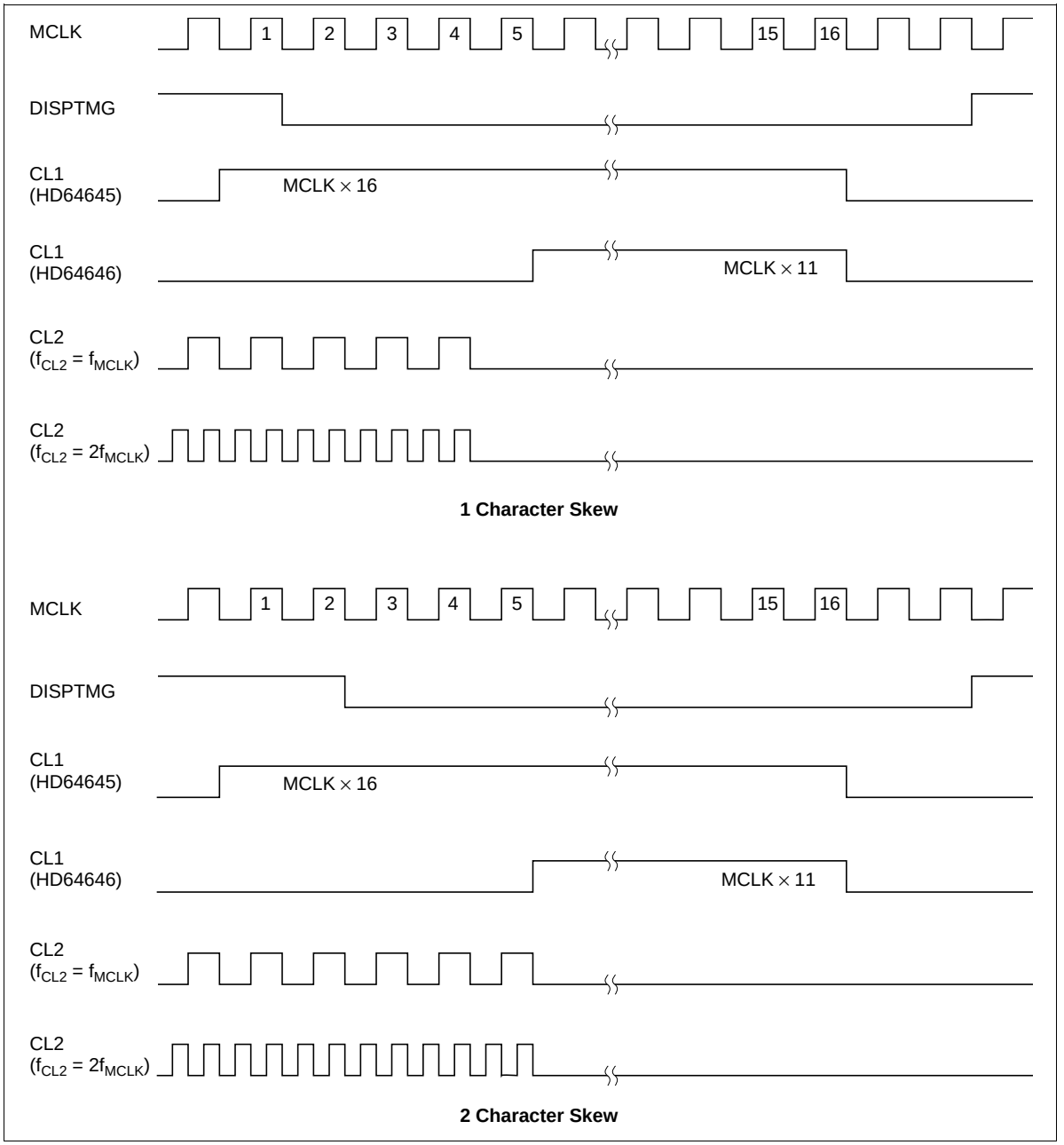


Figure 2 Differences between HD64645 and HD64646 (Skew)

Internal Block Diagram

Figure 3 is a block diagram of the LCTC.

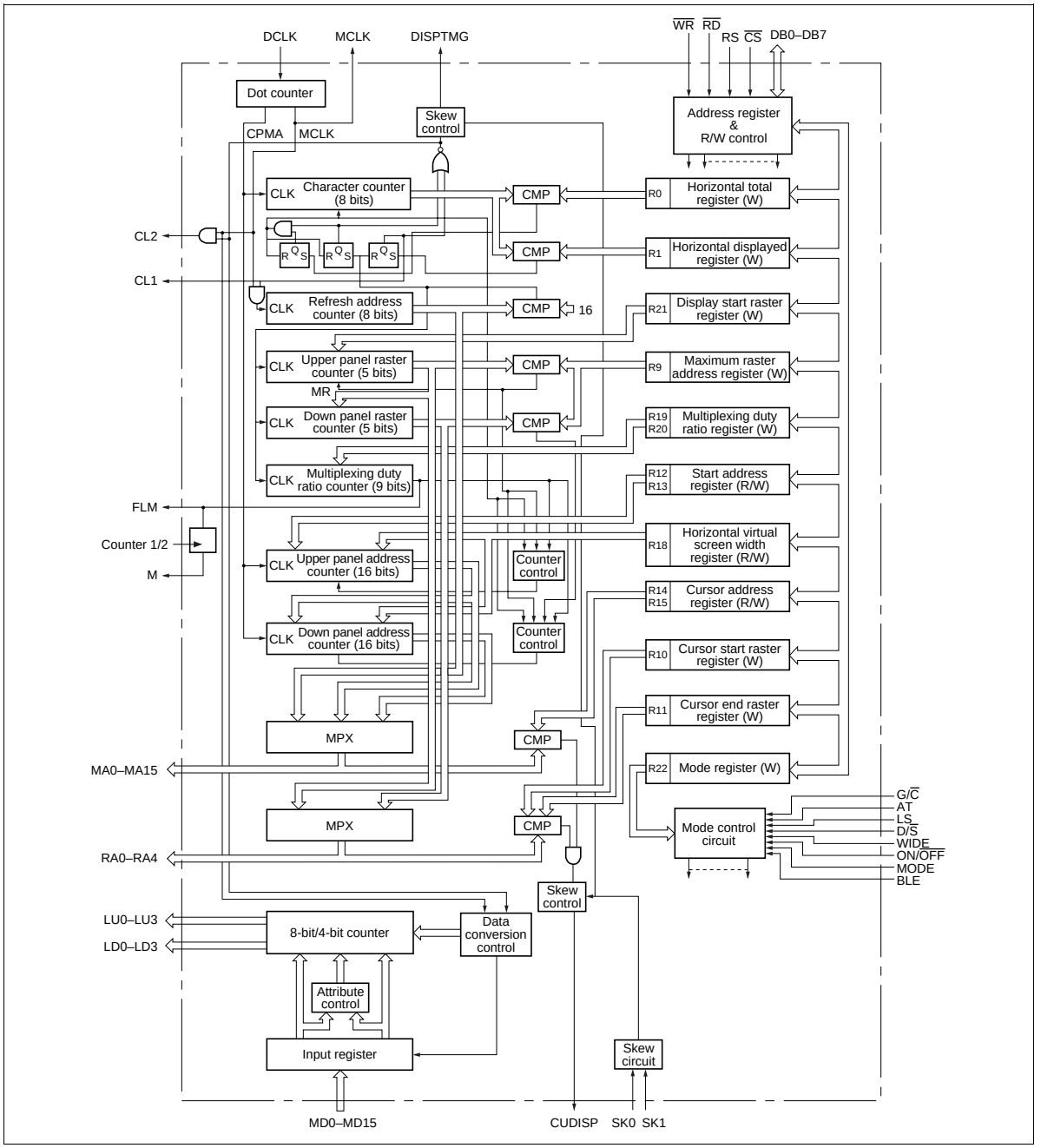


Figure 3 LCTC Block Diagram

System Block Configuration Examples

Figure 4 is a block diagram of a character/graphic display system. Figure 6 shows two examples using LCD drivers.

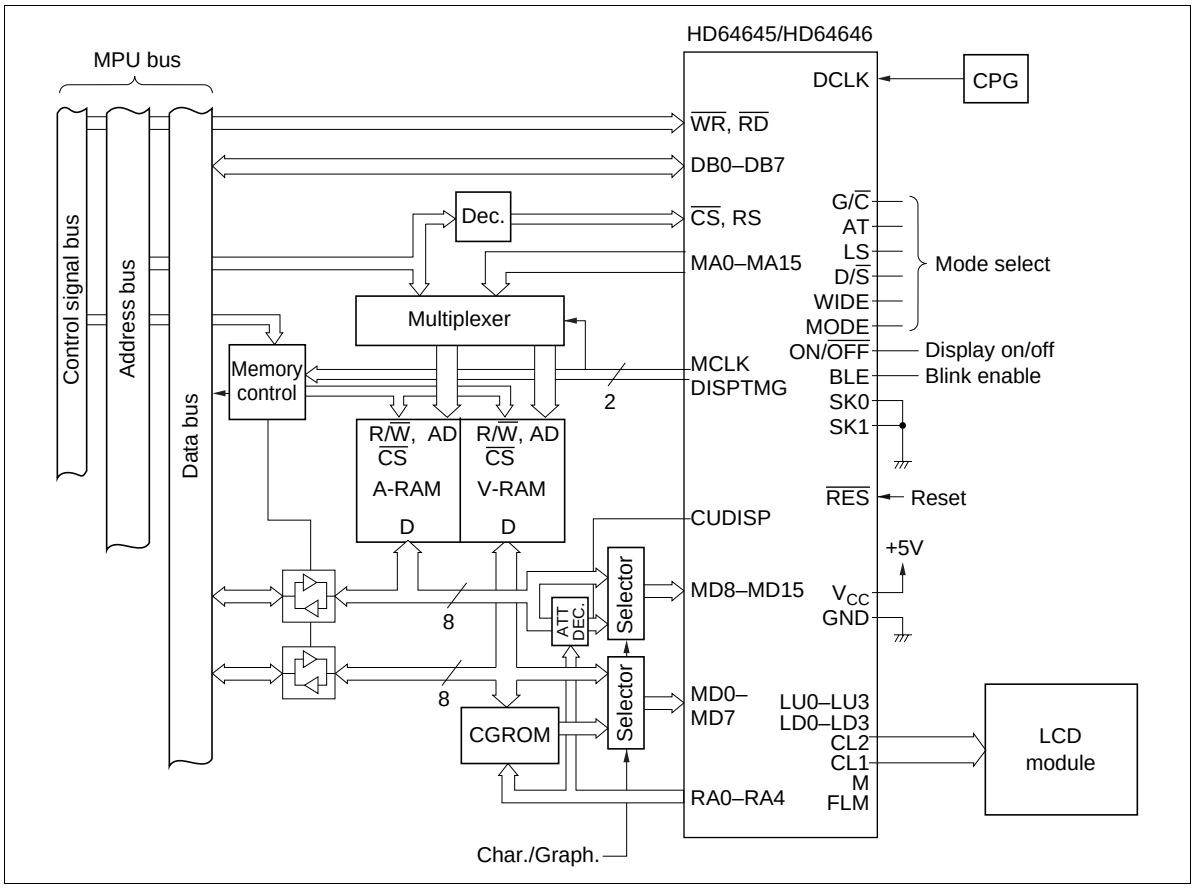
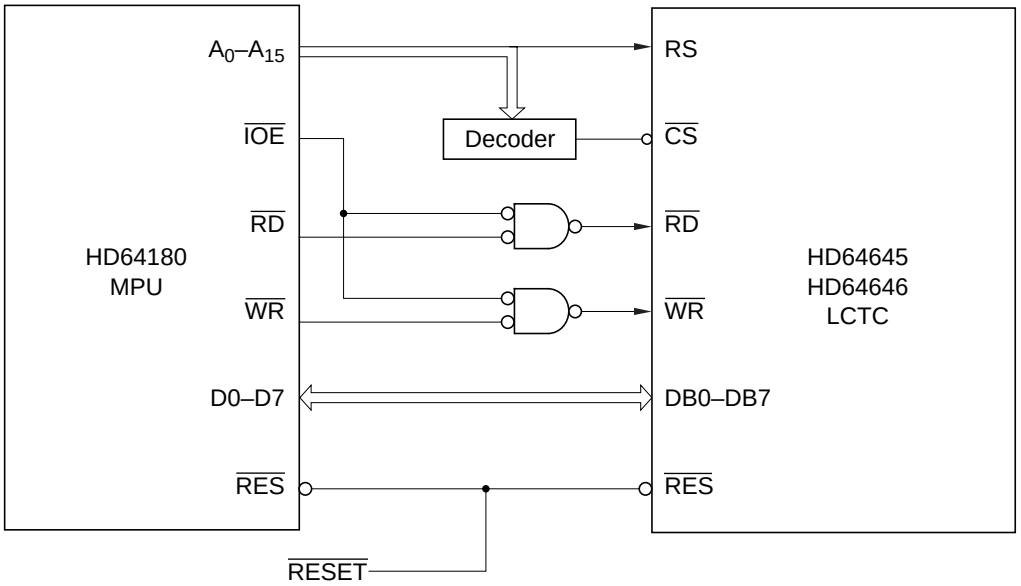


Figure 4 Character/Graphic Display System Example

Interface to MPU



Note: In 80 family MPUs, I/O space is separate from memory space in software. Thus the LCTC, a part of I/O, needs the ORed signals of the interface signals and IOE. So $\overline{IOE}$ and $\overline{RD}$, and $\overline{IOE}$ and $\overline{WR}$ should be ORed to satisfy t_{AS}, the timing of $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$.

Interface between HD64180, HD64645 and HD64646

Figure 5 Interfacep to MPU

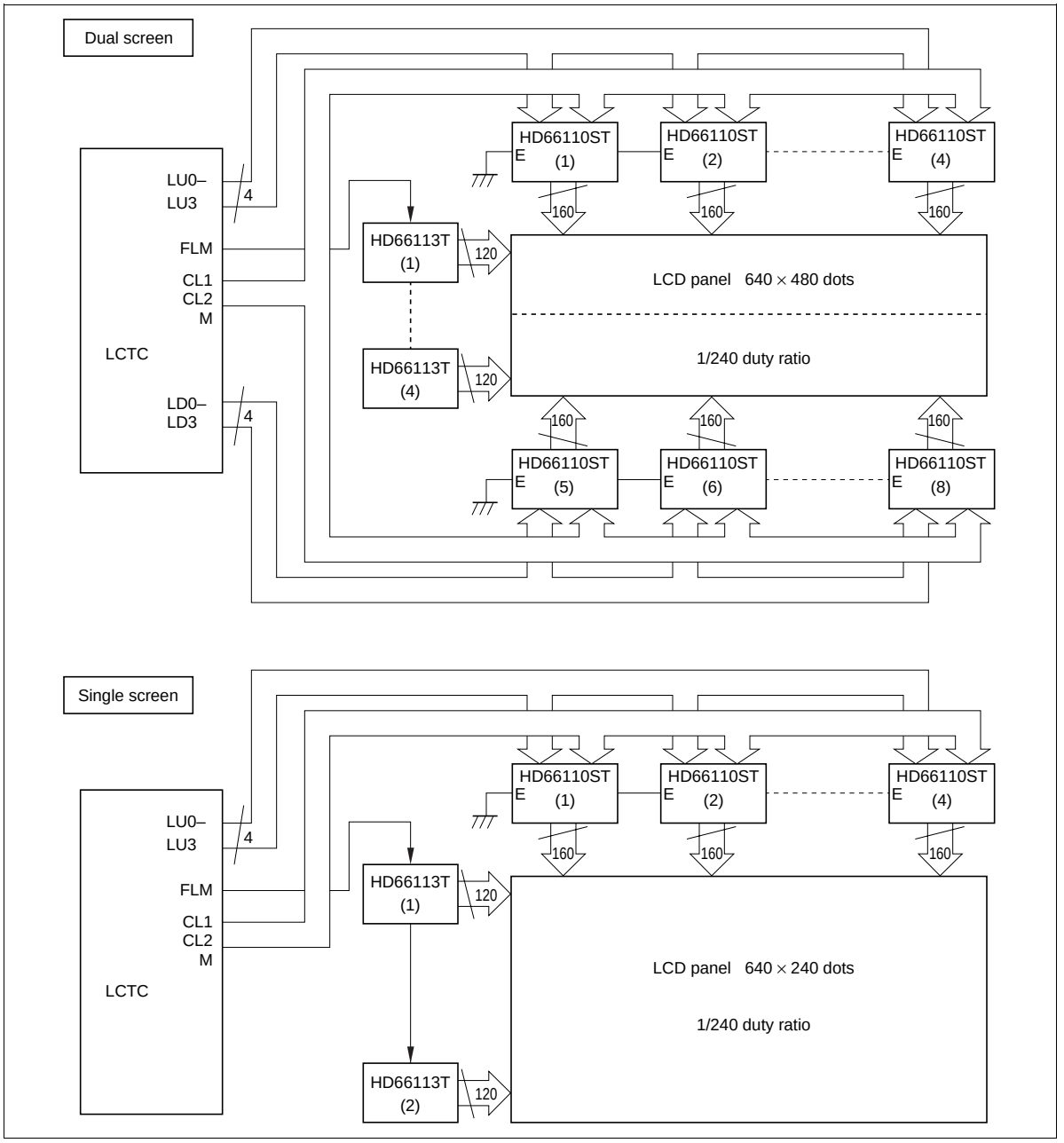


Figure 6 LCD Driver Examples

Registers

Table 4 shows the register mapping. Table 5 describes their function. Table 6 shows the differences between CRTC and LCTC registers.

Table 4 Registers Mapping

		Address Register					Reg.				Data Bit							
$\overline{CS}$	RS	4	3	2	1	0	No.	Register Name	Program Unit	Symbol	R/W	7	6	5	4	3	2	1	0
1	—	—	—	—	—	—		Invalid	—	—	—								
0	0	—	—	—	—	—	AR	Address Register	—	—	W								
0	1	0	0	0	0	0	R0	Horizontal total characters	Character*3	Nht	W								
0	1	0	0	0	0	1	R1	Horizontal displayed char.s	Character	Nhd	W								
0	1	0	1	0	0	1	R9	Maximum raster address	Raster	Nr	W								
0	1	0	1	0	1	0	R10	Cursor start raster	Raster*4	Ncs	W		B	P					
0	1	0	1	0	1	1	R11	Cursor end raster	Raster	Nce	W								
0	1	0	1	1	0	0	R12	Start address (H)	Memory address	—	R/W								
0	1	0	1	1	0	1	R13	Start address (L)	Memory address	—	R/W								
0	1	0	1	1	1	0	R14	Cursor address (H)	Memory address	—	R/W								
0	1	0	1	1	1	1	R15	Cursor address (L)	Memory address	—	R/W								
0	1	1	0	0	1	0	R18	Horizontal virtual screen width	Character	Nir	W								
0	1	1	0	0	1	1	R19	Multiplexing duty ratio (H)	Raster*3	Ndh	W								
0	1	1	0	1	0	0	R20	Multiplexing duty ratio (L)	Raster*3	Ndl	W								
0	1	1	0	1	0	1	R21	Display start raster	Raster	Nsr	W								
0	1	1	0	1	1	0	R22	Mode register	—*5	—	W				ON/ OFF	G/C	WIDE	BLE	AT

Notes: 1. ▭: Invalid data bits

2. R/W indicates whether write access or read access is enabled to/from each register.
   W: Only write accessible
   R/W: Both read and write accessible
3. The “value to be specified minus 1” should be programmed in these registers: R0, R1 and R20.
4. Data bits 5 and 6 of cursor start register control the cursor status as shown below (for more details, refer to page 27).

B	P	Cursor Blink Mode
0	0	Cursor on; without blinking
0	1	Cursor off
1	0	Blinking once every 32 frames
1	1	Blinking once every 64 frames

5. The OR of mode pin status and mode register data determines the mode.
6. Registers R2–R8, R16, and R17 are not assigned for the LCTC. Programming to these registers will be ignored.

Table 5 Internal Register Description

Reg. No.	Register Name	Size (Bits)	Description
AR	Address register	5	Specifies the internal control registers (R0, R1, R9–R15, R18–R22) address to be accessed
R0	Horizontal total characters	8	Specifies the horizontal scanning period
R1	Horizontal displayed characters	8	Specifies the number of displayed characters per character row
R9	Maximum raster address	5	Specifies the number of rasters per character row, including the space between character rows
R10	Cursor start raster	5 + 2	Specifies the cursor start raster address and its blink mode
R11	Cursor end raster	5	Specifies the cursor end raster address
R12 R13	Start address (H) Start address (L)	16	Specify the display start address
R14 R15	Cursor address (H) Cursor address (L)	16	Specify the cursor display address
R18	Horizontal virtual screen width	8	Specifies the length of one row in memory space for horizontal scrolling
R19 R20	Multiplexing duty ratio (H) Multiplexing duty ratio (L)	9	Specify the number of rasters for one screen
R21	Display start raster	5	Specifies the display start raster within a character row for smooth scrolling
R22	Mode register	5	Controls the display mode

Note: For more details of registers, refer to “Internal Registers.”

Table 6 Internal Register Comparison between LCTC and CRTC

Reg. No.	LCTC HD64645/HD64646	Comparison	CRTC HD6845
AR	Address register	Equivalent to CRTC	Address register
R0	Horizontal total characters		Horizontal total characters
R1	Horizontal displayed characters		Horizontal displayed characters
R2	—	Particular to CRTC; unnecessary for LCTC	Horizontal sync position
R3			Sync width
R4			Vertical total characters
R5			Vertical total adjust
R6			Vertical displayed characters
R7			Vertical sync position
R8			Interface and skew
R9	Maximum raster address	Equivalent to CRTC	Maximum raster address
R10	Cursor start raster		Cursor start raster
R11	Cursor end raster		Cursor end raster
R12	Start address (H)		Start address (H)
R13	Start address (L)		Start address (L)
R14	Cursor address (H)		Cursor (H)
R15	Cursor address (L)		Cursor (L)
R16		Particular to CRTC; unnecessary for LCTC	Light pen (H)
R17			Light pen (L)
R18	Horizontal virtual screen width	Additional registers for LCTC	
R19	Multiplexing duty ratio (H)		
R20	Multiplexing duty ratio (L)		
R21	Display start raster		
R22	Mode register		

Functional Description

Programmable Screen Format

Figure 7 illustrates the relation between LCD display screen and registers. Figure 8 shows a timing chart of signals output from the LCTC in mode 5 as an example.

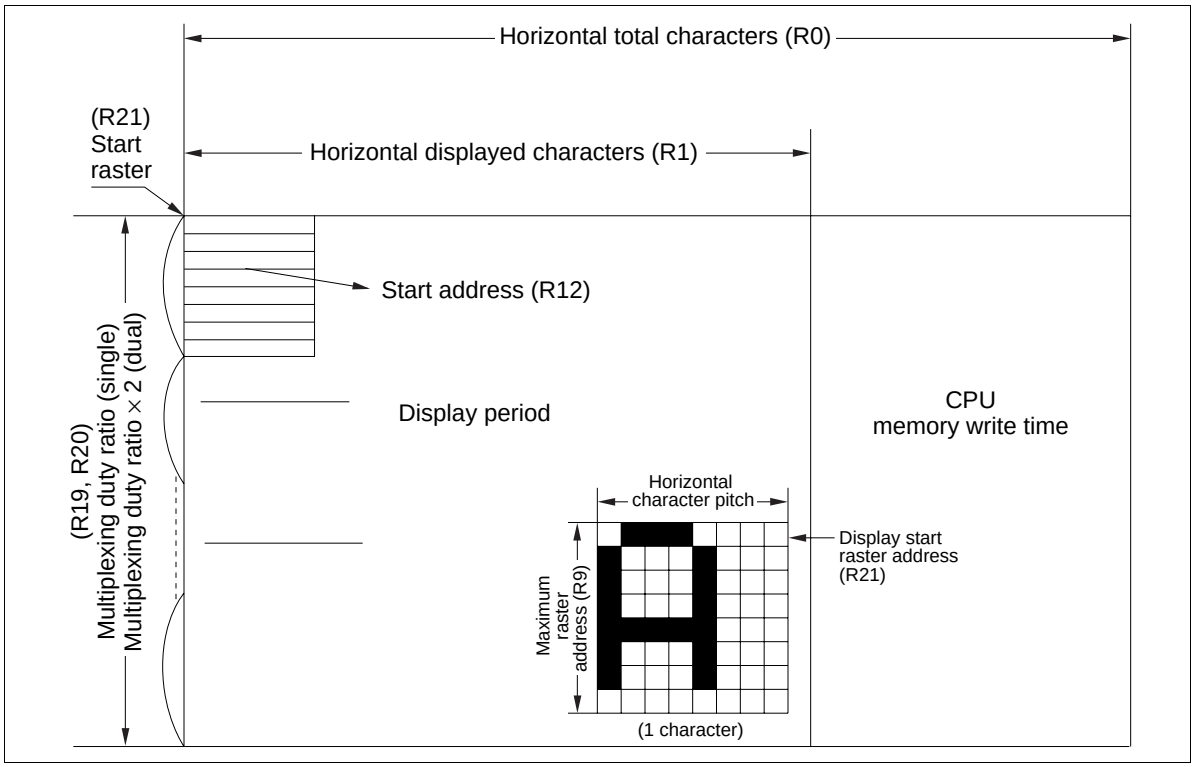
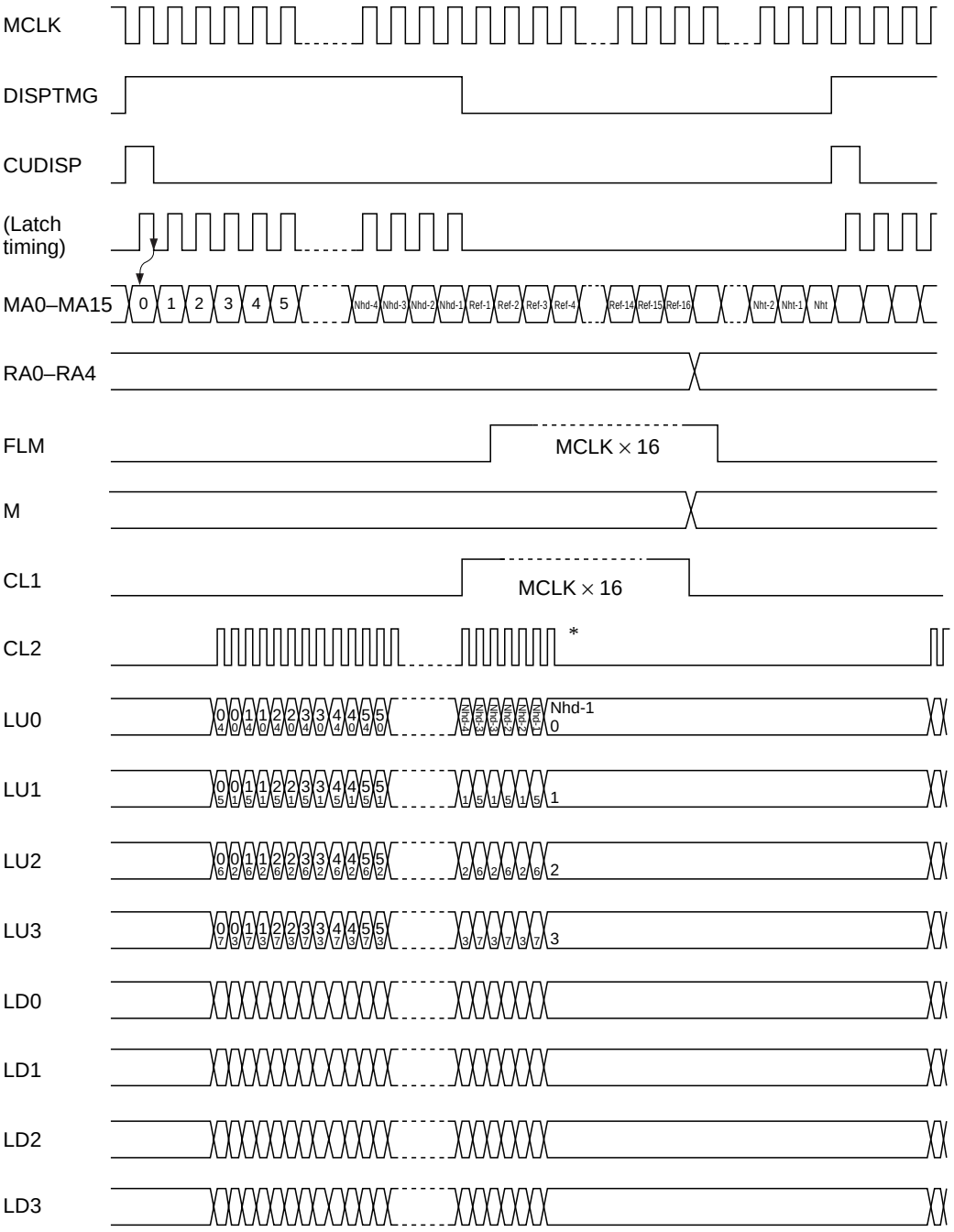


Figure 7 Relation between Display Screen and Registers



Note: * Relation between CL1 and CL2 in the case of HD64646 is difference from one shown in this chart. Refer to “Difference between HD64645 and HD64646.”

Figure 8 LCTC Timing Chart
(In Mode 5: Single Screen, 4-Bit Transfer, Normal Character Display)

Cursor Control

The following cursor functions (Figure 9) can be controlled by programming specific registers.

- Cursor display position
- Cursor height
- Cursor blink mode

A cursor can be displayed only in character mode. Also, CUDISP pin must be connected to MD12 pin to display a cursor.

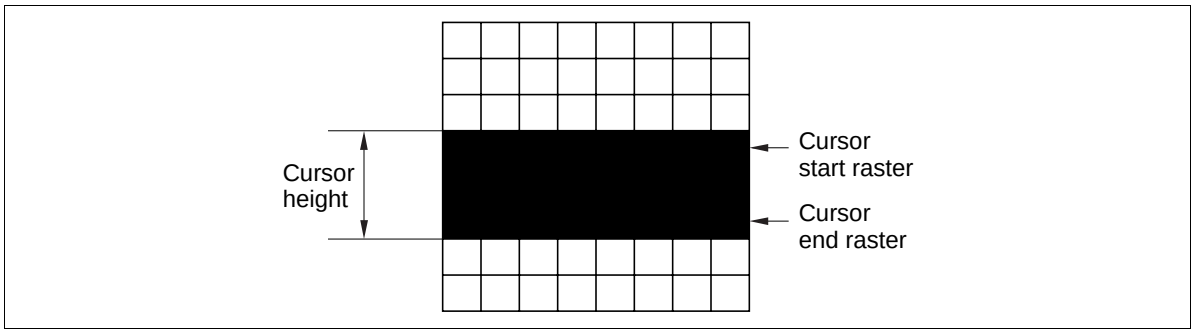


Figure 9 Cursor Display

Character Mode and Graphic Mode

The LCTC supports two types of display modes; character mode and graphic mode. Graphic mode 2 is provided to utilize software for a system using the CRTC (HD6845).

The display mode is controlled by an OR between the mode select pins (D/$\overline{S}$, G/$\overline{C}$, LS, WIDE, AT) and mode register (R22).

Character Mode: character mode displays characters by using CG-ROM. The display data supplied from memory is accessed in 8-bit units. A variety of character attribute functions are provided, such as reverse video, blinking, nondisplay (white or black), by storing the attribute data in attribute RAM (A-RAM).

Figure 10 illustrates the relation between character display screen and memory contents.

Graphic Mode 1: Graphic mode 1 directly displays data stored in a graphic memory buffer. The display data supplied from memory is accessed in 16-bit units. Character attribute functions or wide mode are not provided. Figure 11 illustrates the relation between graphic display screen and memory contents.

Graphic Mode 2: Graphic mode 2 utilizes software for a system using the CRTC (HD6845). The display data supplied from memory is accessed in 16-bit units. Character attribute functions or wide mode are not provided. The same memory addresses are output repeatedly the number of times specified by maximum raster register (R9). The raster address is output in the same way as in character mode.

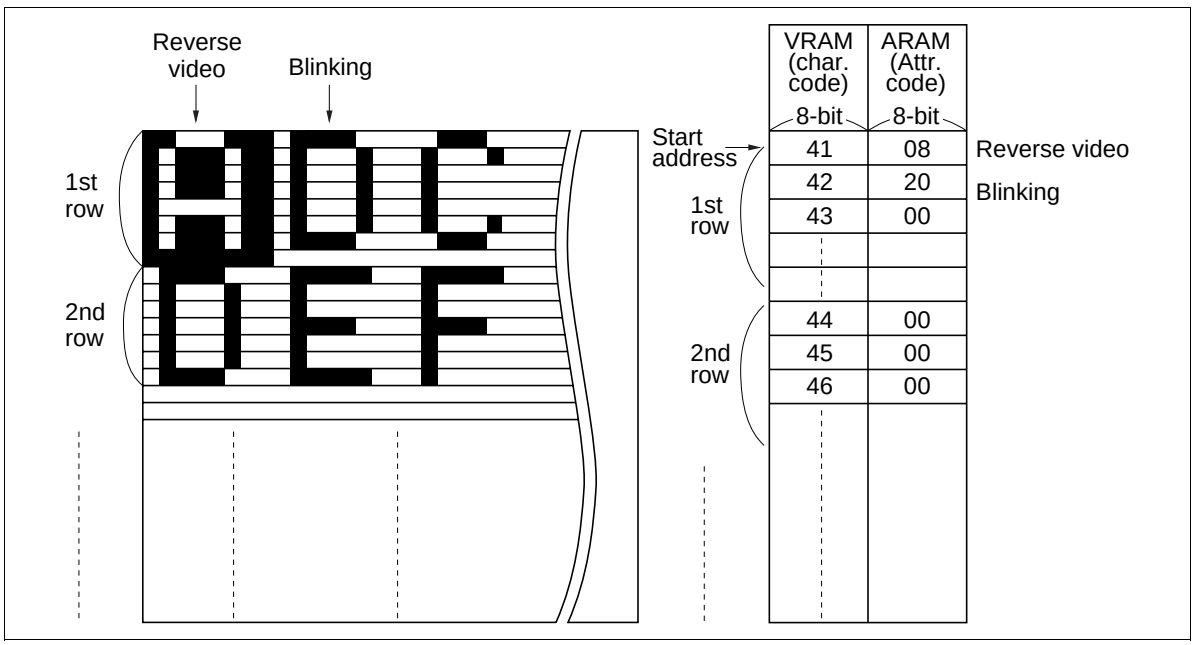


Figure 10 Relation between Character Screen and Memory Contents

Horizontal Virtual Screen Width

Horizontal virtual screen width can be specified by the character in addition to the number of horizontal displayed characters (Figure 12).

The display screen can be scrolled in any direction by the character, by setting the horizontal virtual screen width and updating the start address. This function is enabled by programming the horizontal virtual screen width register (R18).

Figure 13 shows an example.

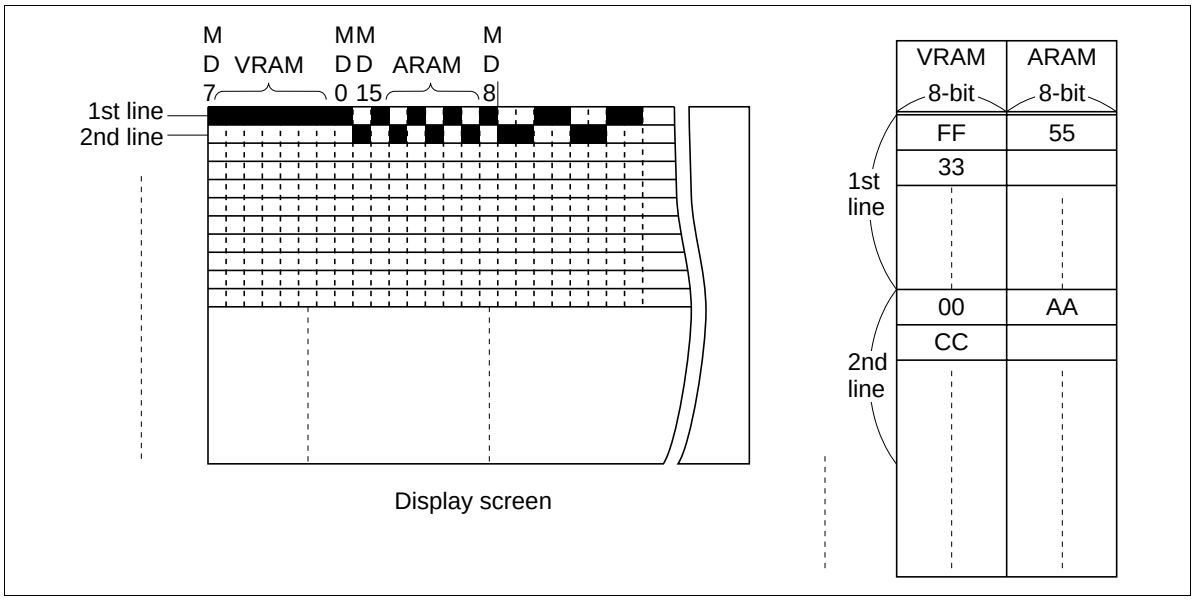


Figure 11 Relation between Graphic Screen and Memory Contents

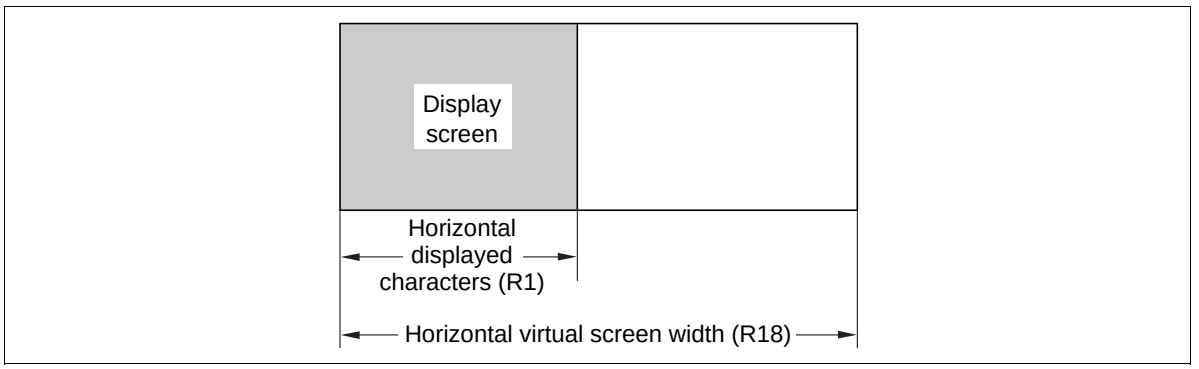


Figure 12 Horizontal Virtual Screen Width

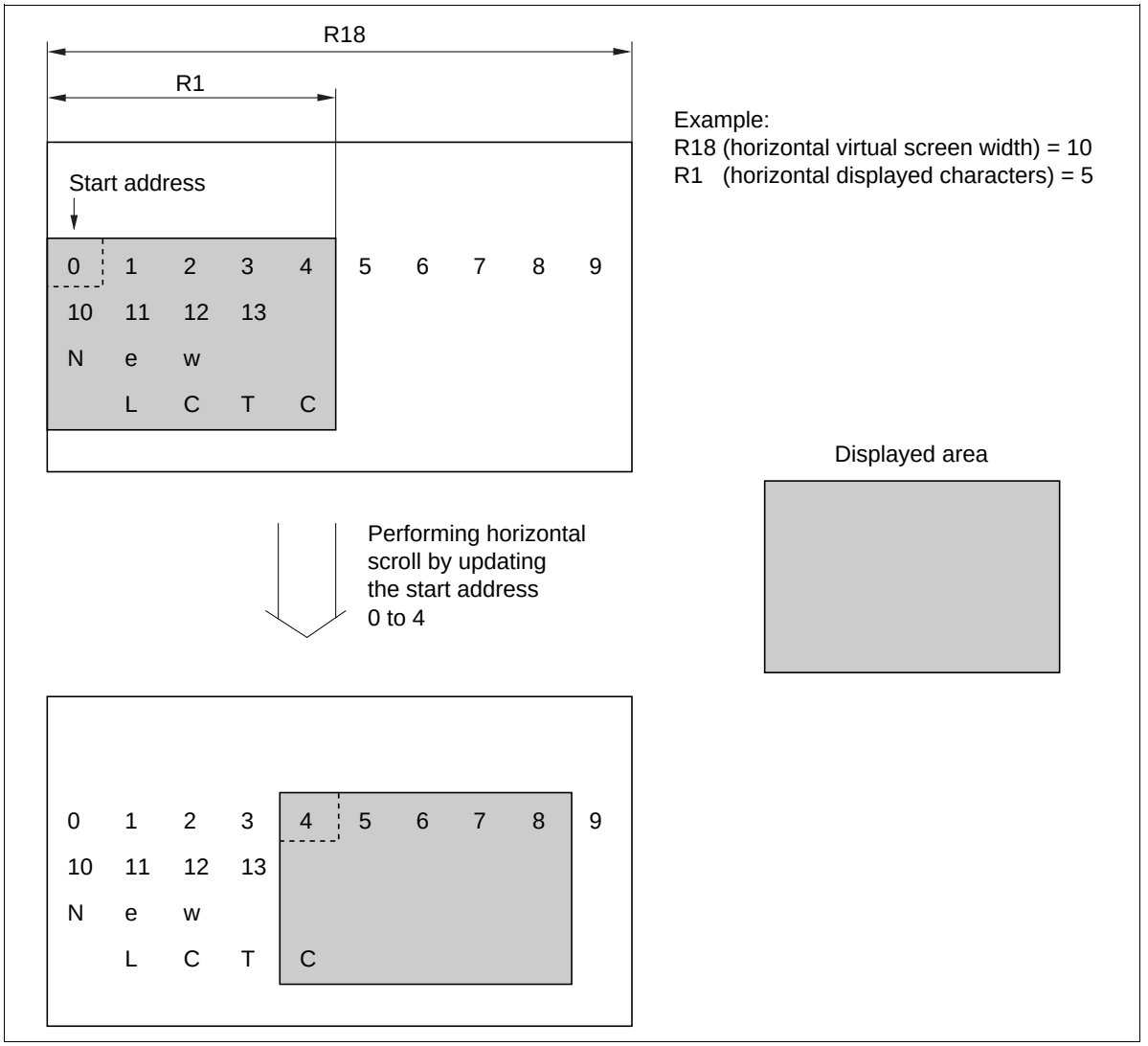


Figure 13 Example of Horizontal Scroll by Setting Horizontal Virtual Screen Width

Smooth Scroll

Vertical smooth scrolling (Figure 14) is performed by updating the display start raster, as specified by the start raster register (R21). This function is offered only in character mode.

Wide Display

The character to be displayed can be doubled in width, by supplying the same data twice (Figure 15). This function is offered only in character mode, and controlled either by bit 2 of the mode register (R22) or by the WIDE pin.

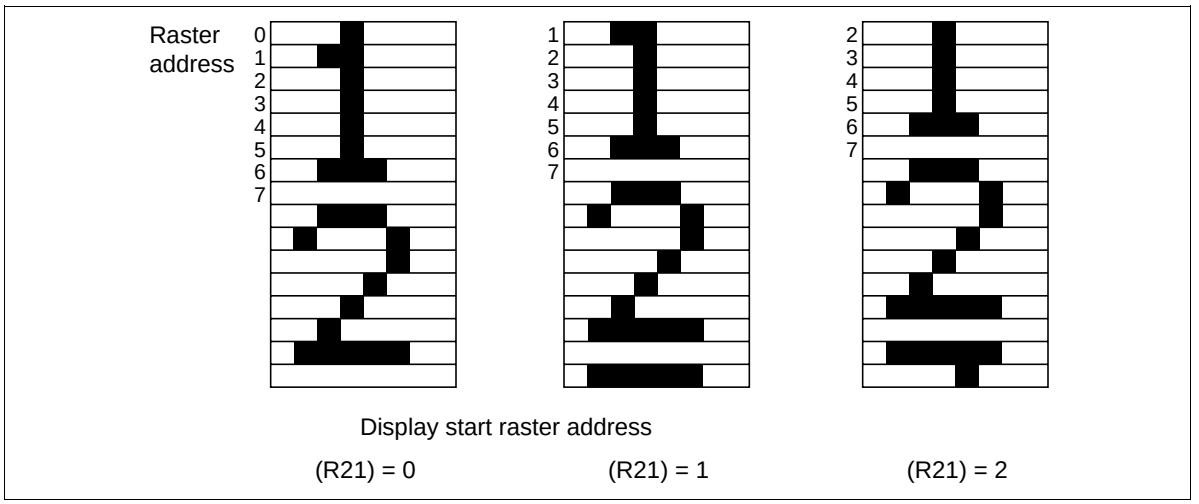


Figure 14 Example of Smooth Scroll by Setting Display Start Raster Address

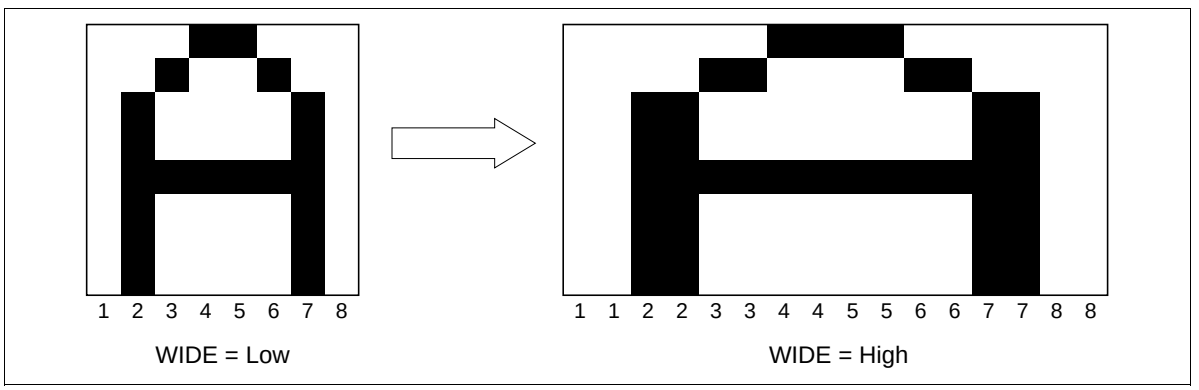


Figure 15 Example of Wide Display

Attribute Functions

A variety of character attribute functions such as reverse video, blinking, nondisplay (white) or nondisplay (black) can be implemented by storing the attribute data in A-RAM (attribute RAM). Figure 16 shows a display example using each attribute function.

The attribute functions are offered only in character mode, and controlled either by bit 0 of the mode register (R22) or the AT pin. As shown in Figure 17, a character attribute can be specified by placing the character code on MD0–MD7, and the attribute code on MD11–MD15. MD8–MD10 are invalid.

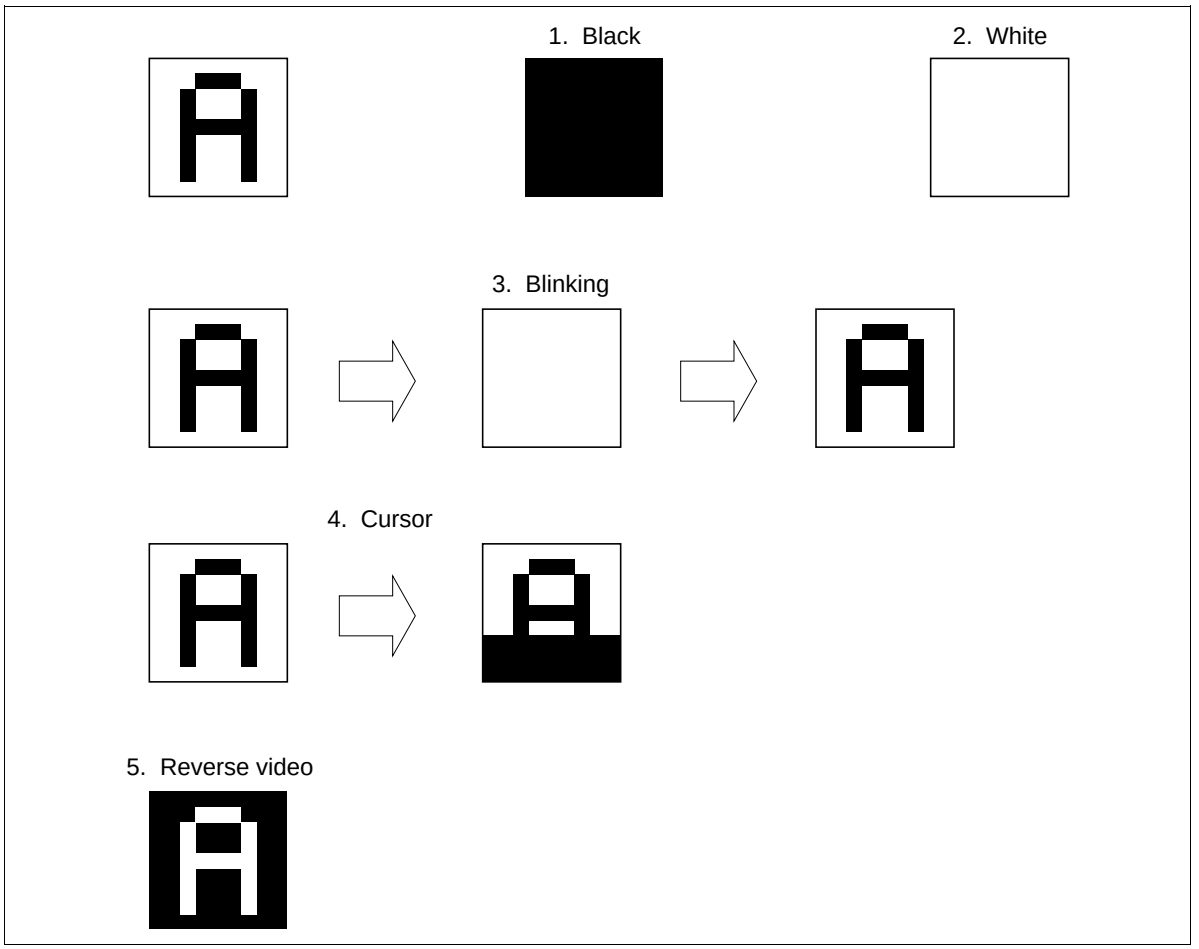


Figure 16 Display Example Using Attribute Functions

MD Input	15	14	13	12	11	10–8	7–0
Function	Non-display (black)	Non-display (white)	Blinking	Cursor	Reverse video	***	Character code

Note: *** Invalid

Figure 17 Attribute Code

OR Function — Superimposing Characters and Graphics

The OR function (Figure 18) generates the OR of the data entered into MD0–MD7 (e.g. character data) and the data into MD8–MD15 (e.g. graphic data) in the LCTC and transfers this data as 1 byte.

This function is offered only in character mode, and controlled by bit 0 of the mode register (R22) or by the AT pin. Any attribute functions are disabled when using the OR function.

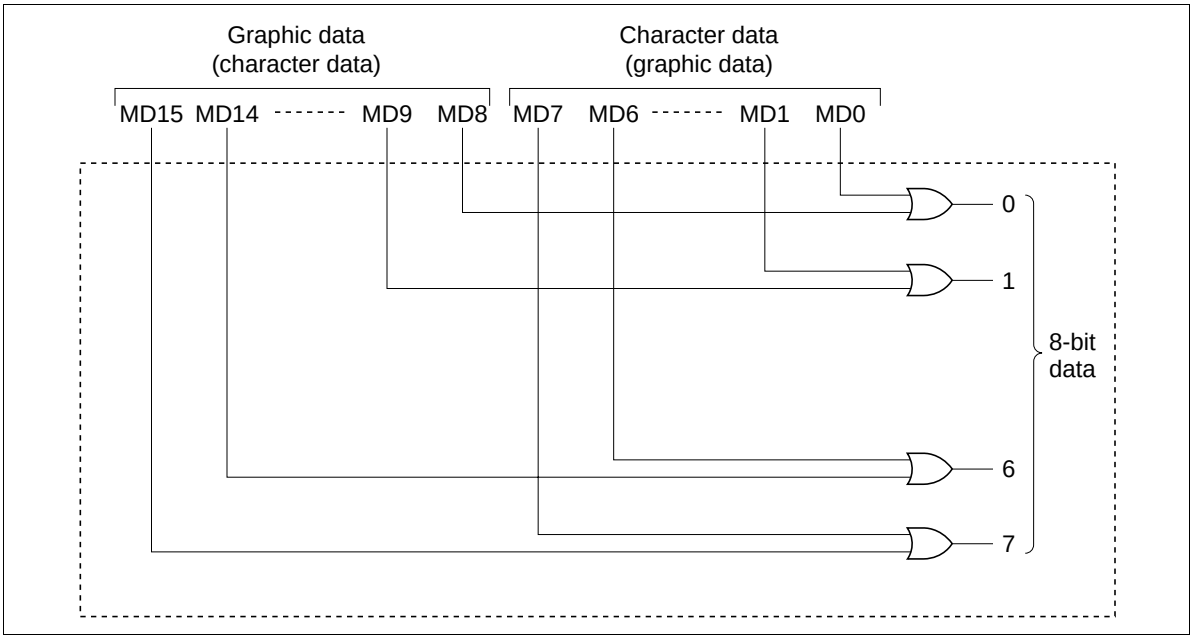


Figure 18 OR Function

DRAM Refresh Address Output Function

The LCTC outputs the address for DRAM refresh while CL1 is high, as shown in Figure 19. The 16 refresh addresses per scanned line are output 16 times, from $00–$FF.

Skew Function

The LCTC can specify the skew (delay) for CUDISP, DISPTMG, CL2 outputs and MD inputs.

If buffer memory and character generator ROM cannot be accessed within one horizontal character display period, the access is retarded to the next cycle by inserting a latch to memory address output and buffer memory output. The skew function retards the CUDISP, DISPTMG, CL2 outputs, and MD inputs in the LCTC to match phase with the display data signal.

By utilizing this function, a low-speed memory can be used as a buffer RAM or a character generator ROM.

This function is controlled by pins SK0 and SK1 as shown in Table 7.

Table 7 Skew Function

SK0	SK1	Skew Function
0	0	No skew
1	0	1 character time skew
0	1	2 character time skew
1	1	Inhibited combination

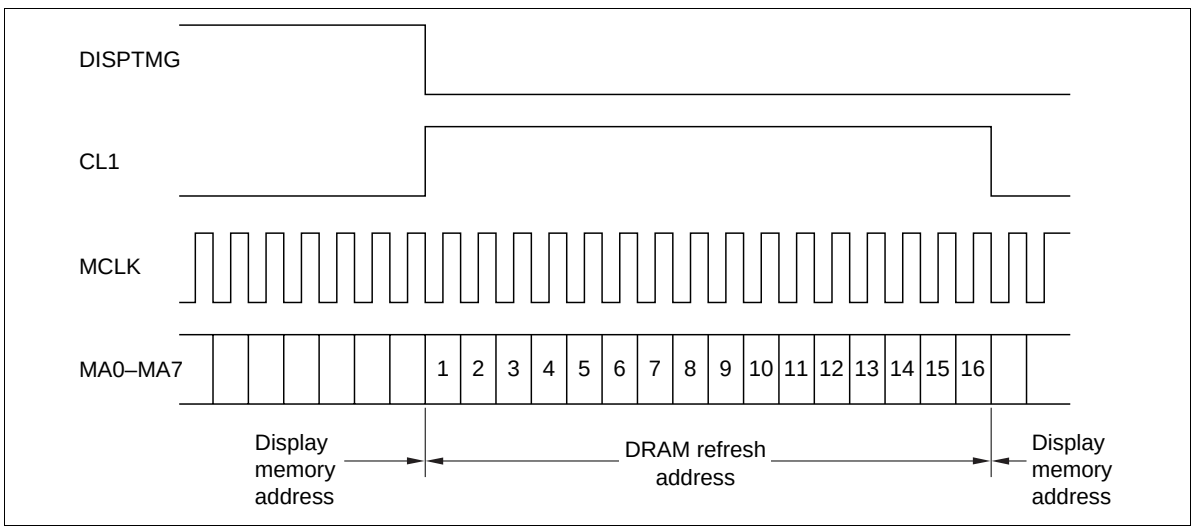


Figure 19 DRAM Refresh Address Output

Easy Mode

This mode utilizes software for systems using the CRTC (HD6845). By setting MODE pin to high, the display mode and screen format are fixed as shown in Table 8. With this mode, software for a CRT screen can be utilized in a system using the LCTC, without changing the BIOS.

Automatic Correction of Down Panel Raster Address

When the LCTC mode is set for character display and dual screen, memory addresses (MA) and raster addresses (RA) are output in such a way as to keep continuity of a display spread over the two panels. Therefore users can use the LCTC without considering the multiplexing duty ratio (the number of vertical dots of a screen) or the character font. (See Figure 20.)

Table 8 Fixed Values in Easy Mode

Reg. No.	Register Name	Fixed Value (Decimal)
R9	Maximum raster address	7
R10	Cursor start raster	6
R11	Cursor end raster	7
R18	Horizontal virtual screen width	Same value as (R1)
R19	Multiplexing duty ratio (H)	99 (in dual screen mode)
R20	Multiplexing duty ratio (L)	199 (in single screen mode)
R21	Display start raster	0
R22	Mode register	0

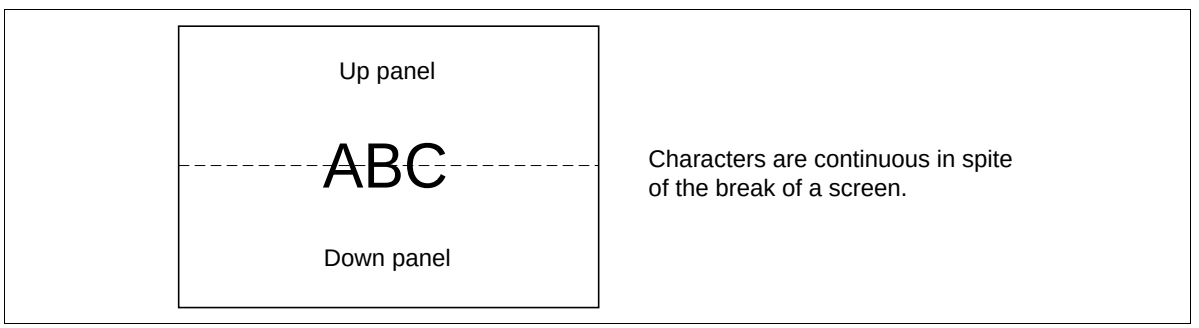


Figure 20 Example of the Display in the Character Mode

System configuration and Mode Setting

LCD System Configuration

The screen configuration, single or dual, must be specified when using the LCD system (Figure 21).

Using the single screen configuration, you can construct an LCD system with lower cost than a dual screen system, since the required number of column drivers is smaller and the manufacturing process for mounting them is simpler. However, there are some limitations, such as duty ratio, breakdown voltage of a driver, and display quality of the liquid crystal, in single screen configuration. Thus, a dual screen configuration may be more suitable to an application.

The LCTC also offers an 8-bit LCD data transfer function to support an LCD screen with a smaller interval of signal input terminals. For a general size LCD screen, such as 640 × 200 single, or 640 × 400 dual, the usual 4-bit LCD data transfer is satisfactory.

Hardware Configuration and Mode Setting

The LCTC supports the following hardware configurations:

- Single or dual screen configuration
- 4-or 8-bit LCD data transfer

and the following screen format:

- Character, graphic 1, or graphic 2 display
- Normal or wide display (only in character mode)
- OR or attribute display (only in character mode)

Also, the LCTC supports up to 40 Mbits/s of large screen mode (mode 13) for large screen display. This mode is provided only in graphic 1 mode.

Table 9 shows the mode selection method according to hardware configuration and screen format. Table 10 shows how they are specified.

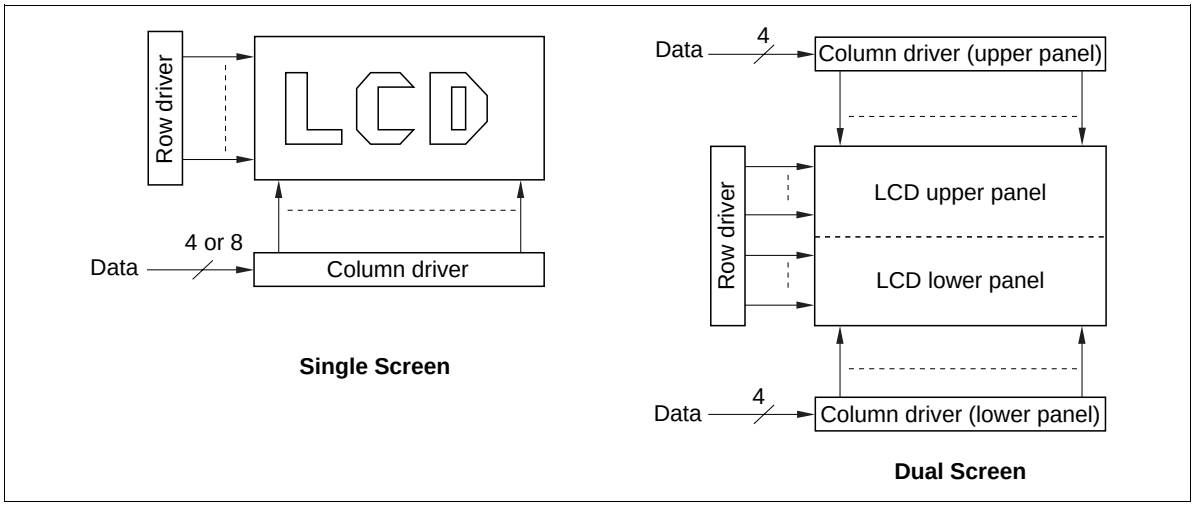


Figure 21 Hardware Configuration According to Screen Format

Table 9 Mode Selection

Hardware Configuration			Screen Format				
LCD Data Transfer	**Screen Configu-ration**	**Screen Size**	**Character/ Graphic**	**Normal/ Wide**	**Attribute/ OR**	**Maximum Data Transfer Speed (Mbps)**	**Mode No.**
4-bit	Single	Normal	Character	Normal	$\frac{AT}{OR}$	20	5
				Wide	$\frac{AT}{OR}$	10	6
			Graphic 1			20	7
			Graphic 2			20	8
	Dual	Normal	Character	Normal	$\frac{AT}{OR}$	20	1
				Wide	$\frac{AT}{OR}$	10	2
			Graphic 1			20	3
			Graphic 2			20	4
		Large	Graphic 1			40	13
8-bit	Single	Normal	Character	Normal	$\frac{AT}{OR}$	20	9
				Wide	$\frac{AT}{OR}$	10	10
			Graphic 1			20	11
			Graphic 2			20	12

Note: Maximum data transfer speed indicates amount of the data read out of a memory. Thus, the data transfer speed sent to the LCD driver in wide function is 20 Mbps.

Mode List

Table 10 Mode List

No.	Mode Name	Pin Name D/$\overline{S}$	G/$\overline{C}$	LS	WIDE	AT	Screen Config.	Graphic/ Character	Data Transfer	Wide Display	Attribute
1	Dual-screen character	1	0	0	0	0	Dual screen	Character	4-bit × 2	Normal	OR
		1	0	0	0	1					AT
2	Dual-screen wide character	1	0	0	1	0				Wide	OR
		1	0	0	1	1					AT
3	Dual-screen graphic 1	1	1	0	0	1		Graphic		—	—
4	Dual-screen graphic 2	1	1	0	0	0					
5	Single-screen character	0	0	0	0	0	Single screen	Character	4-bit	Normal	OR
		0	0	0	0	1					AT
6	Single-screen wide character	0	0	0	1	0				Wide	OR
		0	0	0	1	1					AT
7	Single-screen graphic 1	0	1	0	0	1		Graphic		—	—
8	Single-screen graphic 2	0	1	0	0	0					
9	8-bit character	0	0	1	0	0	Single screen	Character	8-bit	Normal	OR
		0	0	1	0	1					AT
10	8-bit wide character	0	0	1	1	0				Wide	OR
		0	0	1	1	1					AT
11	8-bit graphic 1	0	1	1	0	1		Graphic		—	—
12	8-bit graphic 2	0	1	1	0	0					
13	Large screen	1	1	1	0	1	Dual screen		4-bit × 2		

The LCTC display mode is determined by pins D/$\overline{S}$ (pin 55), G/$\overline{C}$ (pin 58), LS (pin 56), WIDE (pin 54), and AT (pin 57). As for G/C, WIDE, and AT, the OR is taken between data bits 0, 2, and 3 of the mode register (R22). The display mode can be controlled by either one of the external pins or the data bits of R22.

Note: The above 5 pins have 32 status combinations (high and low). Any combinations other than the above are prohibited, because they may cause malfunctions. If you set an prohibited combination, set the right combination again.

Internal Registers

The HD64645/HD64646 has one address register and fourteen data registers. In order to select one out of fourteen data registers, the address of the data register to be selected must be written into the address register. The MPU can transfer data to/from the data register corresponding to the written address.

To be software compatible with the CRTC (HD6845), registers R2–R8, R16, and R17, which are not necessary for an LCD are defined as invalid for the LCTC.

Address Register (AR)

AR register (Figure 22) specifies one out of 14 data registers. Address data is written into the address register when RS is low. If no register corresponding to a specified address exists, the address data is invalid.

Horizontal Total Characters Register (R0)

R0 register (Figure 23) specifies a horizontal scanning period. The total number of horizontal characters less 1 must be programmed into this 8-bit register in character units. Nht indicates the horizontal scanning period including the period when the CPU occupies memory (total number of horizontal characters minus the number of horizontal displayed characters). Its units are, then, converted from time into the number of characters. This value should be specified according to the specification of the LCD system to be used.

Note the following restrictions

$$Nhd + \frac{16}{m} \leq Nht + 1$$

Mode No.	m
5, 9	1
1, 6, 7, 8, 10, 11, 12, 13	2
2, 3, 4	4

Horizontal Displayed Characters Register (R1)

R1 register (Figure 24) specifies the number of characters displayed per row. The horizontal character pitches are 8 bits for normal character display and 16 dots for wide character display and graphic display.

Nhd must be less than the total number of horizontal characters.

Maximum Raster Address Register (R9)

R9 register (Figure 25) specifies the number of rasters per row in characters mode, consisting of 5 bits. The programmable range is 0 (1 raster/row) to 31 (32 rasters/row).

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0	—	
—	—	—	Register address						W

Figure 22 Address Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Nht (total characters – 1)								Character	W

Figure 23 Horizontal Total Characters Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Nhd (displayed characters)								Character	W

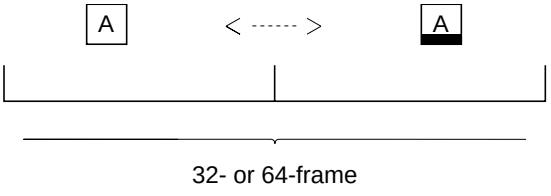
Figure 24 Horizontal Displayed Characters Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	Nr					Raster	W

Figure 25 Maximum Raster Address Register

Cursor Start Raster Register (R10)

R10 register (Figure 26) specifies the cursor start raster address and its blink mode. Refer to Table 11.



Cursor End Raster Register (R11)

R11 register (Figure 27) specifies the cursor end raster address.

Start Address Register (H/L) (R12/R13)

R12/R13 register (Figure 28) specifies a buffer memory read start address. Updating this register facilitates paging and scrolling. R14/R15 register can be read and written to/from the MPU.

Cursor Address Register (H/L) (R14/R15)

R14/R15 register (Figure 29) specifies a cursor display address. Cursor display requires setting R10 and R11, and CUDISP should be connected with MD12 (in character mode). This register can be read from and written to the MPU.

Horizontal Virtual Screen Width Register (R18)

R18 register (Figure 30) specifies the memory width to determine the start address of the next row. By using this register, memory width can be specified larger than the number of horizontal displayed characters. Updating the display start address facilitates scrolling in any direction within a memory space.

The start address of the next row is that of the previous row plus Nir. If a larger memory width than display width is unnecessary, Nir should be set equal to the number of horizontal displayed characters.

Table 11 Cursor Blink Mode

B	P	Cursor Blink Mode
0	0	Cursor on; without blinking
0	1	Cursor off
1	0	Blinking once every 32 frames
1	1	Blinking once every 64 frames

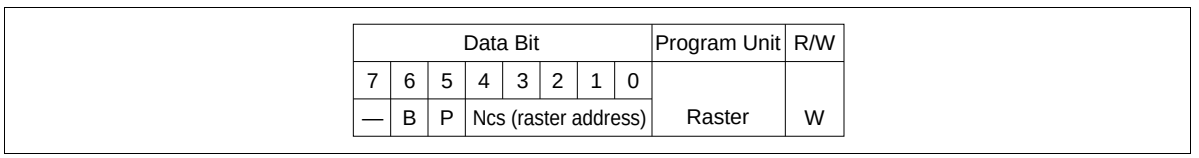


Figure 26 Cursor Start Raster Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	Nce (raster address)					Raster	W

Figure 27 Cursor End Raster Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Memory address (H) (R12)								Memory address	R/W
Memory address (L) (R13)									

Figure 28 Start Address Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Memory address (H) (R14)								Memory address	R/W
Memory address (L) (R15)									

Figure 29 Cursor Address Register

Multiplexing Duty Ratio Register (H/L) (R19/R20)

R19/R20 register (Figure 31) specifies the number of vertical dots of the display screen. The programmed value differs according to the LCD screen configuration.

In single screen configuration:

$$\text{(Programmed value)} = \text{(Number of vertical dots)} - 1$$

In dual screen configuration:

$$\text{(Programmed value)} = \frac{\text{(Number of vertical dots)}}{2} - 1$$

Display Start Raster Register (R21)

R21 register (Figure 32) specifies the start raster of the character row displayed on the top of the screen. The programmed value should be equal or less than the maximum raster address. Updating this register allows smooth scrolling in character mode.

Mode Register (R22)

The Or of the data bits of R22 (Figure 33) register and the external terminals of the same name determines a particular mode (Figure 34).

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Nir (No. of chars. of virtual width)								Character	W

Figure 30 Horizontal Virtual Screen Width Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	—	—	—	— (R19)	Ndh*	Raster	W
Ndl (Number of rasters – 1) (R20)									

Note: * Number of rasters

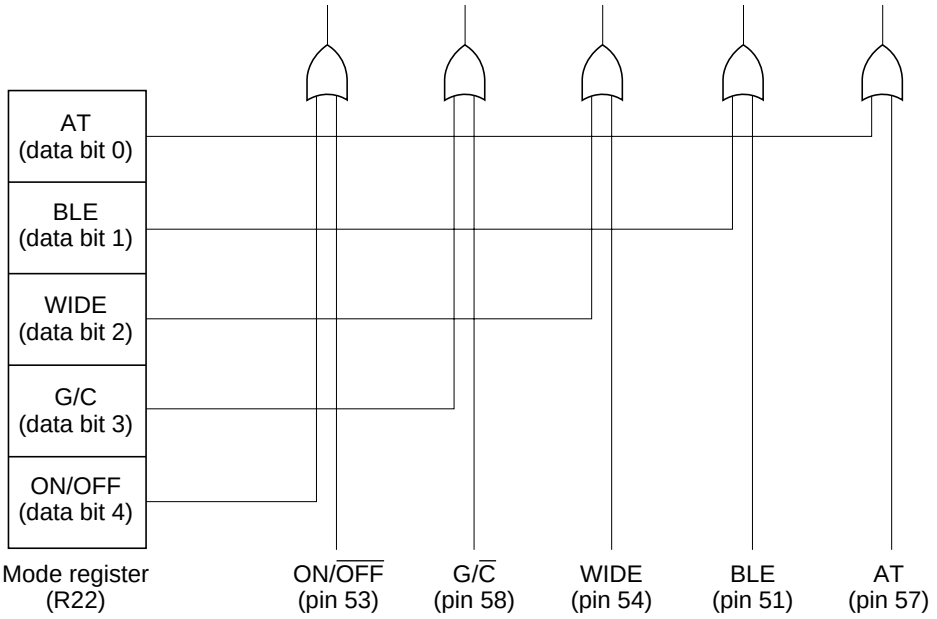
Figure 31 Multiplexing Duty Ratio Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	Raster address					Raster	W

Figure 32 Display Start Raster Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	ON/OFF	G/C	WIDE	BLE	AT	—	W

Figure 33 Mode Register



Notes: 1. AT (valid only when G/$\overline{C}$ is low (character mode))
AT = High: Attribute functions enabled, OR function disabled.
AT = Low: OR function enabled, attribute functions disabled.

2. BLE (valid only when G/$\overline{C}$ is low (character mode))
BLE = High: Blinking enable on the character specified by attribute RAM
BLE = Low: No blinking

3. WIDE (valid only when G/$\overline{C}$ is low (character mode))
WIDE = High: Wide display enabled
WIDE = Low: Normal display

4. G/$\overline{C}$
G/$\overline{C}$ = High: Graphic 1 display (when AT = low) or graphic 2 display (when AT = high)
G/$\overline{C}$ = Low: Character display

5. ON/$\overline{OFF}$
ON/$\overline{OFF}$ = High: Display on state
ON/$\overline{OFF}$ = Low: Display off state

Figure 34 Correspondence between Mode Register and External Pins

Restrictions on Programming Internal Registers

Note when programming that the values you can write into the internal registers are restricted as shown in Table 12.

Table 12 Restrictions on Writing Values into the Internal Registers

Function	Restrictions	Register
Display format	$1 < Nhd < Nht + 1 \leq 256$ $Nhd + \frac{16}{m}$ *1 $\leq Nht + 1$	R0, R1
	(No. of vertical dots) × (No. of horizontal dots) × (frame frequency; fFRM) ≤ (data transfer speed; V) $\left\{\begin{matrix}1\\2\end{matrix}\right\}$ *2 × (Nd + 1) × Nhd × $\left\{\begin{matrix}8\\16\end{matrix}\right\}$ *3 $f_{FRM} \leq V$	R1, R19, R20
	$Nhd \leq Nir$	R1, R18
	$0 \leq Ndi \leq 511$	R19, R20
Cursor control	$0 \leq Ncs \leq Nce$	R10, R11
	$Nce \leq Nr$	R10, R9
Smooth scroll	$Nsr \leq Nr$	R21, R9
Memory width set	$0 \leq Nir \leq 255$	R18

Notes: 1. m varies according to the modes. See the following table.

Mode No.	m
5, 9	1
1, 6, 7, 8, 10, 11, 12, 13	2
2, 3, 4	4

2. Set 1 when an LCD screen is a single screen, and set 2 when dual. Modes are classified as shown in the following table.

Mode No.	Value
5, 6, 7, 8, 9, 10, 11, 12	1
1, 2, 3, 4, 13	2

3. Set 8 when a character is constructed with 8 dots, and set 16 when with 16 dots. Modes are classified as shown in the following table.

Mode No.	Value
1, 5, 9	8
2, 3, 4, 6, 7, 8, 10, 11, 12, 13	16

Reset

$\overline{RES}$ pin determines the internal state of LSI counters and the like. This pin does not affect register contents nor does it basically control output terminals.

Reset is defined as follows (Figure 35):

- At reset: the time when $\overline{RES}$ goes low
- During reset: the period while $\overline{RES}$ remains low
- After reset: the period on and after the $\overline{RES}$ transition from low to high
- Make sure to hold the reset signal low for at least 1 μs

$\overline{RES}$ pin should be pulled high by users during operation.

Reset State of Pins

$\overline{RES}$ pin does not basically control output pins, and operates regardless of other input pins.

1. Preserve states before reset
   LU0–LU3, LD0–LD3, FLM, CL1, RA0–RA4
2. Fixed at high level
   MLCK
3. Preserve states before reset or fixed at low level according to the timing when the reset signal is input
   DISPTMG, CUDISP, MA0–MA15
4. Fixed at high or low according to mode
   CL2
5. Unaffected
   DB0–DB7

Reset State of Registers

$\overline{RES}$ pin does not affect register contents. Therefore, registers can be read or written even during a reset state; their contents will be preserved regardless of reset until they are rewritten to.

Notes for HD64645/HD64646

1. The HD64645/HD64646 are CMOS LSIs, and it should be noted that input pins must not be left disconnected, etc.
2. At power-on, the state of internal registers becomes undefined. The LSI operation is undefined until all internal registers have been programmed.

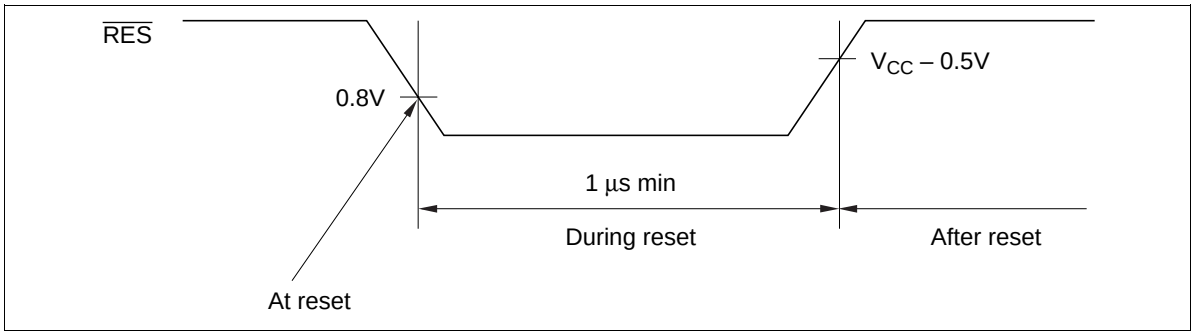


Figure 35 Reset Definition

Absolute Maximum Ratings

Item	Symbol	Value	Note
Supply voltage	V_{CC}	–0.3 to +7.0V	2
Terminal voltage	Vin	–0.3 to VCC + 0.3V	2
Operating temperature	T_{opr}	–20°C to +75°C	
Storage temperature	T_{stg}	–55°C to +125°C	

Notes: 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 5.0V ± 10%, GND = 0V, Ta = –20°C to +75°C). If these conditions are exceeded, it could affect reliability of LSI.

2. With respect to ground (GND = 0V)

Electrical Characteristics

DC Characteristics (V_{CC} = 5.0V ±10%, GND = 0V, T_a = –20°C to +75°C, unless otherwise noted)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input high voltage	$\overline{RES}$, MODE, SK0, SK1	VIH	V_{CC} – 0.5		V_{CC} + 0.3	V	
	DCLK, ON/$\overline{OFF}$		2.2		V_{CC} + 0.3	V	
	All others		2.0		V_{CC} + 0.3	V	
Input low voltage	All others	VIL	–0.3		0.8	V	
Output high voltage	TTL interface*[1]	VOH	2.4			V	I_{OH} = –400 µA
	CMOS interface*[1]		V_{CC} – 0.8			V	I_{OH} = –400 µA
Output low voltage	TTL interface	VOL			0.4	V	I_{OL} = 1.6 mA
	CMOS interface				0.8	V	I_{OL} = 400 µA
Input leakage current	All inputs except DB0–DB7	I_{IL}	–2.5		+2.5	µA	
Three state (off-state) leakage current	DB0–DB7	I_{TSL}	–10		+10	µA	
Current dissipation*[2]		I_{CC}			10	mA	

Notes: 1. TTL Interface; MA0–MA15, RA0–RA4, DISPTMG, CUDISP, DB0–DB7, MCLK
C-MOS Interface; LU0–LU3, LD0–LD3, CL1, CL2, M, FLM

2. Input/output current is excluded. When input is at the intermediate level with CMOS, excessive current flows through the input circuit to power supply. Input level must be fixed at high or low to avoid this condition.

3. If the capacitive loads of LU0–LU3 and LD0–LD3 exceed the rating, noise over 0.8 V may be produced on CUDISP, DISPTMG, MCLK, FLM and M. In case the loads of LU0–LU3 and LD0–LD3 are larger than the ratings, supply signals to the LCD module through buffers.

AC Characteristics

CPU Interface (V_{CC} = 5.0V ± 10%, GND = 0V, T_a = –20°C to +75°C, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Figure
$\overline{RD}$ high level width	t_{WRDH}	190			ns	36
$\overline{RD}$ low level width	t_{WRDL}	190			ns	
$\overline{WR}$ high level width	t_{WWRH}	190			ns	
$\overline{WR}$ low level width	t_{WWRL}	190			ns	
$\overline{CS}$, RS setup time	t_{AS}	0			ns	
$\overline{CS}$, RS hold time	t_{AH}	0			ns	
DB0–DB7 setup time	t_{DSW}	100			ns	
DB0–DB7 hold time	t_{DHW}	0			ns	
DB0–DB7 output delay time	t_{DDR}			150	ns	
DB0–DB7 output hold time	t_{DHR}	20			ns	

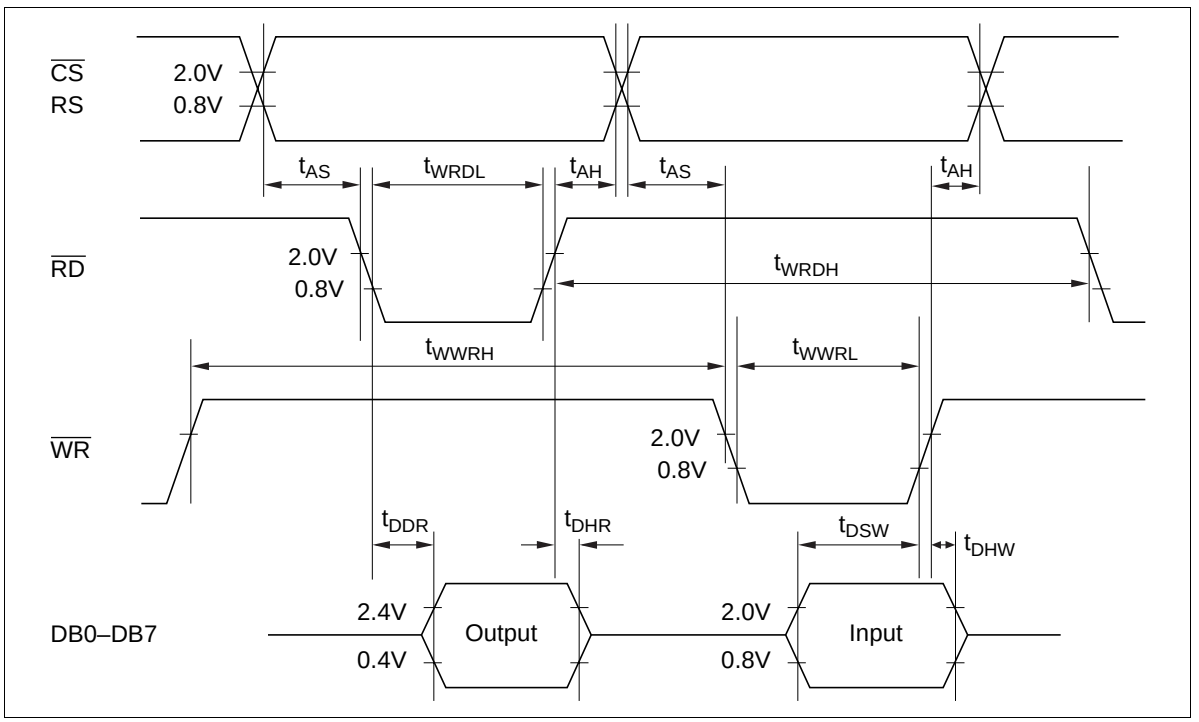


Figure 36 CPU Interface

Memory Interface (V_{CC} = 5.0V ± 10%, GND = 0V, T_a = –20°C to +75°C, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Figure
DCLK cycle time	t_{CYCD}	100	—	—	ns	37
DCLK high level width	t_{WDH}	30	—	—	ns	
DCLK low level width	t_{WDL}	30	—	—	ns	
DCLK rise time	t_{Dr}	—	—	20	ns	
DCLK fall time	t_{Df}	—	—	20	ns	
MCLK delay time	t_{DMD}	—	—	60	ns	
MCLK rise time	t_{Mr}	—	—	30	ns	
MCLK fall time	t_{Mf}	—	—	30	ns	
MA0–MA15 delay time	t_{MAD}	—	—	150	ns	
MA0–MA15 hold time	t_{MAH}	10	—	—	ns	
RA0–RA4 delay time	t_{RAD}	—	—	150	ns	
RA0–RA4 hold time	t_{RAH}	10	—	—	ns	
DISPTMG delay time	t_{DTD}	—	—	150	ns	
DISPTMG hold time	t_{DTH}	10	—	—	ns	
CUDISP delay time	t_{CDD}	—	—	150	ns	
CUDISP hold time	t_{CDH}	10	—	—	ns	
CL1 delay time	t_{CL1D}	—	—	150	ns	
CL1 hold time	t_{CL1H}	10	—	—	ns	
CL1 rise time	t_{CL1r}	—	—	50	ns	
CL1 fall time	t_{CL1f}	—	—	50	ns	
MD0–MD15 setup time	t_{MDS}	30	—	—	ns	
MD0–MD15 hold time	t_{MDH}	15	—	—	ns	

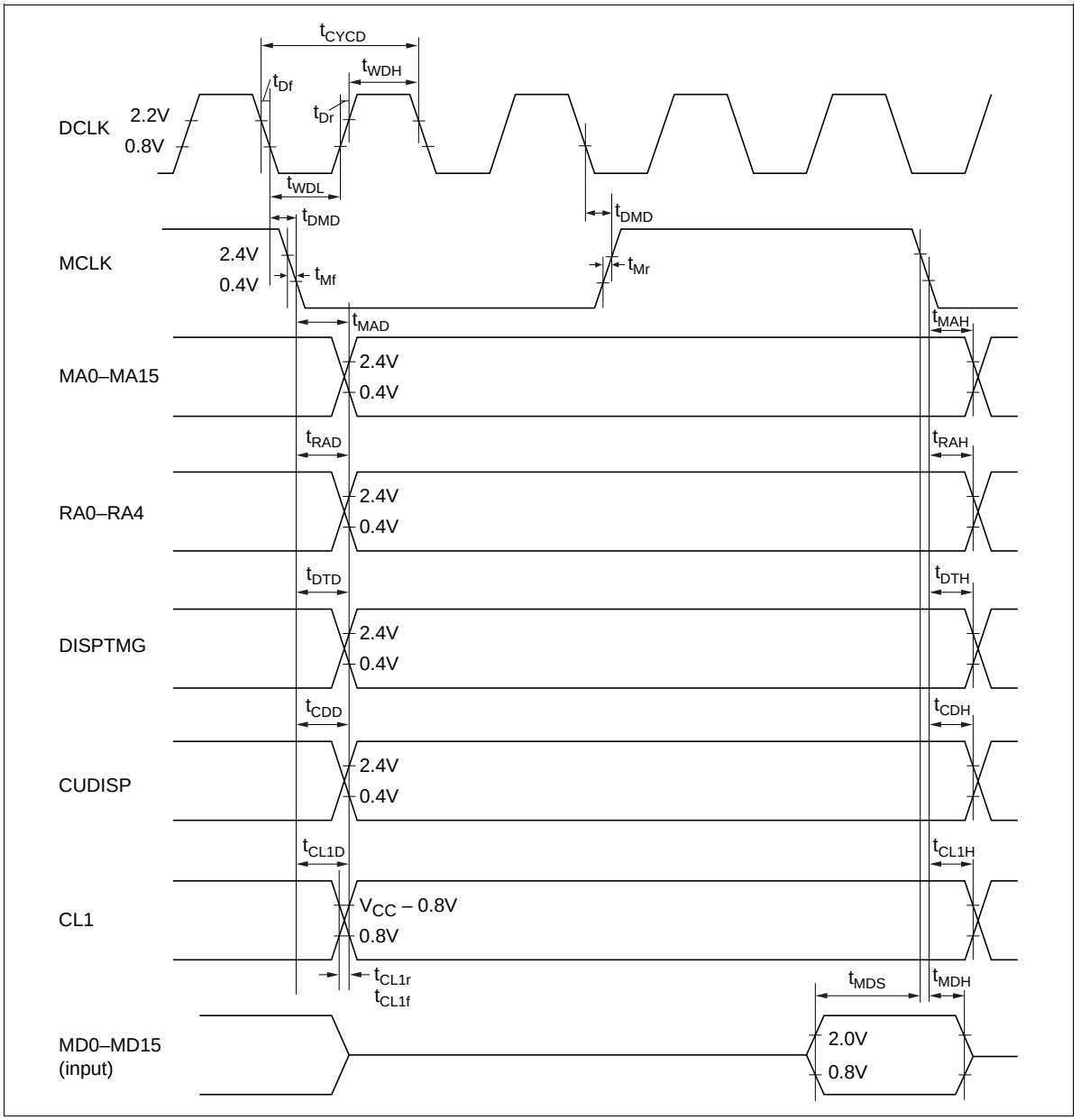


Figure 37 Memory Interface

LCD Interface 1 (HD64645) (V_{CC} = 5.0V ± 10%, GND = 0V, T_a = –20°C to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Figure
Display data setup time	t_{LDS}	50	—	—	ns	38
Display data hold time	t_{LDH}	100	—	—	ns	
CL2 high level width	t_{WCL2H}	100	—	—	ns	
CL2 low level width	t_{WCL2L}	100	—	—	ns	
FLM setup time	t_{FS}	500	—	—	ns	
FLM hold time	t_{FH}	300	—	—	ns	
CL1 rise time	t_{CL1r}	—	—	50	ns	
CL1 fall time	t_{CL1f}	—	—	50	ns	
CL2 rise time	t_{CL2r}	—	—	50	ns	
CL2 fall time	t_{CL2f}	—	—	50	ns	

Note: At f_{CL2} = 3 MHz

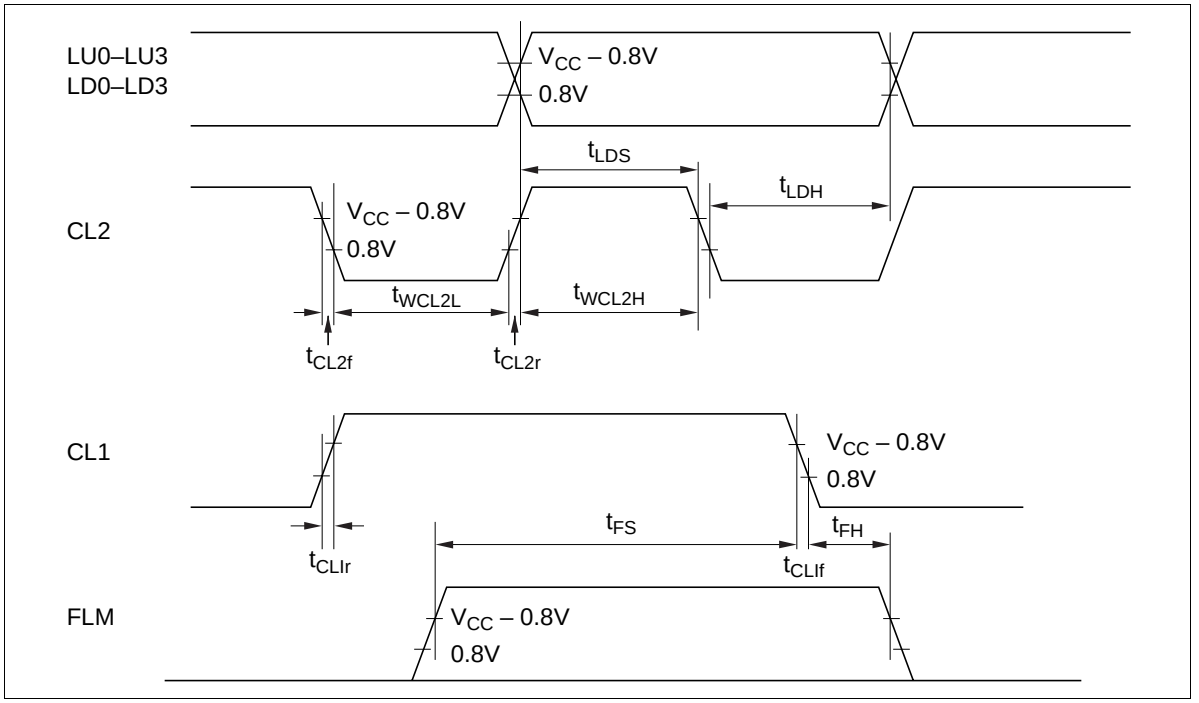


Figure 38 LCD Interface

LCD Interface 2 (HD64646 at f_{CL2} = 3 MHz) (V_{CC} = 5.0V ± 10%, GND = 0V, T_a = –20°C to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Figure
FLM setup time	t_{Fs}	500	—	—	ns	39
FLM hold time	t_{FH}	300	—	—	ns	
M delay time	t_{DM}	—	—	200	ns	
CL1 high level width	t_{CL1H}	300	—	—	ns	
Clock setup time	t_{SCL}	500	—	—	ns	
Clock hold time	t_{HCL}	100	—	—	ns	
Phase difference 1	t_{PD1}	100	—	—	ns	
Phase difference 2	t_{PD2}	500	—	—	ns	
CL2 high level width	t_{CL2H}	100	—	—	ns	
CL2 low level width	t_{CL2L}	100	—	—	ns	
CL2 rise time	t_{CL2r}	—	—	50	ns	
CL2 fall time	t_{CL2f}	—	—	50	ns	
Display data setup time	t_{LDS}	80	—	—	ns	
Display data hold time	t_{LDH}	100	—	—	ns	
Display data delay time	t_{LDD}	—	—	30	ns	

LCD Interface 3 (HD64646 at f_{CL2} = 5 MHz) (V_{CC} = 5.0V ± 10%, GND = 0V, T_a = –20°C to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Figure
FLM setup time	t_{Fs}	500	—	—	ns	39
FLM hold time	t_{FH}	200	—	—	ns	
M delay time	t_{DM}	—	—	200	ns	
CL1 high level width	t_{CL1H}	300	—	—	ns	
Clock setup time	t_{SCL}	500	—	—	ns	
Clock hold time	t_{HCL}	100	—	—	ns	
Phase difference 1	t_{PD1}	70	—	—	ns	
Phase difference 2	t_{PD2}	500	—	—	ns	
CL2 high level width	t_{CL2H}	50	—	—	ns	
CL2 low level width	t_{CL2L}	50	—	—	ns	
CL2 rise time	t_{CL2r}	—	—	50	ns	
CL2 fall time	t_{CL2f}	—	—	50	ns	
Display data setup time	t_{LDS}	30	—	—	ns	
Display data hold time	t_{LDH}	30	—	—	ns	
Display data delay time	t_{LDD}	—	—	30	ns	

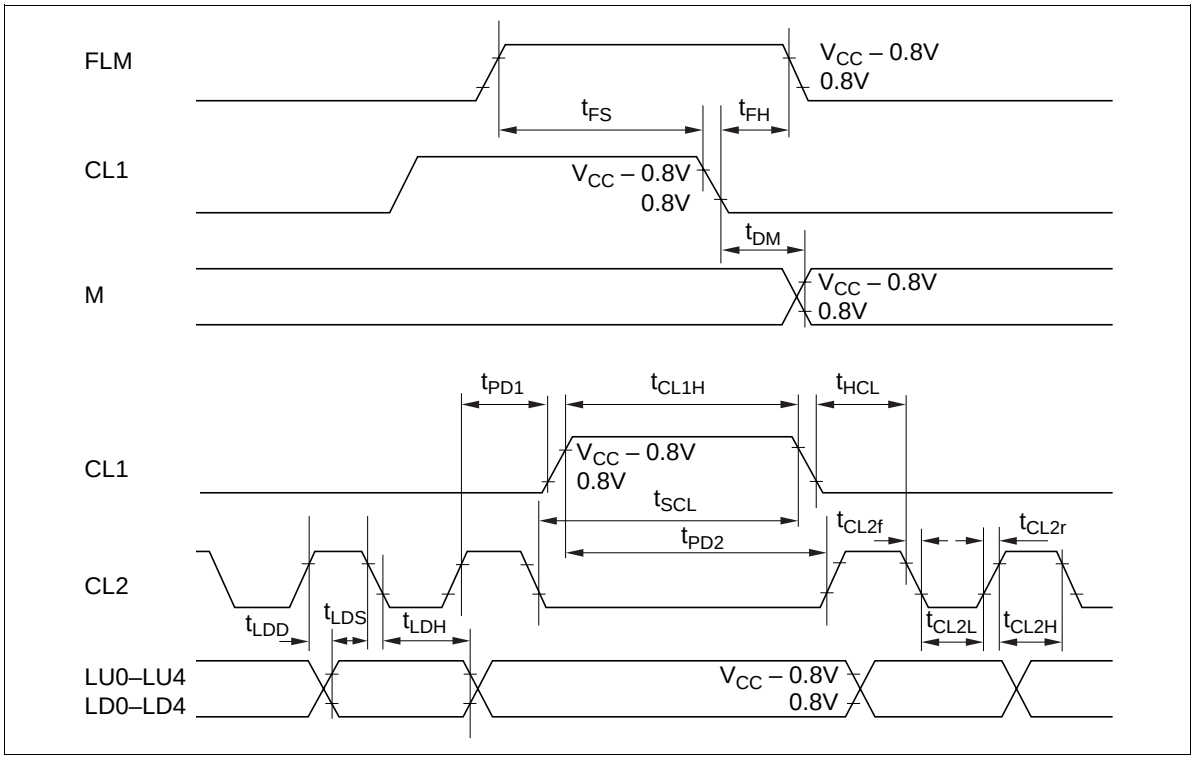
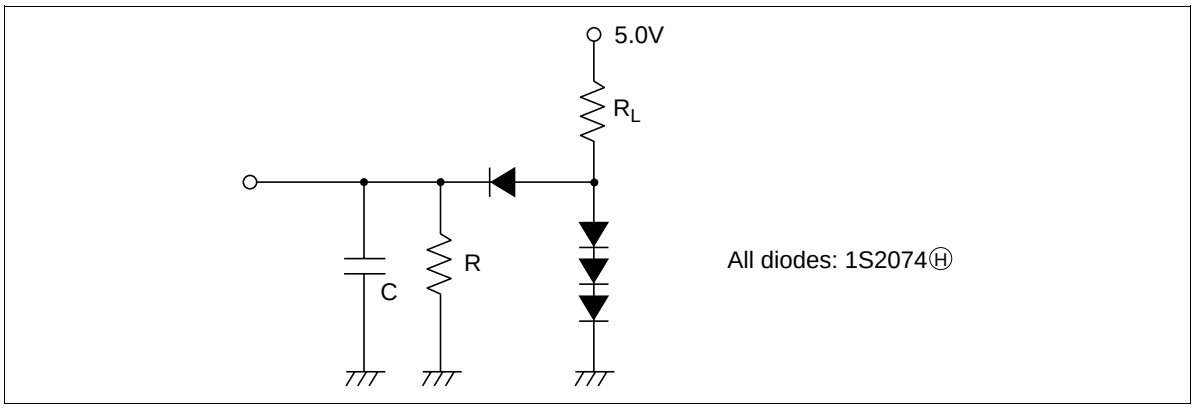


Figure 39 LCD Interface

Load Circuit

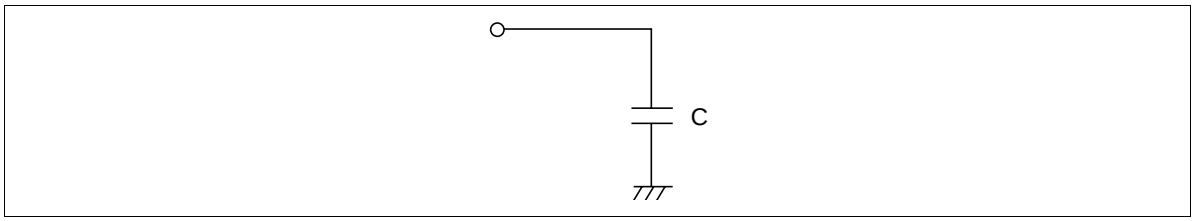
TTL Load

Terminal	R_L	R	C	Remarks
DB0–DB7	2.4 kΩ	11 kΩ	130 pF	tr, tf: Not specified
MA0–MA15, RA0–RA4, DISPTMG, CUDISP	2.4 kΩ	11 kΩ	40 pF	
MCLK	2.4 kΩ	11 kΩ	30 pF	tr, tf: Specified



Capacitive Load

Terminal	C	Remarks
CL2	150 pF	tr, tf: Specified
CL1	200 pF	
LU0–LU3, LD0–LD3, M	150 pF	tr, tf: Not specified
FLM	50 pF	



Refer to user's manual (No. 68-1-160) and application note (No. ADE-502-003) for detail of this product.

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