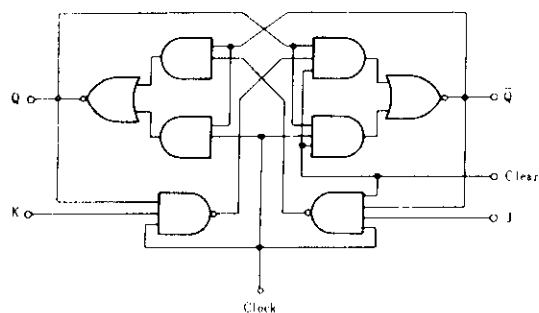
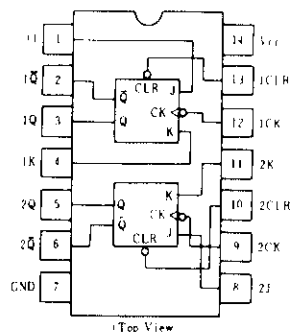


HD74LS107A ● Dual J-K Negative-edge-triggered Flip-Flops (with Clear)

■ BLOCK DIAGRAM (1/2)



■ PIN ARRANGEMENT



■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Clock frequency	f_{clock}	0	—	30	MHz
Pulse width	Clock High	20	—	—	ns
	Clear Low	25	—	—	ns
Setup time	"H" Data	20↓	—	—	ns
	"L" Data	20↓	—	—	ns
Hold time	t_h	0↓	—	—	ns

Note) ↓: The arrow indicates the falling edge.

■ FUNCTION TABLE

Inputs				Outputs	
Clear	Clock	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_0	$\bar{Q}_0$

Notes) H; high level, L; low level, X; irrelevant

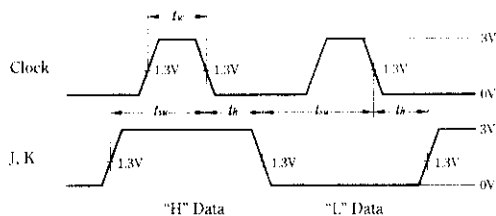
↓; transition from high to low level

Q_0 ; level of Q before the indicated steady-state input conditions were established.

$\bar{Q}_0$; complement of Q_0 or level of $\bar{Q}$ before the indicated steady-state input conditions were established.

Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.

■ TIMING DEFINITION



ELECTRICAL CHARACTERISTICS (Ta = -20 ~ +75°C)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input voltage	V_{IH}		2.0	—	—	V
	V_{IL}		—	—	0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V, V_{IH}=2V, V_{IL}=0.8V, I_{OH}=-400\mu A$	2.7	—	—	V
	V_{OL}	$V_{CC}=4.75V, V_{IH}=2V$	—	—	0.5	V
		$I_{OL}=8mA$	—	—	0.4	
		$V_{IL}=0.8V$	—	—	0.4	
Input current	J, K	$V_{CC}=5.25V, V_I=2.7V$	—	—	20	μA
	Clear		—	—	60	
	Clock		—	—	80	
	J, K	$V_{CC}=5.25V, V_I=0.4V$	—	—	-0.4	mA
	Clear		—	—	-0.8	
	Clock		—	—	-0.8	
	J, K	$V_{CC}=5.25V, V_I=7V$	—	—	0.1	mA
	Clear		—	—	0.3	
	Clock		—	—	0.4	
Short-circuit output current	I_{OS}	$V_{CC}=5.25V$	-20	—	-100	mA
Supply current **	I_{CC}	$V_{CC}=5.25V$	—	4	6	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V, I_{IN}=-18mA$	—	—	-1.5	V

* $V_{CC}=5V, T_a=25^\circ C$

** With all outputs open, I_{CC} is measured with the Q and $\bar{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

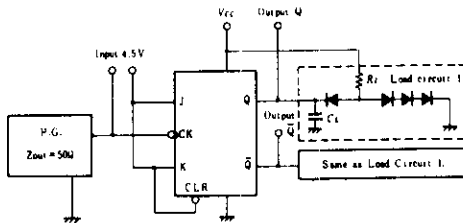
SWITCHING CHARACTERISTICS (VCC = 5V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}			$C_L = 15pF, R_L = 2k\Omega$	30	45	—	MHz
Propagation delay time	t_{PLH}	Clear	Q, $\bar{Q}$		—	15	20	ns
	t_{PHL}	Clock	Q, $\bar{Q}$		—	15	20	ns

TESTING METHOD

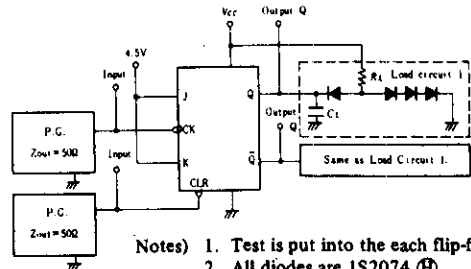
1) Test Circuit

1.1) $f_{max}, t_{PLH}, t_{PHL}$ (Clock → Q, $\bar{Q}$)



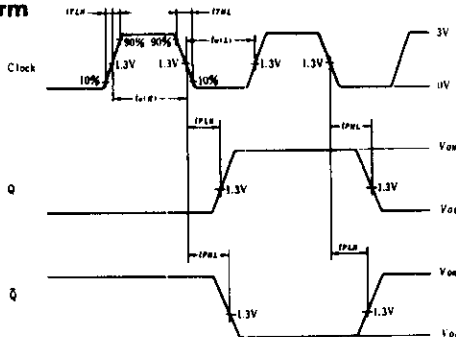
- Notes) 1. Test is put into the each flip-flop.
2. All diodes are 1S2074 (H).
3. C_L includes probe and jig capacitance.

1.2) t_{PHL} (Clear → Q), t_{PLH} (Clear → $\bar{Q}$)

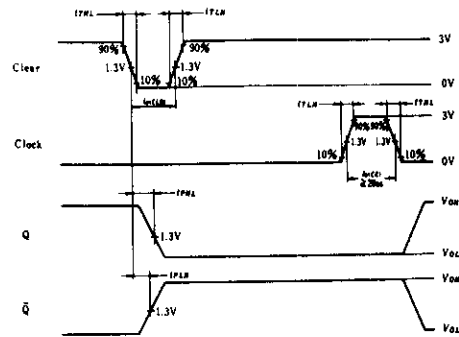


- Notes) 1. Test is put into the each flip-flop.
2. All diodes are 1S2074 (H).
3. C_L includes probe and jig capacitance.

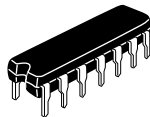
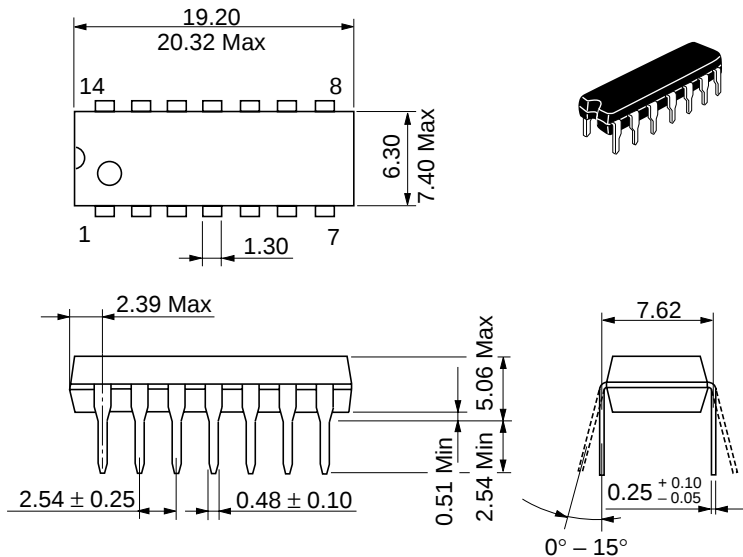
Waveform



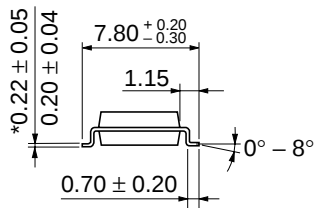
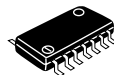
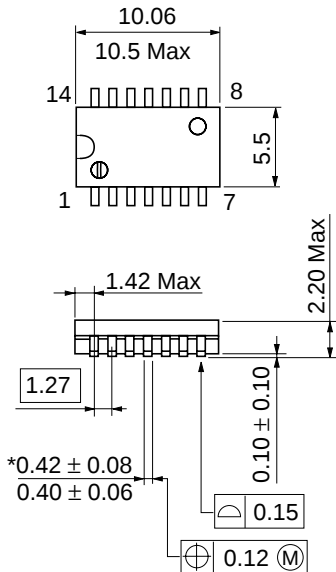
Note) Clock input pulse: $t_{TLH} \leq 15ns, t_{THL} \leq 6ns, PRR=1MHz$, duty cycle=50% and: for $f_{max}, t_{TLH}=t_{THL} \leq 2.5ns$.



Note) Clear and clock input pulse: $t_{TLH} \leq 15ns, t_{THL} \leq 6ns, PRR=1MHz$

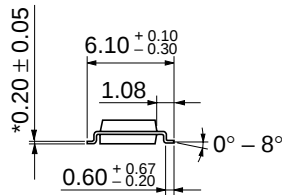
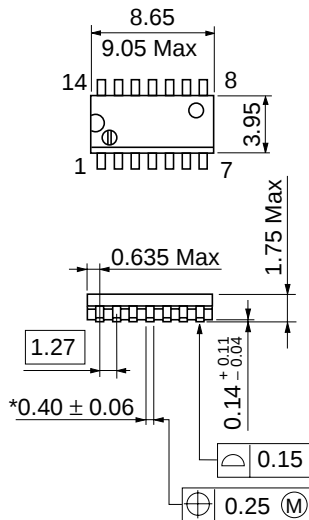


Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

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