

HD74LS193 • Synchronous Up/Down 4-bit Binary Counters (dual clock lines)

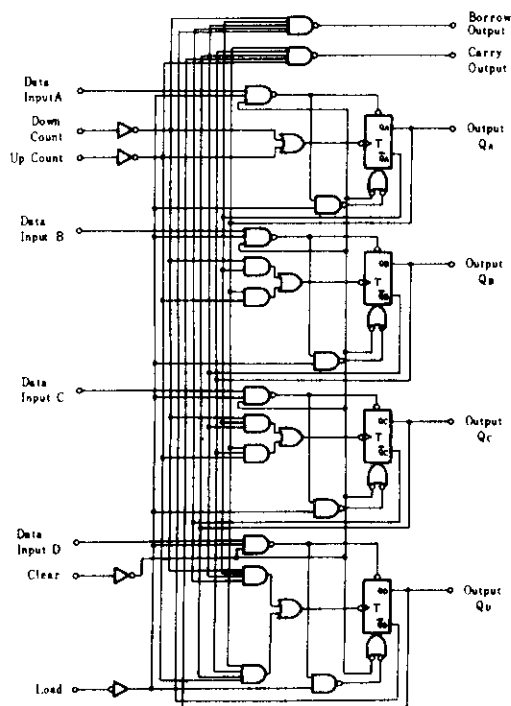
Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters. The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high. This counter is fully programmable; That is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs. A clear input has been

provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words. This counter was designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up-and down-counting functions.

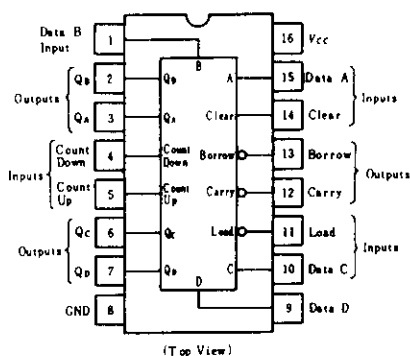
The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists.

The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

■ BLOCK DIAGRAM



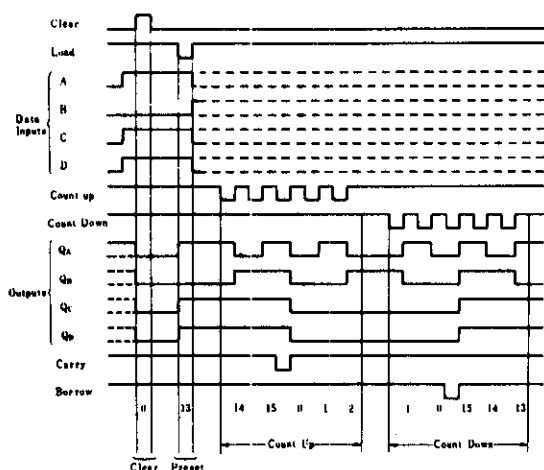
■ PIN ARRANGEMENT



■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Clock frequency	f_{clock}	0	—	25	MHz
Pulse width	t_w	20	—	—	ns
Setup time (Clear)	$t_{su(clear)}$	40	—	—	ns
Setup time	t_{su}	20	—	—	ns
Hold time	t_h	3	—	—	ns

COUNT SEQUENCES



Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input voltage	V_{IH}		2.0	—	—	V
	V_{IL}		—	—	0.8	V
Output voltage	V_{OH}	$V_{CC} = 4.75\text{V}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}, I_{OH} = -400\mu\text{A}$	2.7	—	—	V
	V_{OL}	$V_{CC} = 4.75\text{V}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}$				
Input current	I_{IH}	$V_{CC} = 5.25\text{V}, V_I = 2.7\text{V}$	—	—	20	μA
	I_{IL}	$V_{CC} = 5.25\text{V}, V_I = 0.4\text{V}$	—	—	-0.4	mA
	I_I	$V_{CC} = 5.25\text{V}, V_I = 7\text{V}$	—	—	0.1	mA
Short-circuit output current	I_{OS}	$V_{CC} = 5.25\text{V}$	-20	—	-100	mA
Supply current**	I_{CC}	$V_{CC} = 5.25\text{V}$	—	19	34	mA
Input clamp voltage	V_{IK}	$V_{CC} = 4.75\text{V}, I_{IN} = -18\text{mA}$	—	—	-1.5	V

* $V_{CC} = 5\text{V}, T_a = 25^\circ\text{C}$

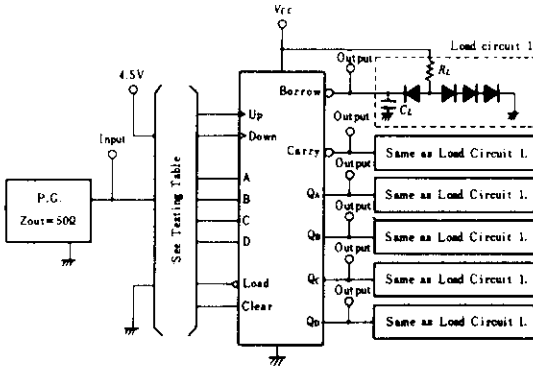
** I_{CC} is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5V.

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{V}, T_a = 25^\circ\text{C}$)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}			$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$	25	32	—	MHz
Propagation delay time	t_{PLH}	Count-up	Carry		—	17	26	ns
	t_{PHL}				—	18	24	ns
	t_{PLH}	Count-down	Borrow		—	16	24	ns
	t_{PHL}				—	15	24	ns
	t_{PLH}	Either Count	Q		—	27	38	ns
	t_{PHL}				—	30	47	ns
	t_{PLH}	Load	Q		—	24	40	ns
	t_{PHL}				—	25	40	ns
	t_{PHL}	Clear	Q		—	23	35	ns

■ TESTING METHOD

1) Test Circuit



Notes) 1. C_L includes probe and jig capacitance.

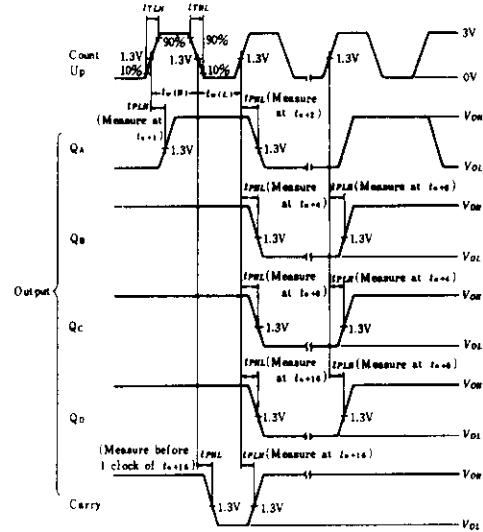
2. All diodes are 1S2074 (H)

Input pulse: $t_{TLH}, t_{THL} \leq 7ns$

Duty Cycle $\leq 50\%$, $PRR=500kHz$ (Data input)

$PRR=1MHz$ (except data input)

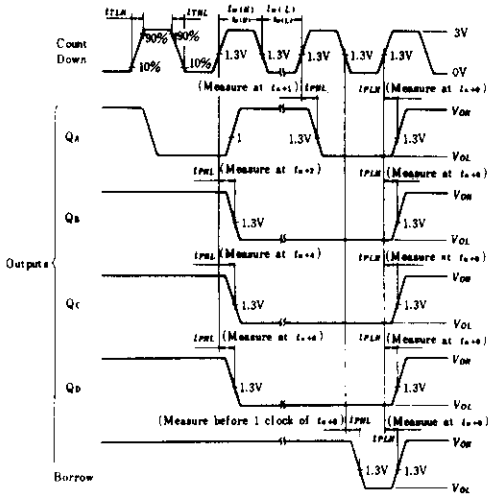
Waveform—1 $f_{max}, t_{PLH}, t_{PHL}$ (Count Up)



Notes) 1. for $f_{max}, t_{TLH} = t_{THL} \leq 2.5ns$.

2. t_n is reference bit time when all outputs are low.

Waveform—2 $f_{max}, t_{PLH}, t_{PHL}$ (Count Down)

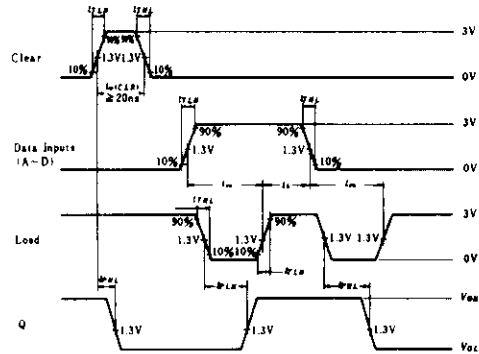


Notes) 1. Input pulse: $t_{TLH} \leq 7ns, t_{THL} \leq 7ns, PRR=1MHz$, duty cycle 50%

2. for $f_{max}, t_{TLH}, t_{THL} \leq 2.5ns$

3. t_n is reference bit time when all outputs are high.

Waveform—3 t_{PLH}, t_{PHL} (Load, Clear $\rightarrow Q$)

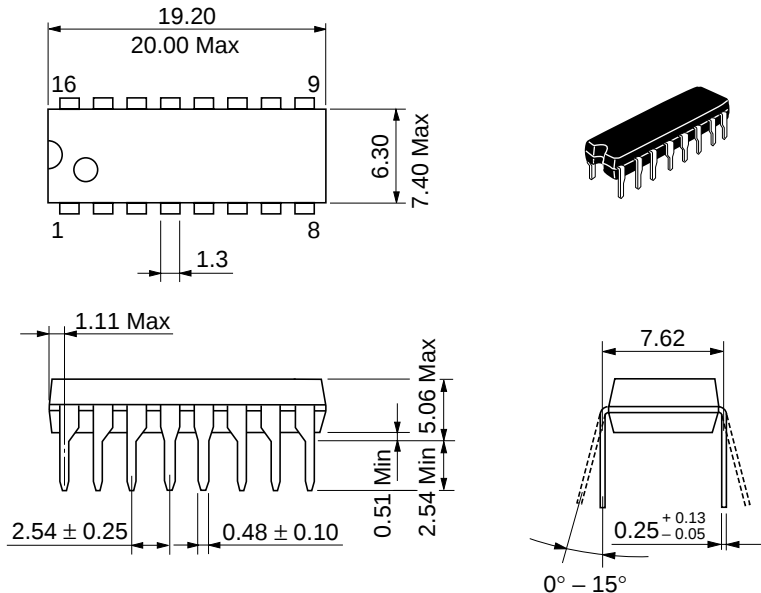


Note) Input pulse: $t_{TLH} \leq 7ns, t_{THL} \leq 7ns$

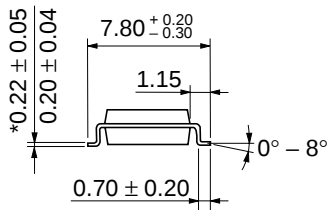
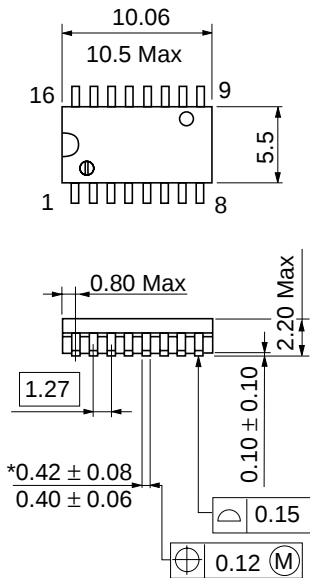
2) Testing Table

Item	From input to output	Inputs								Outputs					
		CLR	Load	Up	Down	A	B	C	D	Q _A	Q _B	Q _C	Q _D	Carry	Borrow
f_{max}	Up Count	GND	4.5V	IN	4.5V	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	—
	Down Count	GND	4.5V	4.5V	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT	—	OUT
t_{PLH}	Up Count	GND	4.5V	IN	4.5V	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	—
	Down Count	GND	4.5V	4.5V	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT	—	OUT
t_{PHL}	Load $\rightarrow Q$	GND	IN	GND	GND	IN	IN	IN	IN	OUT	OUT	OUT	OUT	—	—
	Clear $\rightarrow Q$	IN	IN*	GND	GND	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT	—	—

* for initialized

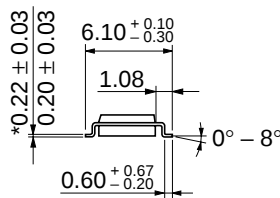
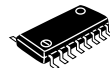


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

*Dimension including the plating thickness
Base material dimension



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL	NorthAmerica	:	http://semiconductor.hitachi.com/
	Europe	:	http://www.hitachi-eu.com/hel/ecg
	Asia (Singapore)	:	http://www.has.hitachi.com.sg/grp3/sicd/index.htm
	Asia (Taiwan)	:	http://www.hitachi.com.tw/E/Product/SICD_Frame.htm
	Asia (HongKong)	:	http://www.hitachi.com.hk/eng/bo/grp3/index.htm
	Japan	:	http://www.hitachi.co.jp/Sicd/indx.htm

For further information write to:

Hitachi Semiconductor (America) Inc. 179 East Tasman Drive, San Jose, CA 95134 Tel: <1> (408) 433-1990 Fax: <1> (408) 433-0223	Hitachi Europe GmbH Electronic components Group Dornacher Straße 3 D-85622 Feldkirchen, Munich Germany Tel: <49> (89) 9 9180-0 Fax: <49> (89) 9 29 30 00 Hitachi Europe Ltd. Electronic Components Group. Whitebrook Park Lower Cookham Road Maidenhead Berkshire SL6 8YA, United Kingdom Tel: <44> (1628) 585000 Fax: <44> (1628) 778322
--	---

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building, No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

Copyright ' Hitachi, Ltd., 1999. All rights reserved. Printed in Japan.