

HM514400A/AL/ASL Series

T-46-23-18

1,048,576-word × 4-bit Dynamic RAM

HITACHI/ LOGIC/ARRAYS/MEM

The Hitachi HM514400A/AL/ASL is a CMOS dynamic RAM organized 1,048,576-word × 4-bit. HM514400A/AL/ASL has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514400A/AL/ASL offers fast page mode as a high speed access mode.

Multiplexed address input permits the HM514400A/AL/ASL to be packaged in standard 20-pin plastic SOJ, 20-pin plastic ZIP, 20-pin TSOP, and 20-pin ST-ZIP.

Features

- Single 5 V (±10%)
- High speed
 - Access time
60 ns/70 ns/80 ns (max)
- Low power dissipation
 - Active mode
605 mW/550 mW/495 mW (max)
 - Standby mode 11 mW (max)
0.83 mW (L-version)
0.55 mW (SL-version)
- Fast page mode capability
- 1,024 refresh cycles: 16 ms
1,024 refresh cycles: 128 ms (L-version)
- 3 variations of refresh
 - RAS-only refresh
 - CAS-before-RAS refresh
 - Hidden refresh
- Test function
- Battery back up operation (L-version)
- Data retention operation (SL-version)

Ordering Information

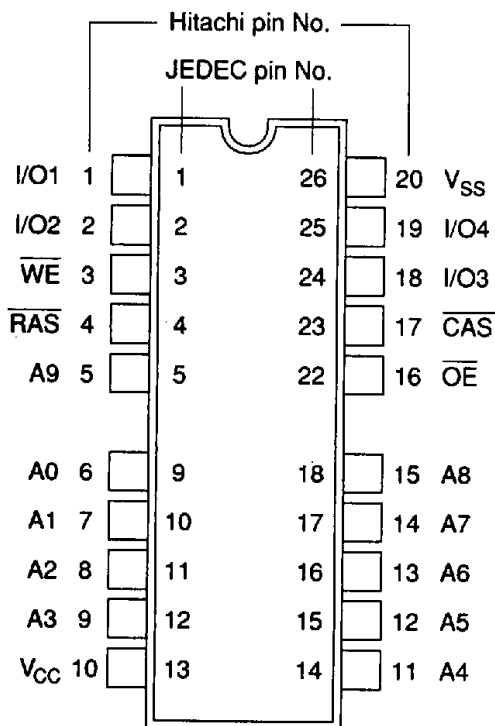
Type No.	Access time	Package
HM514400AJ/ALJ/ASLJ-6	60 ns	350-mil
HM514400AJ/ALJ/ASLJ-7	70 ns	20-pin
HM514400AJ/ALJ/ASLJ-8	80 ns	plastic SOJ (CP-20DA)
HM514400AS/ALS/ASLS-6	60 ns	300-mil
HM514400AS/ALS/ASLS-7	70 ns	20-pin
HM514400AS/ALS/ASLS-8	80 ns	plastic SOJ (CP-20D)
HM514400AZ/ALZ/ASLZ-6	60 ns	400-mil
HM514400AZ/ALZ/ASLZ-7	70 ns	20-pin
HM514400AZ/ALZ/ASLZ-8	80 ns	plastic ZIP (ZP-20)
HM514400AT/ALT/ASLT-6	60 ns	20-pin
HM514400AT/ALT/ASLT-7	70 ns	plastic
HM514400AT/ALT/ASLT-8	80 ns	TSOP I (TFP-20DA)
HM514400AR/ALR/ASLR-6	60 ns	20-pin
HM514400AR/ALR/ASLR-7	70 ns	plastic
HM514400AR/ALR/ASLR-8	80 ns	TSOP I reverse type (TFP-20DAR)
HM514400ATT/ALTT/ASLTT-6	60 ns	20-pin
HM514400ATT/ALTT/ASLTT-7	70 ns	plastic
HM514400ATT/ALTT/ASLTT-8	80 ns	TSOP II (TTP-20D)
HM514400ARR/ALRR/ASLRR-6	60 ns	20-pin
HM514400ARR/ALRR/ASLRR-7	70 ns	plastic
HM514400ARR/ALRR/ASLRR-8	80 ns	TSOP II reverse type (TTP-20DR)
HM514400ATZ/ALTZ-6	60 ns	20-pin
HM514400ATZ/ALTZ-7	70 ns	plastic
HM514400ATZ/ALTZ-8	80 ns	ST-ZIP (ZP-20S)

HM514400A/AL/ASL Series

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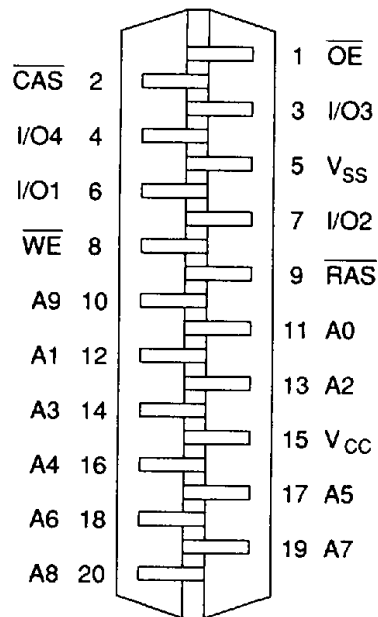
Pin Arrangement

HM514400AJ / ALJ / ASLJ Series
HM514400AS / ALS / ASLS Series



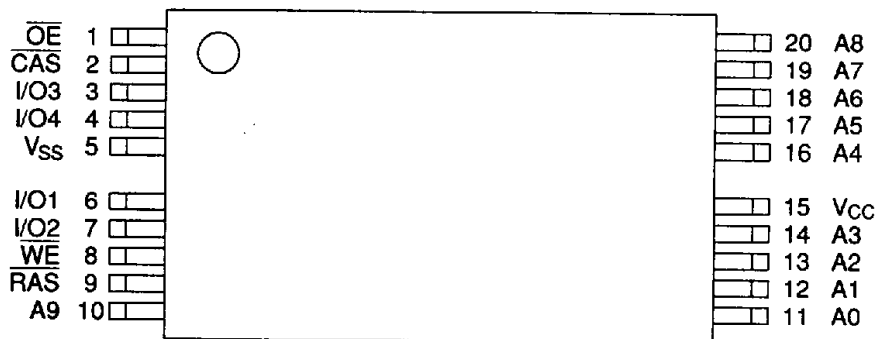
(Top View)

HM514400AZ / ALZ / ASLZ Series
HM514400ATZ/ALTZ Series



(Bottom View)

HM514400AT / ALT / ASLT Series



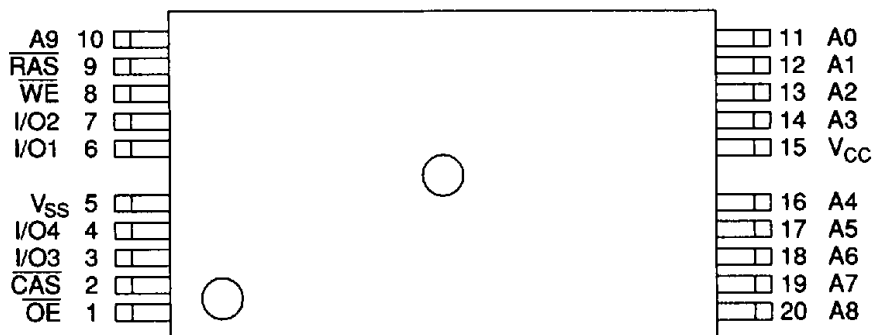
(Top View)

HM514400A/AL/ASL Series

Pin Arrangement (cont)

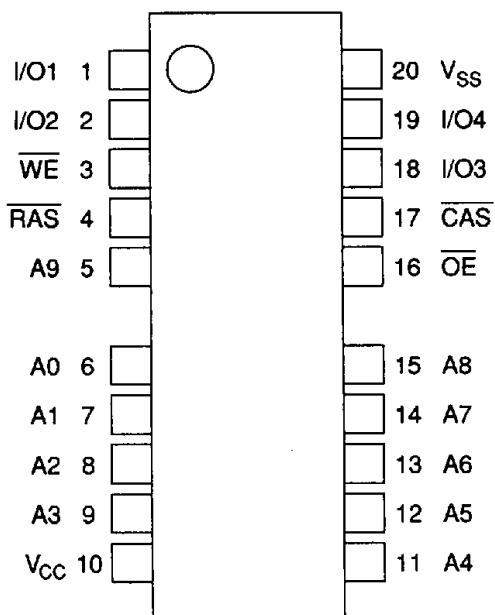
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HM514400AR / ALR / ASLR Series



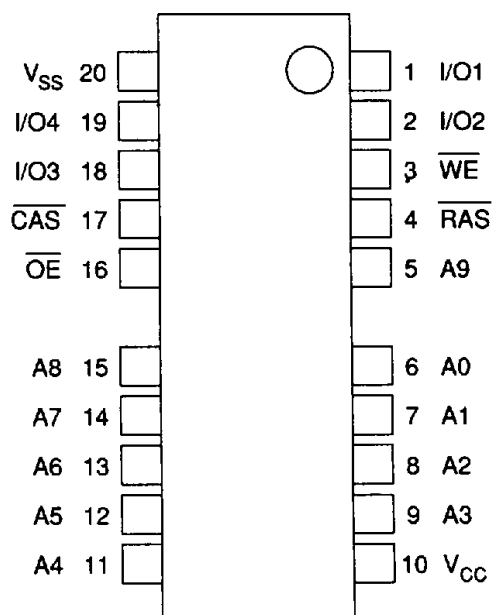
(Top View)

HM514400ATT / ALTT / ASLTT Series



(Top View)

HM514400ARR / ALRR / ASLRR Series



(Top View)

HM514400A/AL/ASL Series

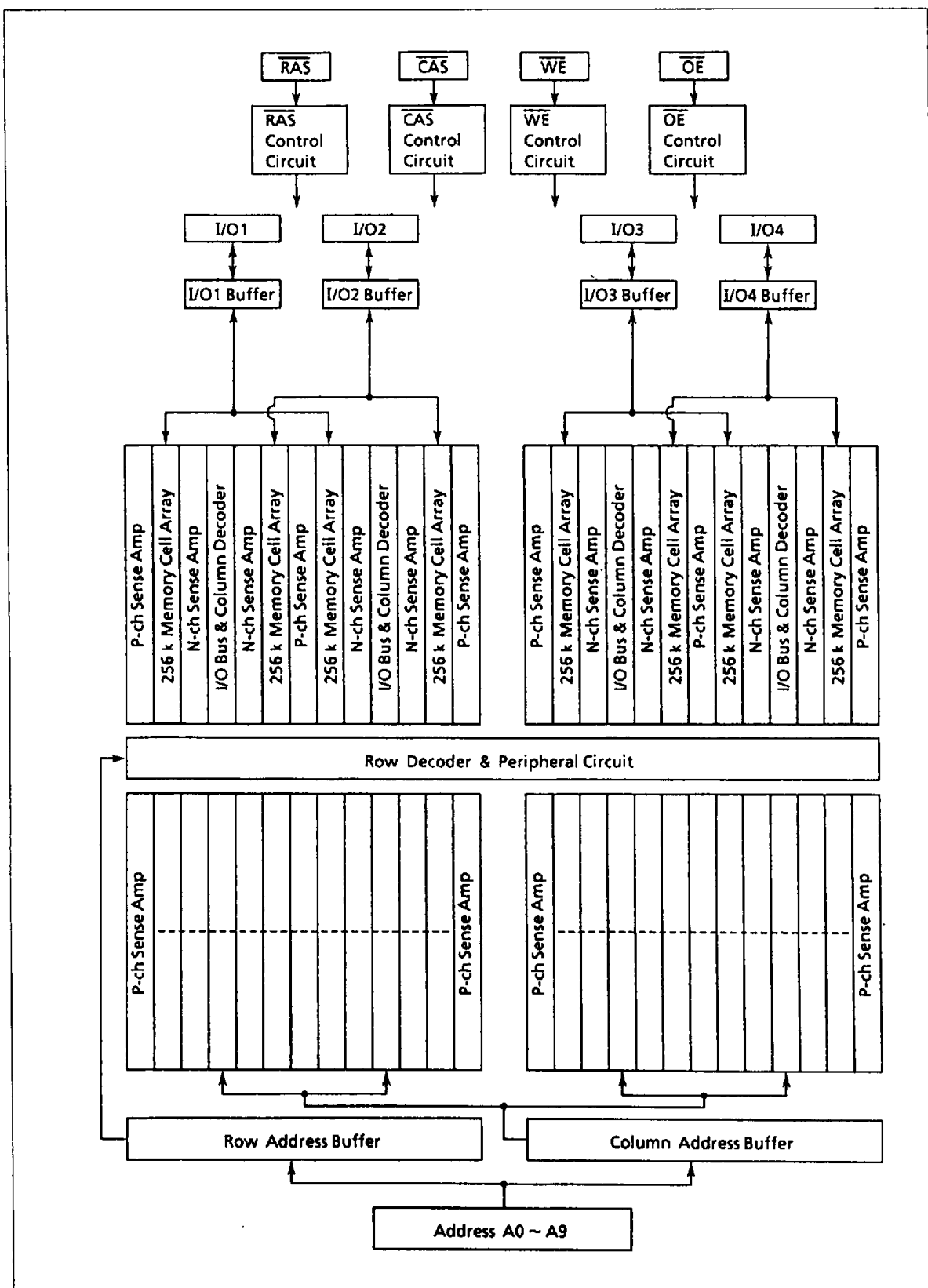
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Pin Description

Pin name	Function
A0 – A9	Address input
A0 – A9	Refresh address input
I/O1 – I/O4	Data-in/data-out
RAS	Row address strobe
CAS	Column address strobe

Pin name	Function
WE	Read/write enable
OE	Output enable
V _{CC}	Power (+5 V)
V _{SS}	Ground

Block Diagram



HM514400A/AL/ASL Series**HITACHI/ LOGIC/ARRAYS/MEM****Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Operating temperature (SL-version)	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)
 ($T_a = 0$ to +60°C (SL-version))

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
		4.0	—	5.5	V	1, 2
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	-1.0	—	0.8	V	1

Notes: 1. All voltage referenced to V_{SS}
 2. Only for data retention operation (SL-version)

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HM514400A/AL/ASL Series

DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$)
($T_a = 0$ to $+60^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$ (SL-version))

Parameter	Symbol	HM514400A -6		HM514400A -7		HM514400A -8		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Operating current	I_{CC1}	—	110	—	100	—	90	mA	RAS, CAS cycling $t_{RC} = \text{min}$	1, 2
Standby current	I_{CC2}	—	2	—	2	—	2	mA	TTL interface RAS, CAS = V_{IH} Dout = High-Z	
		—	1	—	1	—	1	mA	CMOS interface RAS, CAS $\geq$ $V_{CC} - 0.2\text{ V}$ Dout = High-Z	
Standby current (L-version)		—	150	—	150	—	150	μA	CMOS interface RAS, CAS = V_{IH}	4
Standby current (SL-version)		—	100	—	100	—	100	μA	WE, OE, address, Din = V_{IH} or V_{IL} Dout = High-Z	
RAS-only refresh current	I_{CC3}	—	110	—	100	—	90	mA	$t_{RC} = \text{min}$	2
Standby current	I_{CC5}	—	5	—	5	—	5	mA	RAS = V_{IH} CAS = V_{IL} Dout = enable	1
CAS-before-RAS refresh current	I_{CC6}	—	110	—	100	—	90	mA	$t_{RC} = \text{min}$	
Fast page mode current	I_{CC7}	—	110	—	100	—	90	mA	$t_{PC} = \text{min}$	1, 3
Battery back up operation current (CBR refresh) (L-version)	I_{CC10}	—	200	—	200	—	200	μA	$t_{RC} = 125\text{ }\mu\text{s}$ $t_{RAS} \leq 1\text{ }\mu\text{s}$ WE = V_{IH} , CAS = V_{IL} OE, address, Din = V_{IH} or V_{IL} Dout = High-Z	4
Data retention current (CBR refresh) (SL-version)		—	150	—	150	—	150	μA	$t_{RC} = 250\text{ }\mu\text{s}$ $t_{RAS} \leq 200\text{ ns}$ WE = V_{IH} , CAS = V_{IL} OE, address, Din = V_{IH} or V_{IL} Dout = High-Z $4.0\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	4

HM514400A/AL/ASL Series**HITACHI/ LOGIC/ARRAYS/MEM**

DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$)
 ($T_a = 0$ to $+60^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$ (SL-version))
 (cont)

Parameter	Symbol	HM514400A -6		HM514400A -7		HM514400A -8		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	$0\text{ V} \leq V_{in} \leq 7\text{ V}$	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	$0\text{ V} \leq V_{out} \leq 7\text{ V}$ Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = -5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

- Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
 2. Address can be changed twice or less while $\overline{RAS} = V_{IL}$.
 3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.
 4. $V_{CC} - 0.2\text{ V} \leq V_{IH} \leq 6.5\text{ V}$, $0\text{ V} \leq V_{IL} \leq 0.2\text{ V}$.

Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1, 3
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, data-out)	$C_{I/O}$	—	10	pF	1, 2

- Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. $\overline{CAS} = V_{IH}$ to disable Dout
 3. C_{I1} (max) = 7 pF for HM514100ATZ/ALTZ Series.

HM514400A/AL/ASL Series

AC Characteristics ($T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$)*1, *14, *15, *16
($T_a = 0^\circ\text{C}$ to $+60^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$ (SL-version))

Test Conditions

Input rise and fall times: 5 ns
Input timing reference levels: 0.8 V, 2.4 V
Output load: 2 TTL gate + C_L (100 pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

Parameter	Symbol	HM514400A -6		HM514400A -7		HM514400A -8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110	—	130	—	150	—	ns	
RAS precharge time	t_{RP}	40	—	50	—	60	—	ns	
RAS pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns	19
CAS pulse width	t_{CAS}	15	10000	20	10000	20	10000	ns	20
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	15	—	ns	
RAS to CAS delay time	t_{RCD}	20	45	20	50	20	60	ns	8
RAS to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	9
RAS hold time	t_{RSH}	15	—	20	—	20	—	ns	
CAS hold time	t_{CSH}	60	—	70	—	80	—	ns	
CAS to RAS precharge time	t_{CRP}	10	—	10	—	10	—	ns	
OE to Din delay time	t_{ODD}	15	—	20	—	20	—	ns	
OE delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	
CAS setup time from Din	t_{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7

HM514400A/AL/ASL Series
HITACHI/ LOGIC/ARRAYS/MEM
Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters) (cont)

Parameter	Symbol	HM514400A -6		HM514400A -7		HM514400A -8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Refresh period	t_{REF}	—	16	—	16	—	16	ms	
Refresh period (L-version)	t_{REF}	—	128	—	128	—	128	ms	
Refresh period (SL-version)	t_{REF}	—	256	—	256	—	256	ms	21

Read Cycle

Parameter	Symbol	HM514400A -6		HM514400A -7		HM514400A -8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Access time from RAS	t_{RAC}	—	60	—	70	—	80	ns	2, 3, 17
Access time from CAS	t_{CAC}	—	15	—	20	—	20	ns	3, 4, 13, 17
Access time from address	t_{AA}	—	30	—	35	—	40	ns	3, 5, 13, 17
Access time from OE	t_{OAC}	—	15	—	20	—	20	ns	3, 17
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to CAS	t_{RCH}	0	—	0	—	0	—	ns	18
Read command hold time to RAS	t_{RRH}	0	—	0	—	0	—	ns	18
Column address to RAS lead time	t_{RAL}	30	—	35	—	40	—	ns	
Output buffer turn-off time	t_{OFF1}	0	15	0	20	0	20	ns	6
Output buffer turn-off to OE	t_{OFF2}	0	15	0	20	0	20	ns	6
CAS to Din delay time	t_{CDD}	15	—	20	—	20	—	ns	
OE pulse width	t_{OEP}	15	—	20	—	20	—	ns	

HM514400A/AL/ASL Series
Write Cycle
HITACHI/ LOGIC/ARRAYS/MEM

Parameter	Symbol	HM514400A -6		HM514400A -7		HM514400A -8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command setup time	t _{WCS}	0	—	0	—	0	—	ns	10
Write command hold time	t _{WCH}	15	—	15	—	15	—	ns	
Write command pulse width	t _{WP}	10	—	10	—	10	—	ns	
Write command to RAS lead time	t _{RWL}	15	—	20	—	20	—	ns	
Write command to CAS lead time	t _{CWL}	15	—	20	—	20	—	ns	
Data-in setup time	t _{DS}	0	—	0	—	0	—	ns	11
Data-in hold time	t _{DH}	15	—	15	—	15	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514400A -6		HM514400A -7		HM514400A -8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	t _{RWC}	150	—	180	—	200	—	ns	
RAS to WE delay time	t _{RWD}	80	—	95	—	105	—	ns	10
CAS to WE delay time	t _{CWD}	35	—	45	—	45	—	ns	10
Column address to WE delay time	t _{AWD}	50	—	60	—	65	—	ns	10
OE hold time from WE	t _{OEH}	15	—	20	—	20	—	ns	

HM514400A/AL/ASL Series

HITACHI/ LOGIC/ARRAYS/MEM

Refresh Cycle

Parameter	Symbol	HM514400A -6		HM514400A -7		HM514400A -8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
CAS setup time (CAS-before-RAS refresh cycle)	t _{CSR}	10	—	10	—	10	—	ns	
CAS hold time (CAS-before-RAS refresh cycle)	t _{CHR}	10	—	10	—	10	—	ns	
RAS precharge to CAS hold time	t _{RPC}	10	—	10	—	10	—	ns	
CAS precharge time in normal mode	t _{CPN}	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM514400A -6		HM514400A -7		HM514400A -8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Fast page mode cycle time	t _{PC}	40	—	45	—	50	—	ns	
Fast page mode CAS precharge time	t _{CP}	10	—	10	—	10	—	ns	
Fast page mode RAS pulse width	t _{RASC}	—	100000	—	100000	—	100000	ns	12
Access time from CAS precharge	t _{ACP}	—	35	—	40	—	45	ns	3, 13, 17
RAS hold time from CAS precharge	t _{RHCP}	35	—	40	—	45	—	ns	

Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM514400A -6		HM514400A -7		HM514400A -8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Fast page mode read-modify-write cycle time	t _{PCM}	80	—	95	—	100	—	ns	
CAS precharge to WE delay time	t _{CPW}	55	—	65	—	70	—	ns	10

HITACHI/ LOGIC/ARRAYS/MEM **HM514400A/AL/ASL Series****Test Mode Cycle**

Parameter	Symbol	HM514400A -6		HM514400A -7		HM514400A -8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Test mode WE setup time	t _{WS}	0	—	0	—	0	—	ns	
Test mode WE hold time	t _{WH}	10	—	10	—	10	—	ns	

Counter Test Cycle

Parameter	Symbol	HM514400A -6		HM514400A -7		HM514400A -8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
CAS precharge time in counter test cycle	t _{CPT}	40	—	40	—	40	—	ns	

- Notes:
1. AC measurements assume $t_T = 5$ ns.
 2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 4. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$.
 5. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \geq t_{RAD}(\text{max})$.
 6. $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 7. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 8. Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
 9. Operation with the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RAD}(\text{max})$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
 10. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{AWD} \geq t_{AWD}(\text{min})$ and $t_{CPW} \geq t_{CPW}(\text{min})$ the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 11. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in an early write cycle and to WE leading edge in a delayed write or a read-modify-write cycle.
 12. t_{RASC} defines $\overline{\text{RAS}}$ pulse width in fast page mode cycles.
 13. Access time is determined by the longest of t_{AA} or t_{CAC} or t_{ACP} .
 14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (RAS-only refresh cycle or $\overline{\text{CAS}}$ -before-RAS refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before-RAS refresh cycles is required.
 15. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffers prior to applying data to the device.

HM514400A/AL/ASL Series **HITACHI/ LOGIC/ARRAYS/MEM**

16. Test mode operation specified in this data sheet is 2-bit test function controlled by control address bits – CA0. This test mode operation can be performed by $\overline{WE}$ -and- $\overline{CAS}$ -before- $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of two test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. In order to end this test mode operation, perform a $\overline{RAS}$ -only refresh cycle or a $\overline{CAS}$ -before- $\overline{RAS}$ refresh cycle.
17. In a test mode read cycle, the value of t_{RAC} , t_{CAC} , t_{AA} , t_{OAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
18. Either t_{RCH} or t_{RRH} must be satisfied.
19. $t_{RAS}(\text{min}) = t_{RWD}(\text{min}) + t_{RWL}(\text{min}) + t_T$ in read-modify-write cycle.
20. $t_{CAS}(\text{min}) = t_{CWD}(\text{min}) + t_{CWL}(\text{min}) + t_T$ in read-modify-write cycle.
21. t_{REF} is 16 ms without data retention.