

HM534251A Series — HITACHI/ LOGIC/ARRAYS/MEM

262144-word × 4-bit Multiport CMOS Video RAM

T-46-23-20

The HM534251A is a 1-Mbit multiport video RAM equipped with a 256-kword × 4-bit dynamic RAM and a 512-word × 4-bit SAM (serial access memory). Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has write mask function.

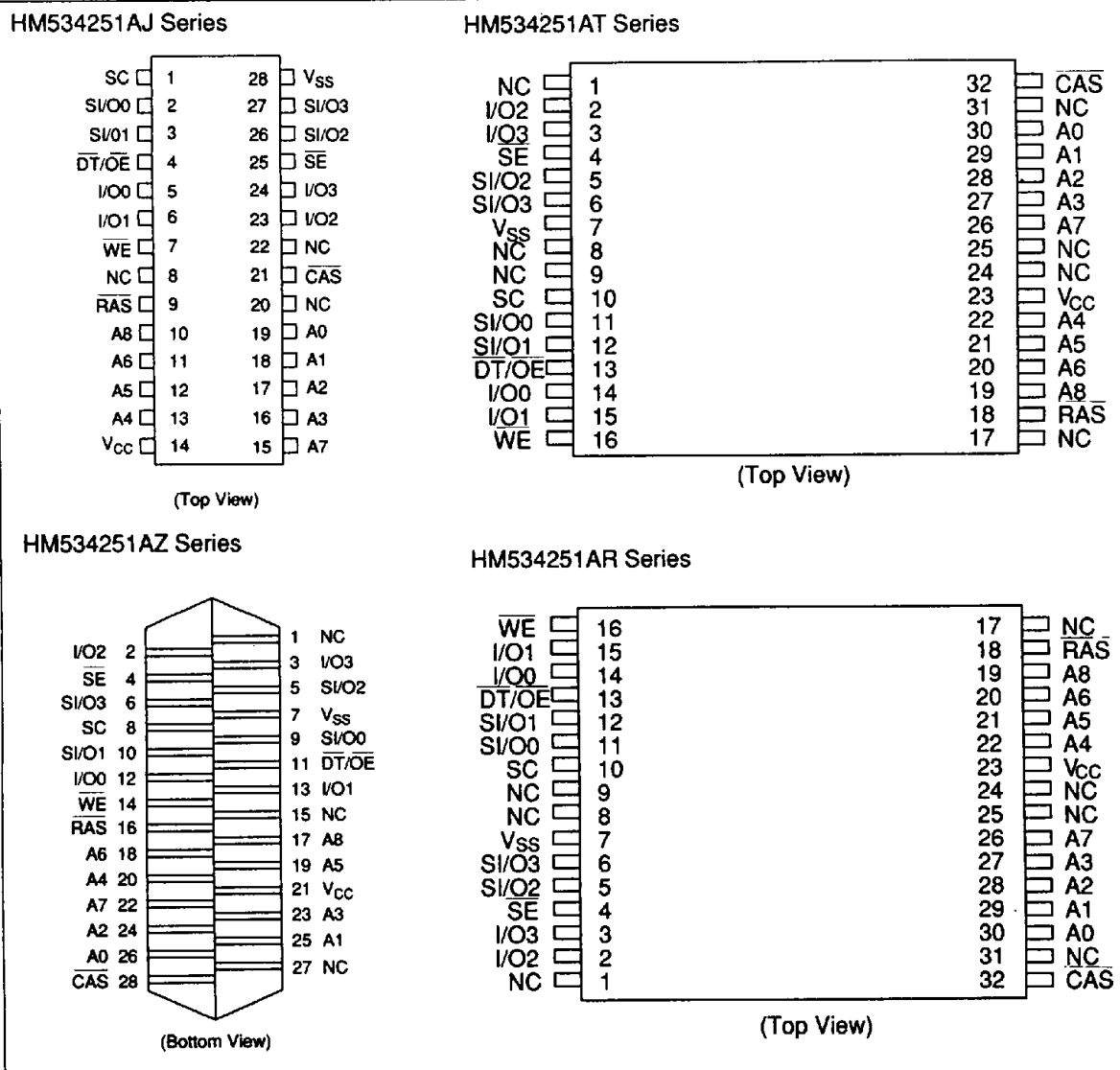
Features

- Multiport organization
 - Asynchronous and simultaneous operation of RAM and SAM capability
 - RAM: 256 kword × 4 bit
 - SAM: 512 word × 4 bit
- Access time
 - RAM: 60 ns/70 ns/80 ns/100 ns max
 - SAM: 20 ns/22 ns/25 ns/25 ns max
- Cycle time
 - RAM: 125 ns/135 ns/150 ns/180 ns min
 - SAM: 25 ns/25 ns/30 ns/30 ns min
- Low power
 - Active RAM: 413 mW max
 - SAM: 275 mW max
 - Standby 38.5 mW max
- High-speed page mode capability
- Mask write mode capability
- Bidirectional data transfer cycle between RAM and SAM capability
- Real time read transfer cycle capability
- 3 variations of refresh (8 ms/512 cycles)
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package
HM534251AJ-6	60 ns	400-mil 28-pin plastic SOJ (CP-28D)
HM534251AJ-7	70 ns	
HM534251AJ-8	80 ns	
HM534251AJ-10	100 ns	
HM534251AZ-6	60 ns	400-mil 28-pin plastic ZIP (ZP-28)
HM534251AZ-7	70 ns	
HM534251AZ-8	80 ns	
HM534251AZ-10	100 ns	
HM534251AT-6	60 ns	8 mm × 14 mm 32-pin TSOP type I (TFP-32DA)
HM534251AT-7	70 ns	
HM534251AT-8	80 ns	
HM534251AT-10	100 ns	
HM534251AR-6	60 ns	8 mm × 14 mm 32-pin TSOP type I reverse (TFP-32DAR)
HM534251AR-7	70 ns	
HM534251AR-8	80 ns	
HM534251AR-10	100 ns	

Pin Arrangement



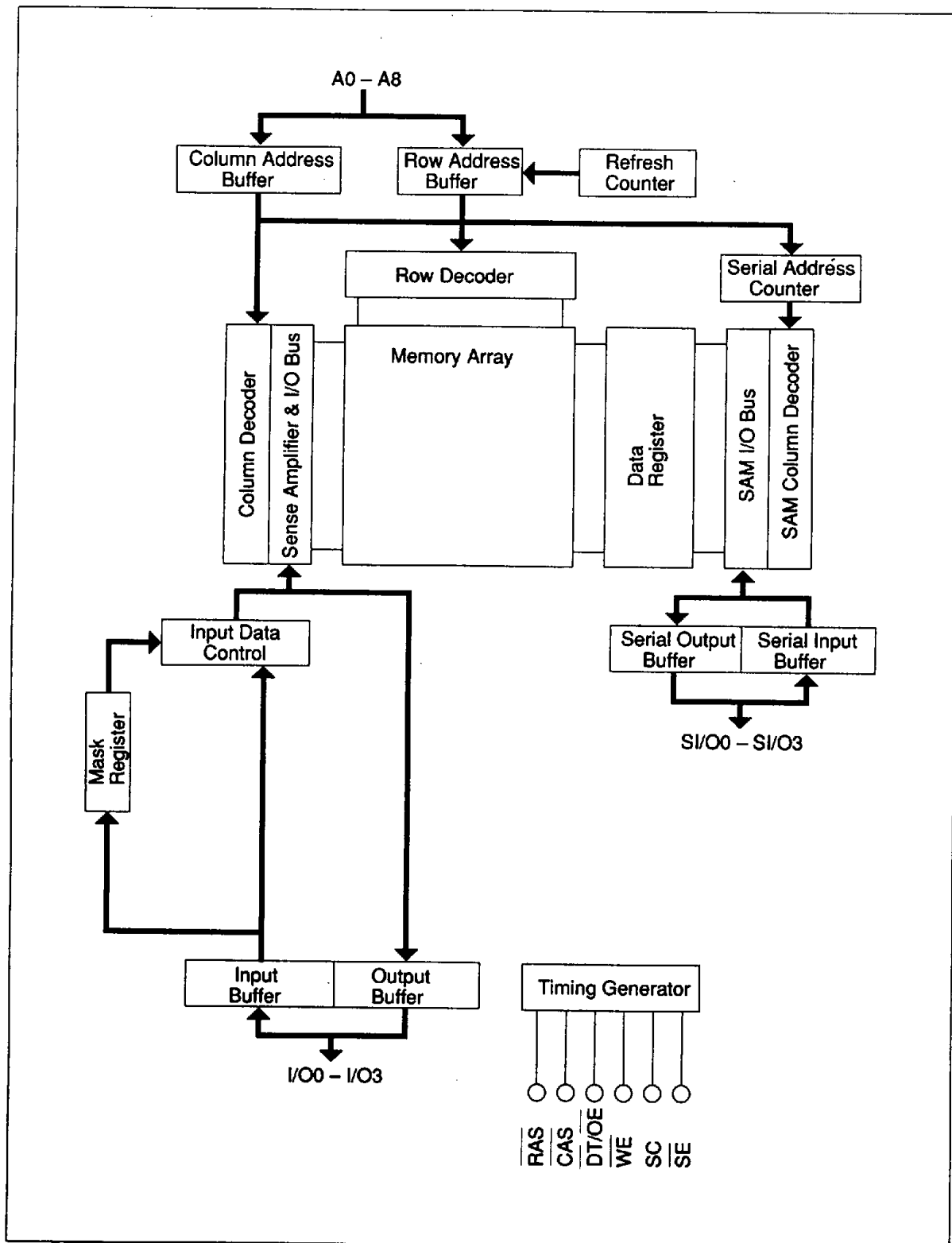
Pin Description

Pin name	Function	Pin name	Function
A0 – A8	Address inputs	DT/OE	Data transfer/Output enable
I/O0 – I/O3	RAM port data inputs/outputs	SC	Serial clock
SI/O0 – SI/O3	SAM port data inputs/outputs	SE	SAM port enable
RAS	Row address strobe	V _{CC}	Power supply
CAS	Column address strobe	V _{SS}	Ground
WE	Write enable	NC	No connection

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Block Diagram



Pin Functions

RAS (input pin): $\overline{\text{RAS}}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{\text{RAS}}$. The input level of these signals determine the operation cycle of the HM534251A.

Table 1. Operation Cycles of the HM534251A

Input level at the falling edge of RAS

CAS	DT/OE	WE	SE	Operation mode
L	X	X	X	CBR refresh
H	L	L	L	Write transfer
H	L	L	H	Pseudo transfer
H	L	H	X	Read transfer
H	H	L	X	Read/mask write
H	H	H	X	Read/write

Note: X : Don't care.

CAS (input pin): Column address is fetched into chip at the falling edge of $\overline{\text{CAS}}$. $\overline{\text{CAS}}$ controls output impedance of I/O in RAM.

A0-A8 (input pins): Row address is determined by A0-A8 level at the falling edge of $\overline{\text{RAS}}$. Column address is determined by A0-A8 level at the falling edge of $\overline{\text{CAS}}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

WE (input pin): $\overline{\text{WE}}$ pin has two functions at the falling edge of $\overline{\text{RAS}}$ and after. When $\overline{\text{WE}}$ is low at the falling edge of $\overline{\text{RAS}}$, the HM534251A turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{\text{WE}}$ level at the falling edge of $\overline{\text{RAS}}$ is don't care in read cycle.) When $\overline{\text{WE}}$ is high at the falling edge of $\overline{\text{RAS}}$, a normal write cycle is executed. After that, $\overline{\text{WE}}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{\text{WE}}$ level at the falling edge of $\overline{\text{RAS}}$. When $\overline{\text{WE}}$ is low, data is transferred

from SAM to RAM (data is written into RAM), and when $\overline{\text{WE}}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O0 - I/O3 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{\text{RAS}}$ (in mask write mode). Data is written only to high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

DT/OE (input pin): $\overline{\text{DT/OE}}$ pin functions as $\overline{\text{DT}}$ (data transfer) pin at the falling edge of $\overline{\text{RAS}}$ and as $\overline{\text{OE}}$ (output enable) pin after that. When $\overline{\text{DT}}$ is low at the falling edge of $\overline{\text{RAS}}$, this cycle becomes a transfer cycle. When $\overline{\text{DT}}$ is high at the falling edge of $\overline{\text{RAS}}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data outputs from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is fetched into the SAM data register.

SE (input pin): $\overline{\text{SE}}$ pin activates SAM. When $\overline{\text{SE}}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not fetched into the SAM data register in serial write cycle. $\overline{\text{SE}}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O0-SI/O3 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

Operation of HM534251A

RAM Read Cycle ($\overline{\text{DT/OE}}$ high and $\overline{\text{CAS}}$ high at the falling edge of $\overline{\text{RAS}}$)

Row address is entered at the $\overline{\text{RAS}}$ falling edge and column address at the $\overline{\text{CAS}}$ falling edge to the device as in standard DRAM. Then, when $\overline{\text{WE}}$ is high and $\overline{\text{DT/OE}}$ is low while $\overline{\text{CAS}}$ is low, the selected address data outputs through I/O pin. At the falling edge of $\overline{\text{RAS}}$, $\overline{\text{DT/OE}}$ and $\overline{\text{CAS}}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{\text{RAS}}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

HM534251A Series**HITACHI/ LOGIC/ARRAYS/MEM****RAM Write Cycle (Early Write, Delayed Write, Read-Modify-Write)**

($\overline{DT}/\overline{OE}$ high and $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

- Normal Mode Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after driving $\overline{RAS}$ low, a write cycle is executed and I/O data is written in the selected addresses. When all 4 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes in high impedance. Data is entered at the $\overline{CAS}$ falling edge.

If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.

If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables read/write at the same address in one cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and driving $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is retained. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode cycle, the mask data is retained during the page access.

High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high and $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle. Note that address access time (t_{AA}), $\overline{RAS}$ to column address delay

time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 512-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 μ s).

Transfer Operation

The HM534251A provides the read transfer cycle, pseudo transfer cycle and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{CAS}$ high and $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$. They have following functions:

- (1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)
Read transfer cycle: RAM to SAM
Write transfer cycle: SAM to RAM
- (2) Determine SI/O state
Read transfer cycle: SI/O output
Pseudo transfer cycle
and write transfer cycle: SI/O input
- (3) Determine first SAM address to access after transferring at column address (SAM start address).

SAM start address must be determined by read transfer cycle or pseudo transfer cycle after power on, and determined for each transfer cycle.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by driving $\overline{DT}/\overline{OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address data (512 x 4-bit) determined by this cycle is transferred to SAM data register synchronously at the rising edge of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from SAM start address determined by column address. In read transfer cycle, $\overline{DT}/\overline{OE}$ must be risen to transfer data from RAM to SAM.

This cycle can access SAM even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge and t_{SDH} (min) specified between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge must be satisfied. (See figure 1.).

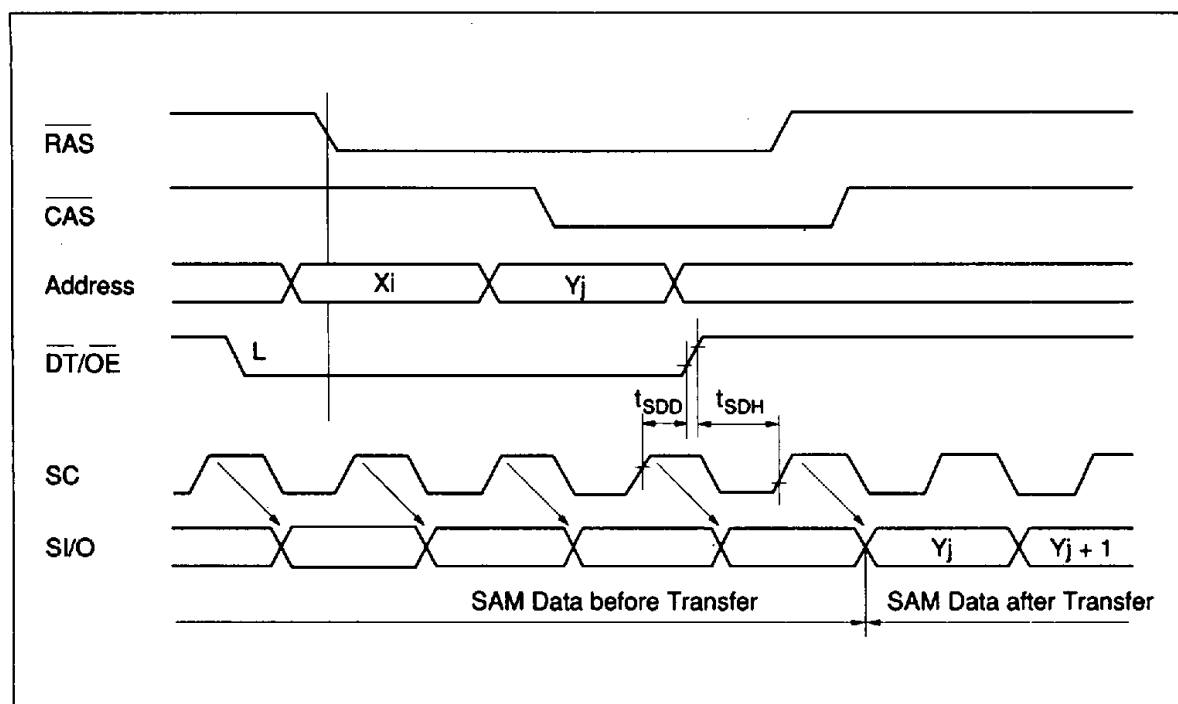


Figure 1. Real Time Read Transfer

When read transfer cycle is executed, SI/O becomes output state by first SAM access. Input must be set high impedance before t_{SZS} (min) of the first SAM access to avoid data contention.

Pseudo Transfer Cycle ($\overline{\text{CAS}}$ high, $\overline{\text{DT/OE}}$ low, $\overline{\text{WE}}$ low and $\overline{\text{SE}}$ high at the falling edge of $\overline{\text{RAS}}$)

Pseudo transfer cycle switches SI/O to input state and set SAM start address without data transfer to RAM.

This cycle starts when $\overline{\text{CAS}}$ is high, $\overline{\text{DT/OE}}$ low, $\overline{\text{WE}}$ low and $\overline{\text{SE}}$ high at the falling edge of $\overline{\text{RAS}}$. Data should be input to SI/O later than t_{SID} (min) after $\overline{\text{RAS}}$ becomes low to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{\text{RAS}}$ becomes high. In this cycle, SAM access is inhibited during $\overline{\text{RAS}}$ low, therefore, SC must not be risen.

Write Transfer Cycle ($\overline{\text{CAS}}$ high, $\overline{\text{DT/OE}}$ low, $\overline{\text{WE}}$ low and $\overline{\text{SE}}$ low at the falling edge of $\overline{\text{RAS}}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined

by the address at the falling edge of $\overline{\text{RAS}}$. The column address is specified as the first address for serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{\text{RAS}}$ becomes high. SAM access is inhibited during $\overline{\text{RAS}}$ low. In this period, SC must not be risen.

Data transferred to SAM by read transfer cycle can be written to other address of RAM by write transfer cycle. However, the address to write data must be the same MSB of row address (AX8) as that of the read transfer cycle.

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When $\overline{\text{SE}}$ is set high, SI/O becomes high impedance, and the internal pointer is incremented by the SC rising. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

HM534251A Series**HITACHI/ LOGIC/ARRAYS/MEM****Serial Write Cycle**

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is fetched into data register at the SC rising edge like in the serial read cycle. If SE is high, SI/O data isn't fetched into data register. Internal pointer is incremented by the SC rising, so SE high can be used as mask data for SAM. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

Refresh**RAM Refresh**

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is executed by accessing all 512 row addresses within 8 ms. There are three refresh cycles: (1) $\overline{\text{RAS}}$ -only refresh cycle, (2) $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{\text{RAS}}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required when all row addresses are accessed within 8 ms.

- (1) $\overline{\text{RAS}}$ -Only Refresh Cycle: $\overline{\text{RAS}}$ -only refresh cycle is executed by activating only $\overline{\text{RAS}}$ cycle with $\overline{\text{CAS}}$ fixed to high after inputting the row address (= refresh address) from external circuits. To distinguish this cycle from data transfer cycle, $\overline{\text{DT/OE}}$ must be high at the falling edge of $\overline{\text{RAS}}$.
- (2) CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{\text{CAS}}$ circuits don't operate.
- (3) Hidden Refresh Cycle: Hidden refresh cycle executes CBR refresh with the data output by reactivating $\overline{\text{RAS}}$ when $\overline{\text{DT/OE}}$ and $\overline{\text{CAS}}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register and selector), organized as fully static circuitry, require no refresh.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Terminal voltage*1	V_T	-1.0 to +7.0	V
Power supply voltage*1	V_{CC}	-0.5 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Note: 1. Relative to V_{SS} .

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Recommended DC Operating Conditions ($T_a = 0$ to $+70^\circ\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage*1	V_{CC}	4.5	5.0	5.5	V
Input high voltage*1	V_{IH}	2.4	—	6.5	V
Input low voltage*1	V_{IL}	-0.5^{*2}	—	0.8	V

- Notes: 1. All voltages referenced to V_{SS} .
2. -3.0 V for pulse width ≤ 10 ns.

DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$)

HM534251A											
		-6		-7		-8		-10		Test conditions	
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	RAM port SAM port
Operating current	I_{CC1}	—	75	—	70	—	60	—	55	mA	RAS, CAS cycling $SC = V_{IL}, SE = V_{IH}$
	I_{CC7}	—	125	—	120	—	100	—	95	mA	$t_{RC} = \min$ $SE = V_{IL}, SC$ cycling $t_{SCC} = \min$
Standby current	I_{CC2}	—	7	—	7	—	7	—	7	mA	RAS, CAS $= V_{IH}$ $SC = V_{IL}, SE = V_{IH}$
	I_{CC8}	—	50	—	50	—	40	—	40	mA	$SE = V_{IL}, SC$ cycling $t_{SCC} = \min$
RAS-only refresh current	I_{CC3}	—	75	—	70	—	60	—	55	mA	RAS cycling $CAS = V_{IH}$ $SC = V_{IL}, SE = V_{IH}$
	I_{CC9}	—	125	—	120	—	100	—	95	mA	$t_{RC} = \min$ $SE = V_{IL}, SC$ cycling $t_{SCC} = \min$
Page mode current	I_{CC4}	—	80	—	80	—	70	—	65	mA	CAS cycling $RAS = V_{IL}$ $SC = V_{IL}, SE = V_{IH}$
	I_{CC10}	—	130	—	130	—	110	—	105	mA	$t_{PC} = \min$ $SE = V_{IL}, SC$ cycling $t_{SCC} = \min$
CAS-before-RAS refresh current	I_{CC5}	—	50	—	45	—	40	—	35	mA	RAS cycling $t_{RC} = \min$ $SC = V_{IL}, SE = V_{IH}$
	I_{CC11}	—	100	—	95	—	80	—	75	mA	$SE = V_{IL}, SC$ cycling $t_{SCC} = \min$
Data transfer current	I_{CC6}	—	80	—	75	—	65	—	60	mA	RAS, CAS cycling $SC = V_{IL}, SE = V_{IH}$
	I_{CC12}	—	130	—	125	—	105	—	100	mA	$t_{RC} = \min$ $SE = V_{IL}, SC$ cycling $t_{SCC} = \min$

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DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$) (cont)

		HM534251A									
		-6		-7		-8		-10		Test conditions	
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	-10	10	μA	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	-10	10	μA	
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V	$I_{OH} = -2\text{ mA}$
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V	$I_{OL} = 4.2\text{ mA}$

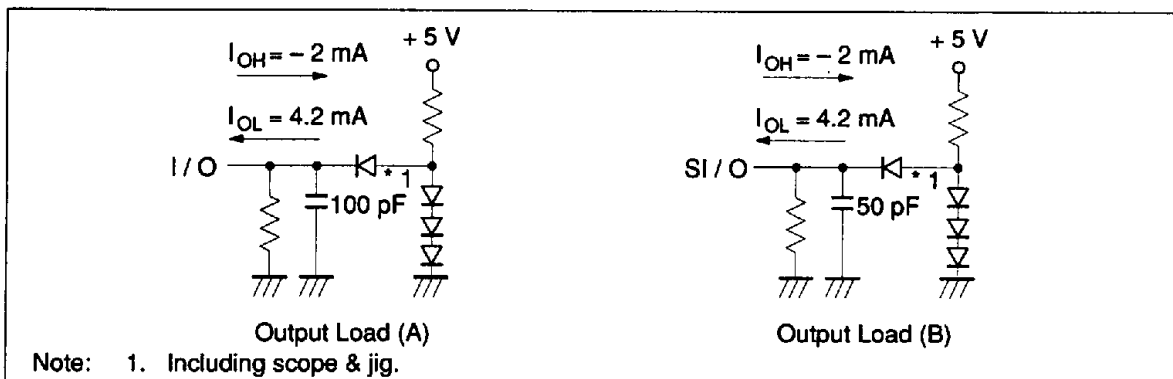
- Note: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.
 2. Address can be changed once while $\overline{\text{RAS}}$ is low and $\overline{\text{CAS}}$ is high.

Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $f = 1\text{ MHz}$, Bias: Clock, I/O = V_{CC} , address = V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clock	C_{I2}	—	—	5	pF
I/O, SI/O	$C_{I/O}$	—	—	7	pF

AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$) *1, *16**Test Conditions**

- Input rise and fall time: 5 ns
- Output load: See figures
- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V



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Common Parameter

		HM534251A									
		-6		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	125	—	135	—	150	—	180	—	ns	
RAS precharge time	t_{RP}	55	—	55	—	60	—	70	—	ns	
RAS pulse width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
CAS pulse width	t_{CAS}	20	—	20	—	20	—	25	—	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	15	—	15	—	ns	
RAS to CAS delay time	t_{RCD}	20	40	20	50	20	60	20	75	ns	²
RAS hold time referenced to CAS	t_{RSH}	20	—	20	—	20	—	25	—	ns	
CAS hold time referenced to RAS	t_{CSH}	60	—	70	—	80	—	100	—	ns	
CAS to RAS precharge time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Transition time (rise to fall)	t_T	3	50	3	50	3	50	3	50	ns	³
Refresh period	t_{REF}	—	8	—	8	—	8	—	8	ms	
DT to RAS setup time	t_{DTS}	0	—	0	—	0	—	0	—	ns	
DT to RAS hold time	t_{DTH}	10	—	10	—	10	—	10	—	ns	
Data-in to CAS delay time	t_{DZC}	0	—	0	—	0	—	0	—	ns	⁴
Data-in to OE delay time	t_{DZO}	0	—	0	—	0	—	0	—	ns	⁴
Output buffer turn-off delay referenced to CAS	t_{OFF1}	—	20	—	20	—	20	—	20	ns	⁵
Output buffer turn-off delay referenced to OE	t_{OFF2}	—	20	—	20	—	20	—	20	ns	⁵

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Read Cycle (RAM), Page Mode Read Cycle

		HM534251A									
		-6		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from RAS	t _{RAC}	—	60	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{\text{CAS}}$	t _{CAC}	—	20	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{\text{OE}}$	t _{OAC}	—	20	—	20	—	20	—	25	ns	7
Address access time	t _{AA}	—	35	—	35	—	40	—	45	ns	7, 9
Read command setup time	t _{RCS}	0	—	0	—	0	—	0	—	ns	
Read command hold time	t _{RCH}	0	—	0	—	0	—	0	—	ns	10
Read command hold time referenced to RAS	t _{RRH}	10	—	10	—	10	—	10	—	ns	10
RAS to column address delay time	t _{RAD}	15	25	15	35	15	40	15	55	ns	2
Column address to RAS lead time	t _{RAL}	35	—	35	—	40	—	45	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t _{CAL}	35	—	35	—	40	—	45	—	ns	
Page mode cycle time	t _{PC}	45	—	45	—	50	—	55	—	ns	
$\overline{\text{CAS}}$ precharge time	t _{CP}	10	—	10	—	10	—	10	—	ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{ACP}	—	40	—	40	—	45	—	50	ns	
Page mode RAS pulse width	t _{RASP}	60	100000	70	100000	80	100000	100	100000	ns	

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Write Cycle (RAM), Page Mode Write Cycle

		HM534251A							
		-6		-7		-8		-10	
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max
Write command setup time	t _{WCS}	0	—	0	—	0	—	0	—
Write command hold time	t _{WCH}	15	—	15	—	15	—	15	—
Write command pulse width	t _{WP}	15	—	15	—	15	—	15	—
Write command to RAS lead time	t _{RWL}	20	—	20	—	20	—	20	—
Write command to CAS lead time	t _{CWL}	20	—	20	—	20	—	20	—
Data-in setup time	t _{DS}	0	—	0	—	0	—	0	—
Data-in hold time	t _{DH}	15	—	15	—	15	—	15	—
WE to RAS setup time	t _{WS}	0	—	0	—	0	—	0	—
WE to RAS hold time	t _{WH}	10	—	10	—	10	—	10	—
Mask data to RAS setup time	t _{MS}	0	—	0	—	0	—	0	—
Mask data to RAS hold time	t _{MH}	10	—	10	—	10	—	10	—
OE hold time referenced to WE	t _{OEH}	20	—	20	—	20	—	20	—
Page mode cycle time	t _{PC}	45	—	45	—	50	—	55	—
CAS precharge time	t _{CP}	10	—	10	—	10	—	10	—
CAS to data-in delay time	t _{CDD}	20	—	20	—	20	—	20	—
Page mode RAS pulse width	t _{RASP}	60	100000	70	100000	80	100000	100	100000

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HM534251A Series
Read-Modify-Write Cycle

		HM534251A									
		-6		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t _{RWC}	175	—	185	—	200	—	230	—	ns	
RAS pulse width (read-modify-write cycle)	t _{RWS}	110	10000	120	10000	130	10000	150	10000	ns	
CAS to WE delay time	t _{CWD}	45	—	45	—	45	—	50	—	ns	14
Column address to WE delay time	t _{AWD}	60	—	60	—	65	—	70	—	ns	14
OE to data-in delay time	t _{ODD}	20	—	20	—	20	—	20	—	ns	12
Access time from RAS	t _{RAC}	—	60	—	70	—	80	—	100	ns	6, 7
Access time form CAS	t _{CAC}	—	20	—	20	—	20	—	25	ns	7, 8
Access time from OE	t _{OAC}	—	20	—	20	—	20	—	25	ns	7
Address access time	t _{AA}	—	35	—	35	—	40	—	45	ns	7, 9
RAS to column address delay time	t _{RAD}	15	25	15	35	15	40	15	55	ns	
Read command setup time	t _{RCS}	0	—	0	—	0	—	0	—	ns	
Write command to RAS lead time	t _{RWL}	20	—	20	—	20	—	20	—	ns	
Write command to CAS lead time	t _{CWL}	20	—	20	—	20	—	20	—	ns	
Write command pulse width	t _{WP}	15	—	15	—	15	—	15	—	ns	
Data-in setup time	t _{DS}	0	—	0	—	0	—	0	—	ns	12
Data-in hold time	t _{DH}	15	—	15	—	15	—	15	—	ns	12
OE hold time referenced to WE	t _{OEH}	20	—	20	—	20	—	20	—	ns	

HITACHI/ LOGIC/ARRAYS/MEM

HM534251A Series

Refresh Cycle

		HM534251A							
		-6		-7		-8		-10	
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max
CAS setup time (CAS-before-RAS refresh)	t _{CSR}	10	—	10	—	10	—	10	—
CAS hold time (CAS-before-RAS refresh)	t _{CHR}	10	—	10	—	10	—	10	—
RAS precharge to CAS hold time	t _{RPC}	10	—	10	—	10	—	10	—

Read Transfer Cycle

		HM534251A							
		-6		-7		-8		-10	
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max
DT hold time referenced to RAS	t _{RDH}	50	10000	60	10000	65	10000	80	10000
DT hold time referenced to CAS	t _{CDH}	20	—	20	—	20	—	25	—
DT hold time referenced to column address	t _{ADH}	25	—	25	—	30	—	30	—
DT precharge time	t _{DTP}	20	—	20	—	20	—	30	—
DT to RAS delay time	t _{DRD}	65	—	65	—	70	—	80	—
SC to RAS setup time	t _{SRS}	25	—	25	—	30	—	30	—
1st SC to RAS hold time	t _{SRH}	60	—	70	—	80	—	100	—
1st SC to CAS hold time	t _{SCH}	25	—	25	—	25	—	25	—
1st SC to column address hold time	t _{SAH}	40	—	40	—	45	—	50	—
Last SC to DT delay time	t _{SDD}	5	—	5	—	5	—	5	—
1st SC to DT hold time	t _{SDH}	10	—	10	—	15	—	15	—
Serial data-in to 1st SC delay time	t _{SZS}	0	—	0	—	0	—	0	—
Serial clock cycle time	t _{SCC}	25	—	25	—	30	—	30	—
SC pulse width	t _{SC}	5	—	5	—	10	—	10	—
SC precharge time	t _{SCP}	10	—	10	—	10	—	10	—

HM534251A Series
HITACHI/ LOGIC/ARRAYS/MEM
Read Transfer Cycle (cont)

		HM534251A							
		-6		-7		-8		-10	
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max
SC access time	t _{SCA}	—	20	—	22	—	25	—	25
Serial data-out hold time	t _{SOH}	5	—	5	—	5	—	5	—
Serial data-in setup time	t _{SIS}	0	—	0	—	0	—	0	—
Serial data-in hold time	t _{SIH}	15	—	15	—	15	—	15	—
RAS to column address delay time	t _{RAD}	15	25	15	35	15	40	15	55
Column address to RAS lead time	t _{RAL}	35	—	35	—	40	—	45	—
DT high hold time from RAS precharge	t _{DTHH}	10	—	10	—	10	—	10	—

Pseudo Transfer Cycle, Write Transfer Cycle

		HM534251A							
		-6		-7		-8		-10	
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max
SE setup time referenced to RAS	t _{ES}	0	—	0	—	0	—	0	—
SE hold time referenced to RAS	t _{EH}	10	—	10	—	10	—	10	—
SC setup time referenced to RAS	t _{SRS}	25	—	25	—	30	—	30	—
RAS to SC delay time	t _{SRD}	20	—	20	—	25	—	25	—
Serial output buffer turn-off time referenced to RAS	t _{SRZ}	10	40	10	40	10	45	10	50
RAS to serial data-in delay time	t _{SID}	40	—	40	—	45	—	50	—
Serial clock cycle time	t _{SCC}	25	—	25	—	30	—	30	—
SC pulse width	t _{SC}	5	—	5	—	10	—	10	—
SC precharge time	t _{SCP}	10	—	10	—	10	—	10	—
SC access time	t _{SCA}	—	20	—	22	—	25	—	25

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Pseudo Transfer Cycle, Write Transfer Cycle (cont)

		HM534251A							
		-6		-7		-8		-10	
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max
SE access time	t _{SEA}	—	20	—	22	—	25	—	25
Serial data-out hold time	t _{SOH}	5	—	5	—	5	—	5	—
Serial write enable setup time	t _{SWS}	5	—	5	—	5	—	5	—
Serial data-in setup time	t _{SIS}	0	—	0	—	0	—	0	—
Serial data-in hold time	t _{SIH}	15	—	15	—	15	—	15	—

Serial Read Cycle, Serial Write Cycle

		HM534251A							
		-6		-7		-8		-10	
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max
Serial clock cycle time	t _{SCC}	25	—	25	—	30	—	30	—
SC pulse width	t _{SC}	5	—	5	—	10	—	10	—
SC precharge width	t _{SCP}	10	—	10	—	10	—	10	—
Access time from SC	t _{SCA}	—	20	—	22	—	25	—	25
Access time from SE	t _{SEA}	—	20	—	22	—	25	—	25
Serial data-out hold time	t _{SOH}	5	—	5	—	5	—	5	—
Serial output buffer turn-off time referenced to SE	t _{SEZ}	—	20	—	20	—	20	—	20
Serial data-in setup time	t _{SIS}	0	—	0	—	0	—	0	—
Serial data-in hold time	t _{SIH}	15	—	15	—	15	—	15	—
Serial write enable setup time	t _{SWS}	5	—	5	—	5	—	5	—
Serial write enable hold time	t _{SWH}	15	—	15	—	15	—	15	—
Serial write disable setup time	t _{SWIS}	5	—	5	—	5	—	5	—
Serial write disable hold time	t _{SWIH}	15	—	15	—	15	—	15	—

HM534251A Series
HITACHI/ LOGIC/ARRAYS/MEM

- Notes:
1. AC measurements assume $t_T = 5$ ns.
 2. When $t_{RCD} > t_{RCD}(\text{max})$ or $t_{RAD} > t_{RAD}(\text{max})$, access time is specified by t_{CAC} or t_{AA} .
 3. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition time t_T is measured between V_{IH} and V_{IL} .
 4. Data input must be floating before output buffer is turned on. In read cycle, read-modify-write cycle and delayed write cycle, either $t_{DZC}(\text{min})$ or $t_{DZO}(\text{min})$ must be satisfied.
 5. $t_{OFF1}(\text{max})$, $t_{OFF2}(\text{max})$ and $t_{SEZ}(\text{max})$ are defined as the time at which the output achieves the open circuit condition ($V_{OH} - 100$ mV, $V_{OL} + 100$ mV).
 6. Assume that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 7. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 8. When $t_{RCD} \geq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$, access time is specified by t_{CAC} .
 9. When $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \geq t_{RAD}(\text{max})$, access time is specified by t_{AA} .
 10. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.
 11. When $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition.
 12. These parameters are specified by the later falling edge of $\overline{\text{CAS}}$ or WE .
 13. Either $t_{CDD}(\text{min})$ or $t_{ODD}(\text{min})$ must be satisfied because output buffer must be turned off by $\overline{\text{CAS}}$ or $\overline{\text{OE}}$ prior to applying data to the device when output buffer is on.
 14. When $t_{AWD} \geq t_{AWD}(\text{min})$ and $t_{CWD} \geq t_{CWD}(\text{min})$ in read-modify-write cycle, the data of the selected address outputs to an I/O pin and input data is written into the selected address. $t_{ODD}(\text{min})$ must be satisfied because output buffer must be turned off by $\overline{\text{OE}}$ prior to applying data to the device.
 15. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
 16. After power-up, pause for 100 μs or more and execute at least 8 initialization cycle (normal memory cycle or refresh cycle), then start operation.
 17. When the serial write cycle is used, at least one SC pulse is required before proper SAM operation after V_{CC} stabilized.
 18. $t_{DTHH}(\text{min})$ must be satisfied only if $\text{DT}/\overline{\text{OE}}$ rises up before RAS rises in a read transfer cycle.