HM538253B Series
HM538254B Series

262,144-word × 8-bit Multiport CMOS Video RAM

HITACHI

Rev. 0.0
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Description

The HM538253B/HM538254B is a 2-Mbit multiport video RAM equipped with a 256-kword × 8-bit dynamic RAM and a 512-word × 8-bit SAM (full-sized SAM). Its RAM and SAM operate independently and asynchronously. The HM538253B/HM538254B is upwardly compatible with the HM534253B/HM538123B except that the pseudo-write-transfer cycle is replaced with masked-write-transfer cycle, which has been approved by JEDEC. Furthermore, several new features have been added to the HM538253B/HM538254B which do not conflict with the conventional features. The stopping column feature realizes allows greater flexibility for split SAM register lengths. Persistent mask is also installed according to the TMS34020 features. The HM538254B has Hyper page mode which enables fast page cycle.

Features

- Multiport organization:RAM and SAM can operate asynchronously and simultaneously:
  - — RAM: 256-kword × 8-bit
  - — SAM: 512-word × 8-bit
- Access time
  - — RAM: 70 ns/80 ns/100 ns max
  - — SAM: 20 ns/23 ns/25 ns max
- Cycle time
  - — RAM: 130 ns/150 ns/180 ns min
  - — SAM: 25 ns/28 ns/30 ns min
- Low power
  - — Active RAM: 605 mW/550 mW/495 mW
    SAM: 358 mW/330 mW/303 mW
  - — Standby 38.5 mW max
- Masked-write-transfer cycle capability
- Stopping column feature capability
- Persistent mask capability
- Fast page mode capability (HM538253B)

Features (cont)

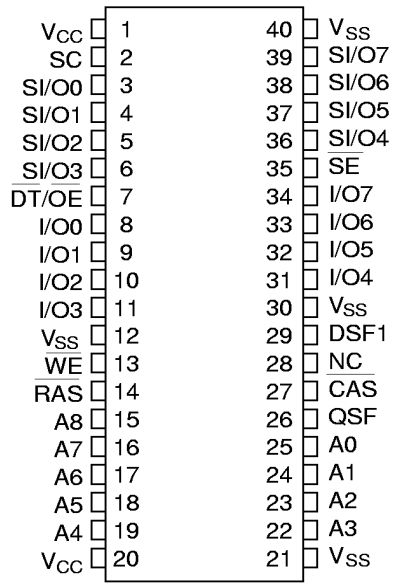
  - — Cycle time: 45 ns/50 ns/55 ns
  - — Power RAM: 605 mW/578 mW/550 mW
- Hyper page mode capability (HM538254B)
  - — Cycle time: 35 ns/40 ns/45 ns
  - — Power RAM: 715 mW/660 mW/605 mW
- Mask write mode capability
- Bidirectional data transfer cycle between RAM and SAM capability
- Split transfer cycle capability
- Block write mode capability
- Flash write mode capability
- 3 variations of refresh (8 ms/512 cycles)
  - — $\overline{\text{RAS}}$-only refresh
  - — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - — Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access Time	Package
HM538253BJ-7	70 ns	400-mil, 40-pin plastic SOJ (CP-40D)
HM538253BJ-8	80 ns	
HM538253BJ-10	100 ns	
HM538254BJ-7	70 ns	
HM538254BJ-8	80 ns	
HM538254BJ-10	100 ns	
HM538253BTT-7	70 ns	44-pin thin small outline package (TTP-44/40DA)
HM538253BTT-8	80 ns	
HM538253BTT-10	100 ns	
HM538254BTT-7	70 ns	
HM538254BTT-8	80 ns	
HM538254BTT-10	100 ns	

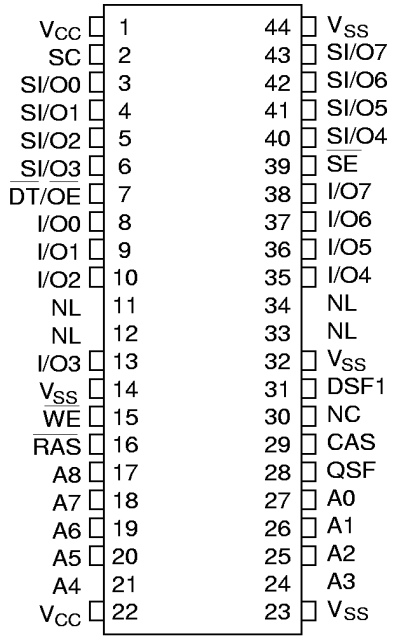
Pin Arrangement

HM538253BJ Series
HM538254BJ Series



(Top view)

HM538253BTT Series
HM538254BTT Series

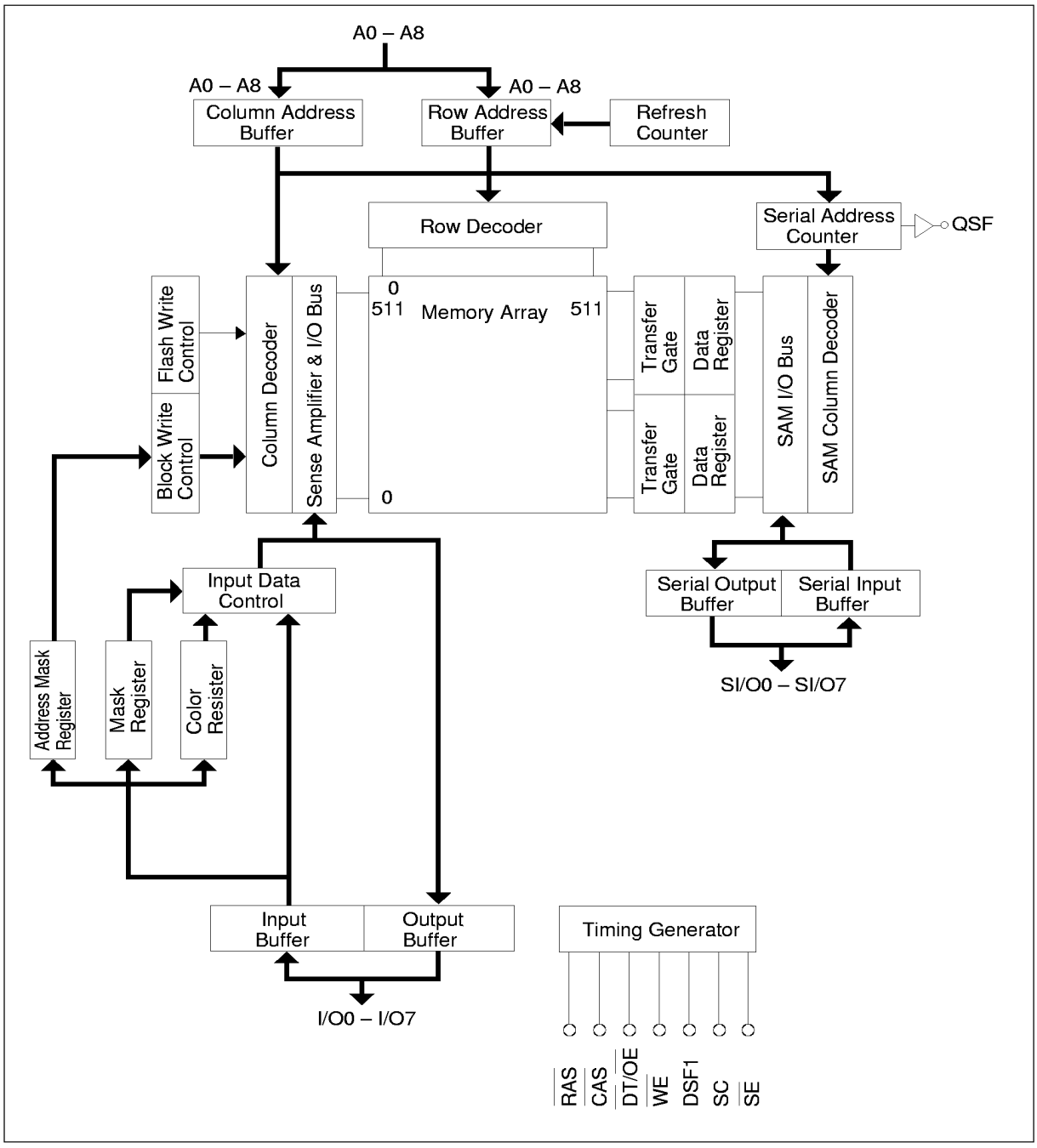


(Top view)

Pin Description

Pin Name	Function
A0-A8	Address inputs
I/O0-I/O7	RAM port data inputs/outputs
SI/O0-SI/O7	SAM port data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{DT}/\overline{OE}$	Data transfer/output enable
SC	Serial clock
$\overline{SE}$	SAM port enable
DSF1	Special function input flag
QSF	Special function output flag
V_{CC}	Power supply
V_{SS}	Ground
NL	No lead
NC	No connection

Block Diagram



Pin Functions

$\overline{\text{RAS}}$ (input pin): $\overline{\text{RAS}}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{\text{RAS}}$. The input level of these signals determines the operation cycle of the HM538253B/HM538254B.

$\overline{\text{CAS}}$ (input pin): Column address and DSF1 signals are fetched into the chip at the falling edge of $\overline{\text{CAS}}$, which determines the operation mode of the HM538253B/HM538254B.

A0–A8 (input pins): Row address (AX0–AX8) is determined by A0–A8 level at the falling edge of $\overline{\text{RAS}}$. Column address (AY0–AY8) is determined by A0–A8 level at the falling edge of $\overline{\text{CAS}}$. In transfer cycles, row address is the address on the word line which transfers data with the SAM data register, and column address is the SAM start address after transfer.

$\overline{\text{WE}}$: The $\overline{\text{WE}}$ pin has two functions at the falling edge of $\overline{\text{RAS}}$ and after. When $\overline{\text{WE}}$ is low at the falling edge of $\overline{\text{RAS}}$, the HM538253B/ HM538254B turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{\text{WE}}$ level at the falling edge of $\overline{\text{RAS}}$ is don't care in read cycle.) When $\overline{\text{WE}}$ is high at the falling edge of $\overline{\text{RAS}}$, a no mask write cycle is executed. After that, $\overline{\text{WE}}$ switches to read/write cycles. In a transfer cycle, the direction of transfer is determined by $\overline{\text{WE}}$ level at the falling edge of $\overline{\text{RAS}}$. When $\overline{\text{WE}}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{\text{WE}}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O0–I/O7 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{\text{RAS}}$ (in mask write mode). Data is written only to high I/O pins. Data on low I/O pins is masked and internal data is retained. After that, they function as input/output pins as those of a standard DRAM. In block write cycle, the data functions as column mask data at the falling edges of $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.

$\overline{\text{DT}}$/$\overline{\text{OE}}$ (input pin): The $\overline{\text{DT}}$/$\overline{\text{OE}}$ pin functions as a $\overline{\text{DT}}$ (data transfer) pin at the falling edge of $\overline{\text{RAS}}$ and as an $\overline{\text{OE}}$ (output enable) pin after that. When $\overline{\text{DT}}$ is low at the falling edge of $\overline{\text{RAS}}$, this cycle becomes a transfer cycle. When $\overline{\text{DT}}$ is high at the falling edge of $\overline{\text{RAS}}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data outputs from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is fetched into the SAM data register.

$\overline{\text{SE}}$ (input pin): $\overline{\text{SE}}$ pin activates SAM. When $\overline{\text{SE}}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not fetched into the SAM data register in serial write cycle. $\overline{\text{SE}}$ can be used as a mask for serial write because the internal pointer is incremented at the rising edge of SC.

SI/O0–SI/O7 (input/output pins): SI/Os are SAM input/output pins. I/O direction is determined by the previous transfer cycle. If it was a read transfer cycle, SI/O outputs data. If it was a masked write transfer cycle, SI/O inputs data.

DSF1 (input pin): DSF1 is a special function data input flag pin. It is set to high at the falling edge of $\overline{\text{RAS}}$ when new functions such as color register and mask register read/write, split transfer, and flash write, are used.

DSF2 (input pin): DSF2 is also a special function data input flag pin. This pin is fixed to low level in all

operations of the HM538253B/HM538254B.

QSF (output pin): QSF outputs data of address A8 in SAM. QSF is switched from low to high by accessing address 255 in SAM, and from high to low by accessing address 511 in SAM.

Table 1 Operation Cycles of the HM538253B/HM538254B

	$\overline{RAS}$					$\overline{CAS}$		Address		I/On Input	
Mnemonic Code	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	DSF1	DSF2	DSF1	DSF2	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}/\overline{WE}$
CBRS	0	—	0	1	0	—	0	Stop	—	—	—
CBRR	0	—	1	0	0	—	0	—	—	—	—
CBRN	0	—	1	1	0	—	0	—	—	—	—
MWT	1	0	0	0	0	—	0	Row	TAP	WM	—
MSWT	1	0	0	1	0	—	0	Row	TAP	WM	—
RT	1	0	1	0	0	—	0	Row	TAP	—	—
SRT	1	0	1	1	0	—	0	Row	TAP	—	—
RWM	1	1	0	0	0	0	0	Row	Column	WM	Input data
BWM	1	1	0	0	0	1	0	Row	Column	WM	Column Mask
RW (No)	1	1	1	0	0	0	0	Row	Column	—	Input Data
BW (No)	1	1	1	0	0	1	0	Row	Column	—	Column Mask
FWM	1	1	0	1	0	—	0	Row	—	WM	—
LMR and Old Mask Set	1	1	1	1	0	0	0	(Row)	—	—	Mask Data
LCR	1	1	1	1	0	1	0	(Row)	—	—	Color
Option	0	0	0	0	0	—	0	Mode	—	Data	—

Table 1 Operation Cycles of the HM538253B/HM538254B (cont)

		Register				
Mnemonic Code	**Write Mask**	**Pers W.M.**	**WM**	**Color**	**No. Of Bndry**	**Function**
CBRS	—	—	—	—	Set	CBR refresh with stop register set
CBRR	—	Reset	Reset	—	Reset	CBR refresh with register reset
CBRN	—	—	—	—	—	CBR refresh (no reset)
MWT	Yes	No Yes	Load/use Use	—	—	Masked write transfer (new/old mask)
MSWT	Yes	No Yes	Load/use Use	—	Use	Masked split write transfer (new/old mask)
RT	—	—	—	—	—	Read transfer
SRT	—	—	—	—	Use	Split read transfer
RWM	Yes	No Yes	Load/use Use	—	—	Read/write (new/old mask)
BWM	Yes	No Yes	Load/use Use		—	Block write (new/old mask)
RW (no)	No	No	—	—	—	Read/write (no mask)
BW (no)	No	No	—	Use	—	Block write (no mask)
FWM	Yes	No Yes	Load/use Use	Use	—	Masked flash write (new/old mask)
LMR and Old Mask Set	—	Set	Load	—	—	Load mask register and old mask set
LCR	—	—	—	Load	—	Load color resister set
Option	—	—	—	—	—	

Notes: 1. With CBRS, all SAM operations use stop register.
2. After LMR, RWM, BWM, FWM, MWT, and MSWT, use old mask which can be reset by CBRR
3. DSF2 is fixed low in all operation (for the addition of operation modes in future).

Operation of HM538253B/HM538254B

RAM Port Operation

RAM Read Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF1 low at the falling edge of $\overline{RAS}$, DSF1 low at the falling edge of $\overline{CAS}$: Mnemonic Code; R) Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM operation. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data outputs through the I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable fast page mode/hyper page mode.

RAM Write Cycle (Early Write, Delayed Write, Read-Modify-Write)($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF1 are low at the falling edge of $\overline{RAS}$, and DSF1 is low at the falling edge of $\overline{CAS}$): Mnemonic Code; W

No Mask Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$): When $\overline{CAS}$ is set low and $\overline{WE}$ is set low after $\overline{RAS}$ low, a write cycle is executed. If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and all I/O become in high impedance. If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high. If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables read/write at the same address in one cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and driving $\overline{OE}$ high.

Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$):If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, two modes of mask write cycle are possible.

In new mask mode, mask data is loaded from I/O pin and used. Whether or not an I/O is written depends on I/O level at the falling edge of $\overline{RAS}$. The data is written in high level I/Os, and the data is masked and retained in low level I/Os. This mask data is effective during the $\overline{RAS}$ cycle. So, in page mode cycles the mask data is retained during the page access.

If a load mask register cycle (LMR) has been performed, Mask write cycle (RAM write cycle, flash write cycle, block write cycle, masked write transfer cycle and masked sprit write transfer cycle) becomes all persistent mask mode. The mask data is not loaded from I/O pins and the mask data stored in mask registers persistently are used. This operation known as persistent write mask is reset by CBRR cycle, and become a new mask.

Fast Page Mode Cycle (HM538253B) ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF1 low at the falling edge of $\overline{RAS}$): Fast page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle. In this cycle, read, write, and block write cycles can be mixed. Note that address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 512-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 µs).

Hyper Page Mode Cycle (HM538254B) ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF1 low at the falling edge of $\overline{RAS}$): Hyper page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one forth of the random read/write cycle. In this cycle, read, write, and block write cycles can be mixed. Note that address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. column address is latched by $\overline{CAS}$ low edge triger, access time from $\overline{CAS}$ is determined by t_{CAC} (t_{AA} from column address, t_{ACP} from $\overline{CAS}$ high edge). Dout data is held during $\overline{CAS}$ high and is sustained until next Dout. Data output enable/disable is controlled by $\overline{DT}/\overline{OE}$ and when both $\overline{RAS}$ and $\overline{CAS}$ become high, Data output become High-Z. In one $\overline{RAS}$ cycle, 512-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 µs).

Color Register Set/Read Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high, $\overline{WE}$ high and DSF1 high at the falling edge of $\overline{RAS}$: Mnemonic Code; LCR) In color register set cycle, color data is set to the internal color register used in flash write cycle or block write cycle. 8 bits of internal color register are provided at each I/O. This register is composed of static circuits, so once it is set, it retains the data until reset. Since color register set cycle is the same as the usual read and write cycle, so read, early write, and delayed write cycle can be executed. In this

cycle, the HM538253B/ HM538254B refreshes the row address fetched at the falling edge of $\overline{RAS}$.

Mask Register Set/Read Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high, $\overline{WE}$ high, and DSF1 low at the falling edge of $\overline{RAS}$: Mnemonic Code; LMR) In this cycle, mask data is set to the internal mask register persistently used in mask write cycle, block write cycle, flash write cycle, masked write transfer, and masked split write transfer. 8 bits of internal mask register are provided at each I/O. This mask register is composed of static circuits. So once it is reset by CBRR cycle, it retains the data until reset or reselect. Once LMR is set, mask write cycle data is written by persistent mask data. Since mask register set cycle is just the same as the usual read and write cycle, so read, early write, and delayed write cycle can be executed.

Flash Write Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high, $\overline{WE}$ low, and DSF1 high at the falling edge of $\overline{RAS}$: Mnemonic; FW) In a flash write cycle, a row of data (512 word × 8 bit) is cleared to 0 or 1 at each I/O according to the data in the color register mentioned before. It is also necessary to mask I/O in this cycle. When $\overline{CAS}$ and $\overline{DT}/\overline{OE}$ is set high, $\overline{WE}$ is low, and DSF1 is high at the falling edge of $\overline{RAS}$, this cycle starts. Then, the row address to clear is given to row address. Mask data is the same as that of a RAM write cycle. Cycle time is the same as those of RAM read/write cycles, so all bits can be cleared in 1/512 of the usual cycle time. (See figure 1.)

Block Write Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high and DSF1 low at the falling edge of $\overline{RAS}$, DSF1 high and $\overline{WE}$ low at the falling edge of $\overline{CAS}$: Mnemonic; BW) In a block write cycle, 4 columns of data (4 column × 8 bit) are cleared to 0 or 1 at each I/O according to the data of color register. Column addresses A0 and A1 are disregarded. The mask data on I/Os and the mask data on column address can be determined independently. I/O level at the falling edge of $\overline{CAS}$ determines the address to be cleared. (See figure 2.) The block write cycle is as the same as the usual write cycle, so early and delayed write, read-modify-write, and page mode write cycle can be executed.

No Mask Mode Block Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$): The data on 8 I/Os are all cleared when $\overline{WE}$ is high at the falling edge of $\overline{RAS}$.

Mask Block Write Cycle ($\overline{WE}$ low at the falling edge of $\overline{RAS}$):When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM538253B/HM538254B starts mask block write cycle to clear the data on an optional I/O. The mask data is the same as that of a RAM write cycle. High I/O is cleared, low I/O is not cleared and the internal data is retained. In new mask mode, the mask data is available in the $\overline{RAS}$ cycle. In persistent mask mode, I/O don't care about mask mode.

- Determine first SAM address to access after transferring at column address (SAM start address).
  - — SAM start address must be determined by read transfer cycle or masked write transfer cycle (split transfer cycle isn't available) before SAM access, after power on, and determined for each transfer cycle.
- Use the stopping columns (boundaries) in the serial shift register. If the stopping columns have been set, split transfer cycles use the stopping columns, but any boundaries cannot be set as the start address.
- Load/use mask data in masked write transfer cycle and masked split write transfer cycle.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high and DSF1 low at the falling edge of $\overline{RAS}$): Mnemonic; RT

This cycle becomes read transfer cycle by driving $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high and DSF1 low at the falling edge of $\overline{RAS}$. The row address data (512 × 8 bits) determined by this cycle is transferred to SAM data register synchronously at the rising edge of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from SAM start address determined by column address. In read transfer cycle, $\overline{DT}/\overline{OE}$ must rise to transfer data from RAM to SAM.

This cycle can access SAM even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge and t_{SDH} (min) specified between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge must be satisfied. (See figure 3.)

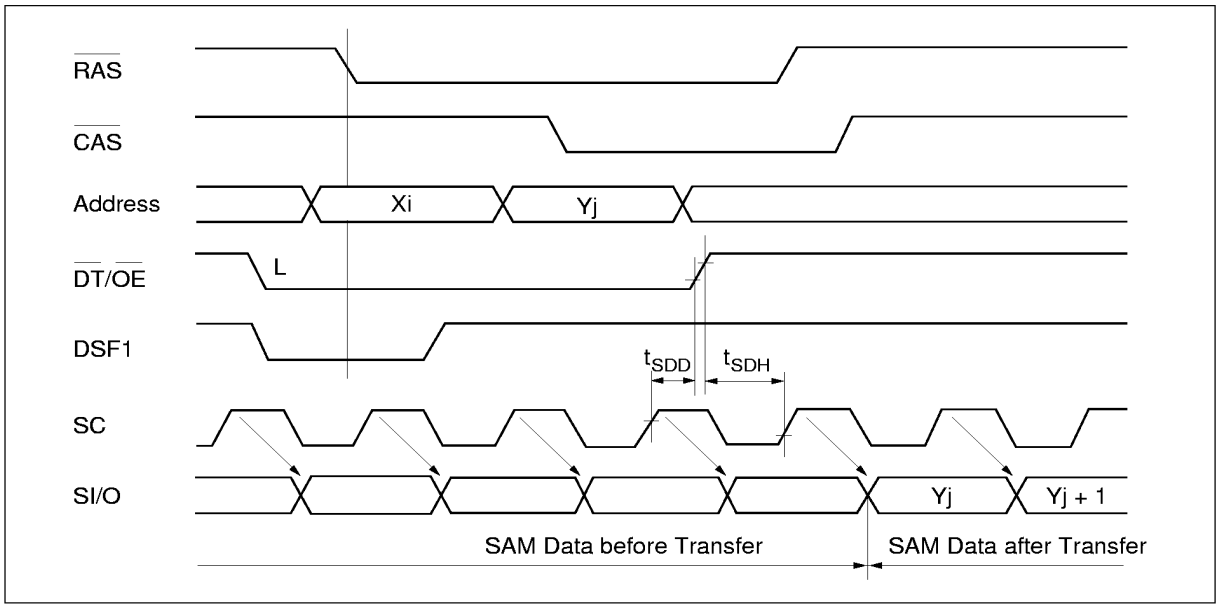


Figure 3 Real Time Read Transfer

When read transfer cycle is executed, SI/O becomes output state by first SAM access. Input must be set high impedance before t_{SZS} (min) of the first SAM access to avoid data contention.

Masked Write Transfer cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and DSF1 low at the falling edge of $\overline{RAS}$): Masked write transfer cycle can transfer only selected I/O data in a row of data input by serial write cycle to

RAM. Whether I/O data is transferred or not depends on the corresponding I/O level (mask data) at the falling edge of $\overline{RAS}$. This mask transfer operation is the same as a mask write operation in RAM cycles, so the persistent mode can be supported.

The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address for serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC must not be risen.

Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addresses of RAM by write transfer cycle. However, the address to write data must be the same as that of the read transfer cycle or the split read transfer cycle (row address AX8). Figure 4 shows the example of row bit data transfer. In case AX8 is 0, data cannot be transferred RAM address within the range of 100000000 to 111111111. Same as the case of AX8 = 1.

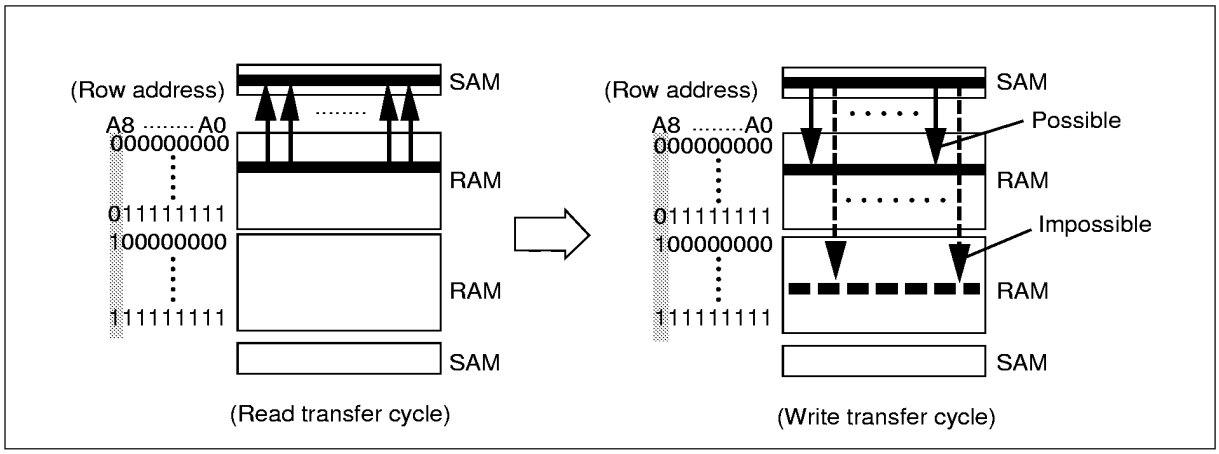


Figure 4 Example of Row Bit Data Transfer

Split Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high and DSF1 high at the falling edge of $\overline{RAS}$): To execute a continuous serial read by real-time read transfer, the HM538253B/HM538254B must satisfy SC and $\overline{DT}/\overline{OE}$ timings and requires an external circuit to detect SAM last address. Split read transfer cycle makes it possible to execute a continuous serial read without the above timing limitation.

The HM538253B/HM538254B supports two types of split register operation. One is the normal split register operation to split the data register into two halves. The other is the boundary split register operation using stopping columns described later.

Figure 5 shows the block diagram for the normal split register operation. SAMdata register (DR) consists of 2 split buffers, whose organizations are 256-word × 8-bit each. Suppose that data is read from upper data register DR1. (The row address AX8 is 0 and SAM address A8 is 1.) When split read transfer is executed setting row address AX8 to 0 and SAM start addresses A0 to A7, 256-word × 8-bit data is transferred from RAM to the lower data register DR0 (SAM address A8 is 0) automatically. After data is read from data register DR1, data read begins from SAM start addresses of data register DR0. If the next split read transfer isn't executed while data is read from data register DR0, data read begins from SAM start address 0 of DR1

after data is read from data register DR0. If split read transfer is executed setting row address AX8 to 1 and SAM start addresses A0 to A7 while data is read from data register DR1, 256-word × 8-bit data is transferred to data register DR2. After data is read from data register DR1, data read begins from the SAM start addresses of data register DR2. If the next split read transfer isn't executed while data is read from data register DR2, data read begins from SAM start address 0 of data register DR1 after data is read from data register DR2. In split read data transfer, the SAM start address A8 is automatically set in the data register, which isn't used.

The data on SAM address A8, which will be accessed next, outputs to QSF. QSF is switched from low to high by accessing SAM last address 255 and from high to low by accessing address 511.

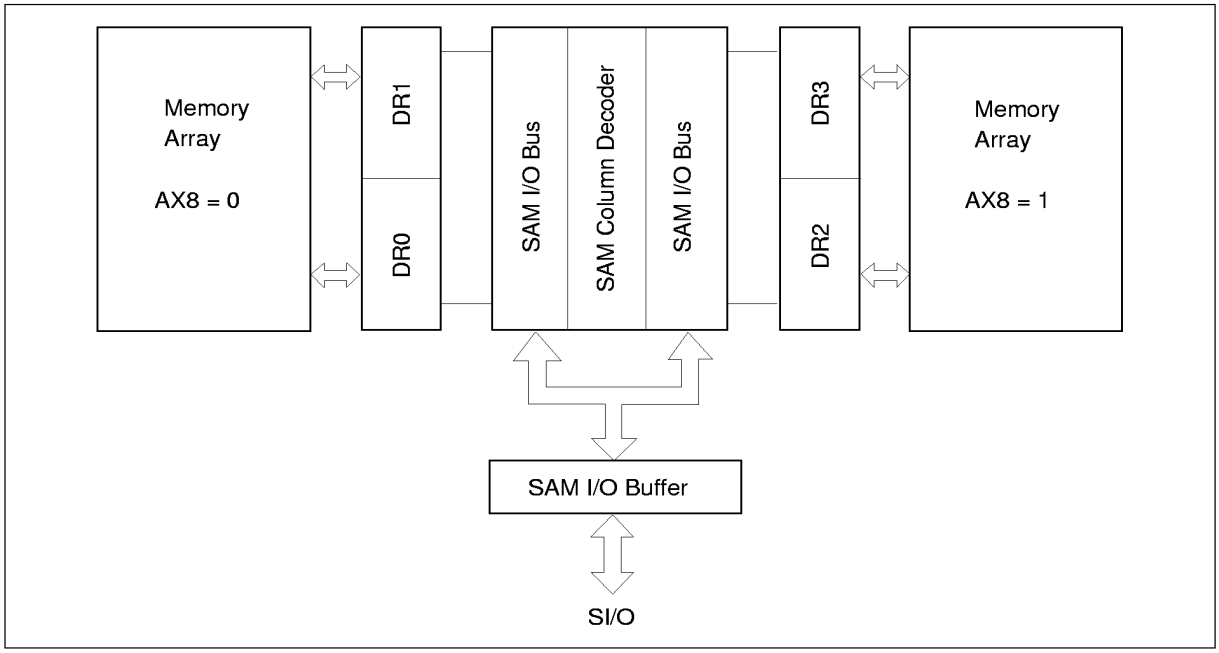


Figure 5 Split Transfer Block Diagram

Split read transfer cycle is set when $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ is low, $\overline{WE}$ is high and DSF1 is high at the falling edge of $\overline{RAS}$. The cycle can be executed asyncronously with SC. However, HM538253B/ HM538254B must be satisfied t_{STS} (min) timing specified between SC rising (boundary address) and $\overline{RAS}$ falling. In split transfer cycle, the HM538253B/HM538254B must satisfy t_{RST} (min), t_{CST} (min) and t_{AST}(min) timings specified between $\overline{RAS}$ or $\overline{CAS}$ falling and column address. (See figure 6.)

In split read transfer, SI/O isn't switched to output state. Therefore, read transfer must be executed to switch SI/O to output state when the previous transfer cycle is masked write transfer cycle or masked split write transfer cycle.

Masked Split Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low and DSF1 high at the falling edge of $\overline{RAS}$): A continuous serial write cannot be executed because accessing SAM is inhibited during $\overline{RAS}$ low in write transfer. Masked split write transfer cycle makes it possible. In this cycle, t_{STS} (min), t_{RST} (min), t_{CST} (min) and t_{AST} (min) timings must be satisfied like split read transfer cycle. And it is impossible to switch SI/O to input state in this cycle. If SI/O is in output state, masked write transfer cycle should be executed to

switch SI/O into input state. Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addresses of RAM by masked split write transfer cycle. However masked write transfer cycle must be executed before masked split write transfer cycle. And in this masked split write transfer cycle, the MSB of row address (AX8) to write data must be the same as that of the read transfer cycle or the split read transfer cycle. In this cycle, the boundary split register operation using stopping columns is possible as with split read transfer cycle.

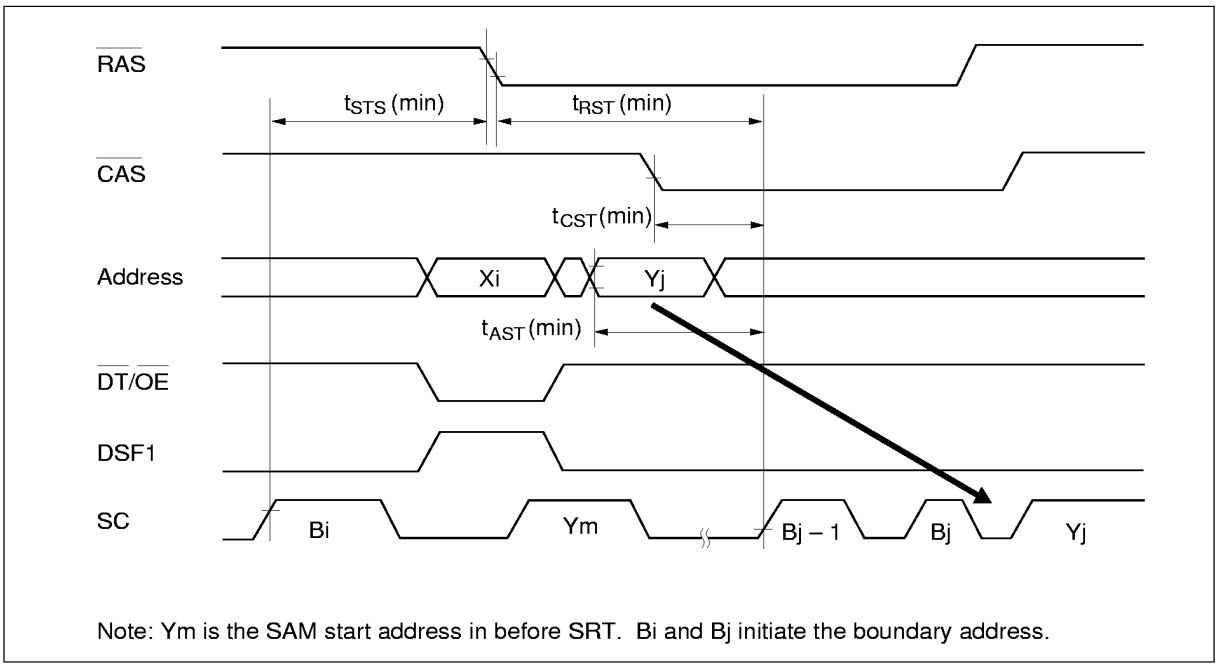


Figure 6 Split Transfer Limitation

Table 2 Stopping Column Boundary Table

		Stop Address					
Boundary Code	**Column Size**	**A2**	**A3**	**A4**	**A5**	**A6**	**A7**
B2	4	0	×	×	×	×	×
B3	8	1	0	×	×	×	×
B4	16	1	1	0	×	×	×
B5	32	1	1	1	0	×	×
B6	64	1	1	1	1	0	×
B7	128	1	1	1	1	1	0
B8	256	1	1	1	1	1	1

Notes: 1. A0, A1, and A8: H or L
2. ×: H or L

Stopping Column in Split Transfer Cycle: The HM538253B/HM538254B has the boundary split register operation using stopping columns. If a CBRS cycle has been performed, split transfer cycle performs the boundary operation. Figure 7 shows an example of boundary split register. (Boundary code is B7.)

First a read data transfer cycle is executed, and SAM start addresses A0 to A8 are set. The RAM data is transferred to the SAM, and SAM serial read starts from the start address (Y1) on the lower SAM. After that, a split read transfer cycle is executed, and the next start address (Y2) is set. The RAM data is transferred to the upper SAM. When the serial read arrive at the first boundary after the split read transfer cycle, the next read jumps to the start address (Y2) on the upper SAM (jump 1) and continues. Then the second split read transfer cycle is executed, and another start address (Y3) is set. The RAM data is transferred to the lower SAM. When the serial read arrive at the other boundary again, the next read jumps to the start address (Y3) on the lower SAM. In stopping column, split transfer is needed for jump operation between lower SAM and upper SAM.

Stopping Column Set Cycle (CBRS): Start a stopping column set cycle by driving $\overline{CAS}$ low, $\overline{WE}$ low, and DSF1 high at the falling edge of $\overline{RAS}$. Stopping column data (boundaries) are latched from address inputs on the falling edge of $\overline{RAS}$. To determine the boundary, A2 to A7 can be used, and A0, A1, and A8 don't care. In the HM538253B/HM538254B, 7 types of boundary (B2 to B8) can be set including the default case. (See stopping column boundary table.) If A2 to A6 are set high and A7 is set low, the boundaries (B7) are selected. Figure 6 shows the example. Once a CBRS is executed, next sprit transfer cycle data become stopping columm data. Stopping columm is reset by CBBR.

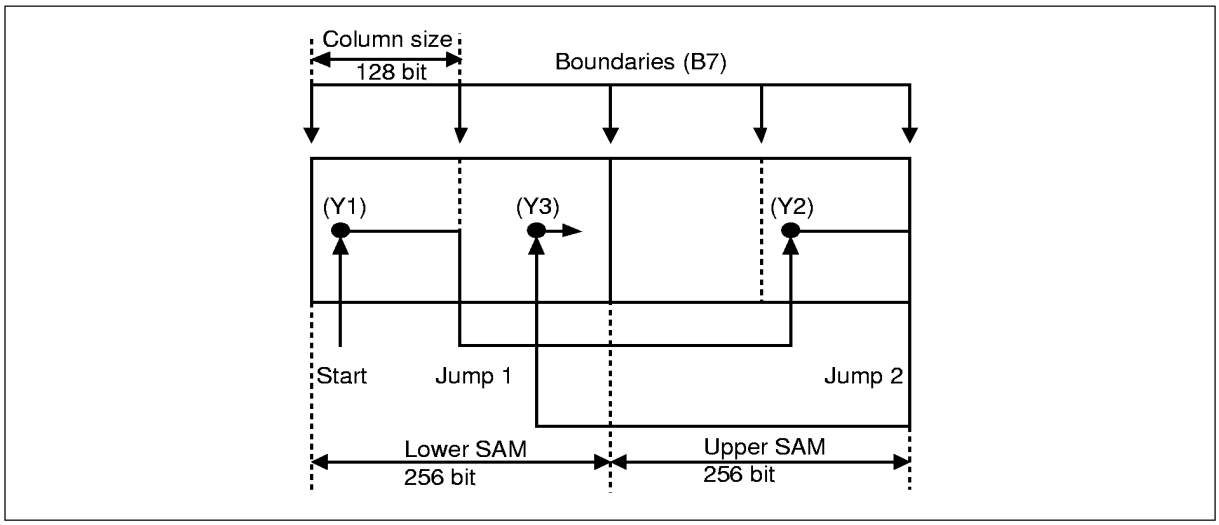


Figure 7 Example of Boundary Split Register

Register Reset Cycle (CBRR): Start a register reset cycle (CBRR) by driving $\overline{CAS}$ low, $\overline{WE}$ high, and DSF1 low at the falling edge of $\overline{RAS}$. A CBRR can reset the persistent mask operation and stopping column operation, so the HM538253B/HM538254B becomes the new mask operation and boundary code B8. When a CBRR is executed for stopping column operation reset and split transfer operation, it needs to satisfy t_{STS} (min) and t_{RST} (min) between $\overline{RAS}$ falling and SC rising.

No Reset CBR cycle (CBRN): This cycle becomes no reset CBR cycle (CBRN) by driving $\overline{CAS}$ low, $\overline{WE}$

high and DSF1 high at the falling edge of $\overline{RAS}$. The CBRN can only execute the refresh operation.

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is a read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When $\overline{SE}$ is set high, SI/O becomes high impedance, and the internal pointer is incremented by the SC rising. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

Serial Write Cycle

If the previous data transfer cycle is a masked write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is fetched into the data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't fetched into the data register. The internal pointer is incremented by the SC rising, so $\overline{SE}$ high can be used as mask data for SAM. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh cycles to retain data. Refresh is executed by accessing all 512 row addresses within 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh cycle, (2) $\overline{CAS}$-before-$\overline{RAS}$ (CBRN, CBRS, and CBRR) refresh cycle, and (3) Hidden refresh cycle. The cycles which activate $\overline{RAS}$, such as read/write cycles or transfer cycles, can also refresh the row address. Therefore, no refresh cycle is required when all row addresses are accessed within 8 ms.

RAS-Only Refresh Cycle: $\overline{RAS}$-only refresh cycle is executed by activating only the $\overline{RAS}$ cycle with $\overline{CAS}$ fixed high after inputting the row address (refresh address) from external circuits. To distinguish this cycle from a data transfer cycle, $\overline{DT}/\overline{OE}$ must be high at the falling edge of $\overline{RAS}$.

CBR Refresh Cycle: CBR refresh cycle (CBRN, CBRS and CBRR) are set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, the refresh address need not be input through external circuits because it is input through an internal refresh counter. In this cycle, output is high impedance and power dissipation is low because $\overline{CAS}$ circuits are not operating.

Hidden Refresh Cycle: Hidden refresh cycle executes CBR refresh with the data output by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift resister and selector), organized as fully static circuitry, require no refresh.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	−0.5*2	—	0.8	V	1

Notes: 1. All voltage referred to V_{SS}
2 −3.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM538253B/HM538254B								
		-7		-8		-10				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Operating current	I_{CC1}	—	110	—	100	—	90	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC7}	—	165	—	150	—	140	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Block write current	I_{CC1BW}	—	115	—	105	—	90	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC7BW}	—	170	—	155	—	140	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Standby current	I_{CC2}	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC8}	—	65	—	60	—	55	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
$\overline{RAS}$-only refresh current	I_{CC3}	—	110	—	100	—	90	mA	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH} t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC9}	—	165	—	150	—	135	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Fast page mode current (HM538253B) *3	I_{CC4}	—	110	—	105	—	100	mA	$\overline{CAS}$ cycling $\overline{RAS}$ = V_{IL} t_{PC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC10}	—	160	—	155	—	150	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Fast page mode block write current *3	I_{CC4BW}	—	130	—	125	—	120	mA	$\overline{CAS}$ cycling $\overline{RAS}$ = V_{IL} t_{PC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC10BW}	—	185	—	175	—	165	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (cont)

		HM538253B/HM538254B								
		-7		-8		-10				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Hyper page mode current (HM538254B) *3	I_{CC4}	—	130	—	120	—	110	mA	$\overline{CAS}$ cycling $\overline{RAS}$ = V_{IL} t_{PC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC10}	—	185	—	170	—	160	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Hyper page mode block write current *3	I_{CC4BW}	—	155	—	140	—	130	mA mA	$\overline{CAS}$ cycling $\overline{RAS}$ = V_{IL} t_{PC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC10BW}	—	210	—	190	—	175	175		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC5}	—	85	—	75	—	65	mA	$\overline{RAS}$ cycling t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC11}	—	140	—	130	—	120	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Data transfer current	I_{CC6}	—	130	—	115	—	100	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC12}	—	180	—	165	—	145	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA		
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA		
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	V	I_{OH} = –1 mA	
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	V	I_{OL} = 2.1 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once while $\overline{RAS}$ is low and $\overline{CAS}$ is high.
3. Address can be changed once in 1 page cycle (t_{PC}).

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%, f = 1 MHz, Bias: Clock, I/O = V_{CC}, Address = V_{SS})

Parameter	Symbol	Typ	Max	Unit	Note
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	5	pF	1
Output capacitance (I/O, SI/O, QSF)	$C_{I/O}$	—	7	pF	1

Note: 1. This parameter is sampled and not 100% tested.

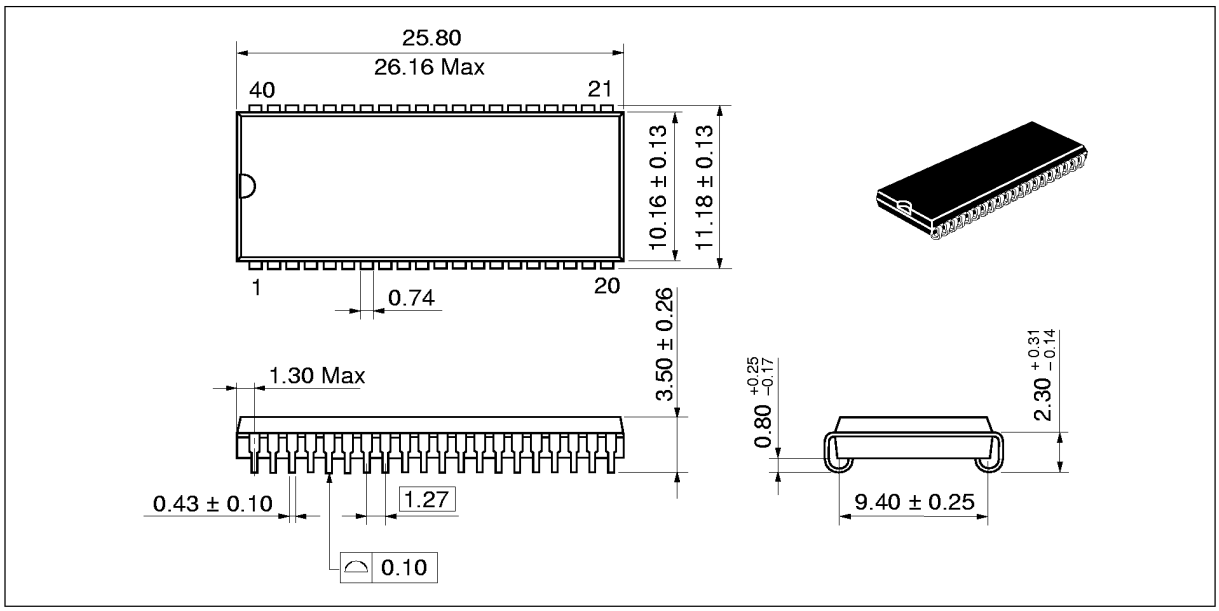
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)[*1, *16]

Test Conditions

- Input rise and fall time: 5 ns
- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: RAM 1 TTL + C_L (50 pF)
  SAM, QSF 1 TTL + C_L (30 pF) (Including scope and jig)

Package Dimensions

HM538253BJ/HM538254BJ Series (CP-40D) Unit: mm



HM638253BTT/HM538254BTT Series (TTP-44/40DA) Unit: mm