

32768-word × 8-bit High Speed CMOS Static RAM

Features

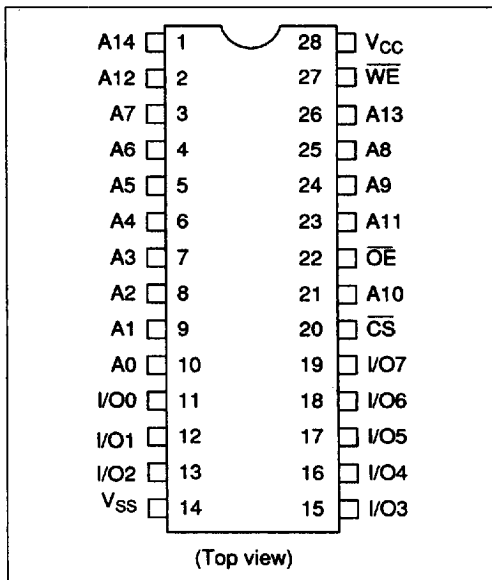
- High speed: Fast access time 85/100/120/150 ns (max)
- Low power standby and low power operation
 - Standby: 200 μ W (typ)/ 10 μ W (typ) (L-/L-SL-version)
 - Operation: 40 mW (typ) ($f = 1$ MHz)
- Single 5 V supply
- Completely static RAM: No clock or timing strobe required
- Equal access and cycle time
- Common data input and output, three-state output
- Directly TTL compatible—all inputs and outputs
- Battery back up operation capability (L-/L-SL-version)

Ordering Information

Type No.	Access time	Package
HM62256P-8	85 ns	600-mil 28-pin plastic DIP
HM62256P-10	100 ns	(DP-28)
HM62256P-12	120 ns	
HM62256P-15	150 ns	
HM62256LP-8	85 ns	
HM62256LP-10	100 ns	
HM62256LP-12	120 ns	
HM62256LP-15	150 ns	
HM62256LP-10SL	100 ns	
HM62256LP-12SL	120 ns	
HM62256LP-15SL	150 ns	

Type No.	Access time	Package
HM62256FP-8T	85 ns	28-pin plastic SOP
HM62256FP-10T	100 ns	(FP-28DA)
HM62256FP-12T	120 ns	
HM62256FP-15T	150 ns	
HM62256LFP-8T	85 ns	
HM62256LFP-10T	100 ns	
HM62256LFP-12T	120 ns	
HM62256LFP-15T	150 ns	
HM62256LFP-10SLT	100 ns	
HM62256LFP-12SLT	120 ns	
HM62256LFP-15SLT	150 ns	

Pin Arrangement



Note: This device is not available for new application.

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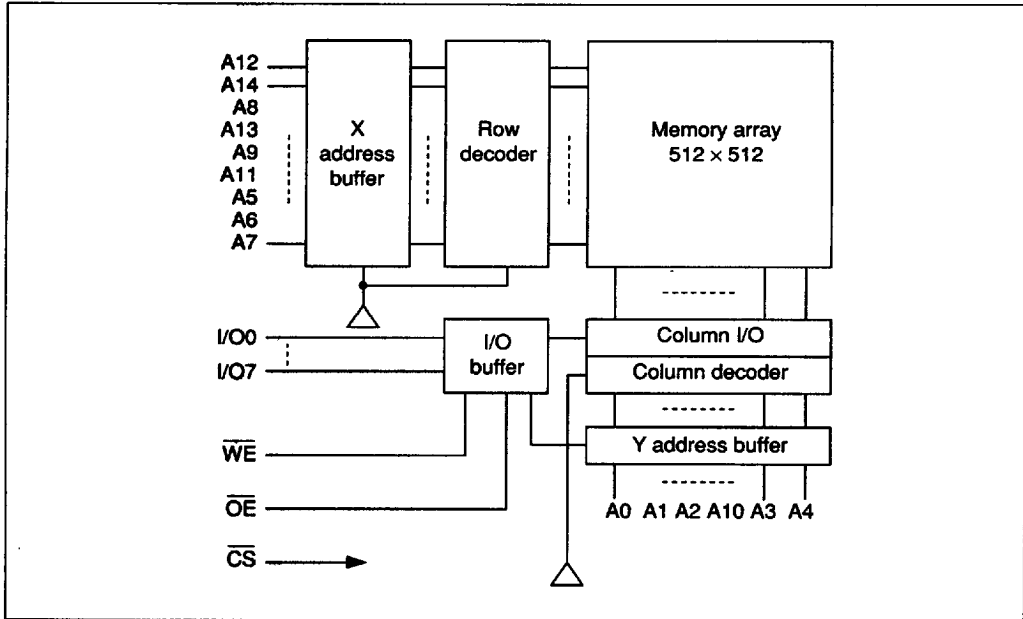
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HM62256 Series

Block Diagram



Truth Table

\overline{CS}	\overline{OE}	\overline{WE}	Mode	V_{CC} current	I/O pin	Reference cycle
H	x	x	Not selected	I_{SB}, I_{SB1}	High Z	—
L	L	H	Read	I_{CC}	Dout	Read cycle No. 1–3
L	H	L	Write	I_{CC}	Din	Write cycle No. 1
L	L	L	Write	I_{CC}	Din	Write cycle No. 2

Note: x means H or L

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Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V _{SS}	V _T	-0.5 to +7.0	V
Power dissipation	P _T	1.0	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +125	°C
Temperature under bias	T _{bias}	-10 to +85	°C

Note: -3.0 V min for pulse width ≤ 50 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
	V _{SS}	0	0	0	V
Input voltage	V _{IH}	2.2	—	6.0	V
	V _{IL}	-0.5	—	0.8	V

Note: -3.0 V min for pulse width ≤ 50 ns

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ *1	Max	Unit	Test condition	
Input leakage current	I _{LI}	—	—	2	μA	V _{IN} = V _{SS} to V _{CC}	
Output leakage current	I _{LO}	—	—	2	μA	CS = V _{IH} or OE = V _{IH} or WE = V _{IL} V _{I/O} = V _{SS} to V _{CC}	
Operating power supply current	I _{CC}	—	8	15	mA	CS = V _{IL} , I _{I/O} = 0 mA	
Average operating power supply current	HM62256-8	I _{CC1}	—	50	70	mA	Min. cycle, duty = 100%, CS = V _{IL} , I _{I/O} = 0 mA
	HM62256-10	—	—	40	70	mA	
	HM62256-12	—	—	35	70	mA	
	HM62256-15	—	—	33	70	mA	
		I _{CC2}	—	8	15	mA	CS = V _{IL} , V _{IH} = V _{CC} , V _{IL} = 0V, I _{I/O} = 0 mA f = 1 MHz

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DC Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 0\text{ to }+70^\circ\text{C}$) (cont)

Parameter	Symbol	Min	Typ ^{*1}	Max	Unit	Test condition
Standby power supply current	I_{SB}	—	0.5	3	mA	$\overline{CS} = V_{IH}$
	I_{SB1}	—	0.04	2	mA	$\overline{CS} \geq V_{CC} - 0.2\text{V}$, $0\text{V} \leq V_{IN}$
	—	—	2 ^{*2}	100 ^{*2}	μA	
	—	—	2 ^{*3}	50 ^{*3}		
Output voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 2.1\text{ mA}$
	V_{OH}	2.4	—	—	V	$I_{OH} = -1.0\text{ mA}$

- Notes: 1. Typical values are at $V_{CC} = 5.0\text{ V}$, $T_a = 25^\circ\text{C}$ and specified loading.
2. These characteristics are guaranteed only for L-version.
3. These characteristics are guaranteed only for L-SL version.

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Typ	Max	Unit	Test Condition
Input capacitance	C_{IN}	—	6	pF	$V_{IN} = 0\text{ V}$
Input/output capacitance	$C_{I/O}$	—	8	pF	$V_{I/O} = 0\text{ V}$

Note: These parameters are sampled and not 100% tested.

AC Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0\text{ to }+70^\circ\text{C}$ unless otherwise noted)

AC Test Conditions:

- Input pulse levels: 0.8 V to 2.4 V
- Input and output timing reference levels: 1.5 V
- Input rise and fall times: 5 ns
- Output load: 1TTL gate and $C_L = 100\text{ pF}$ (including scope and jig)

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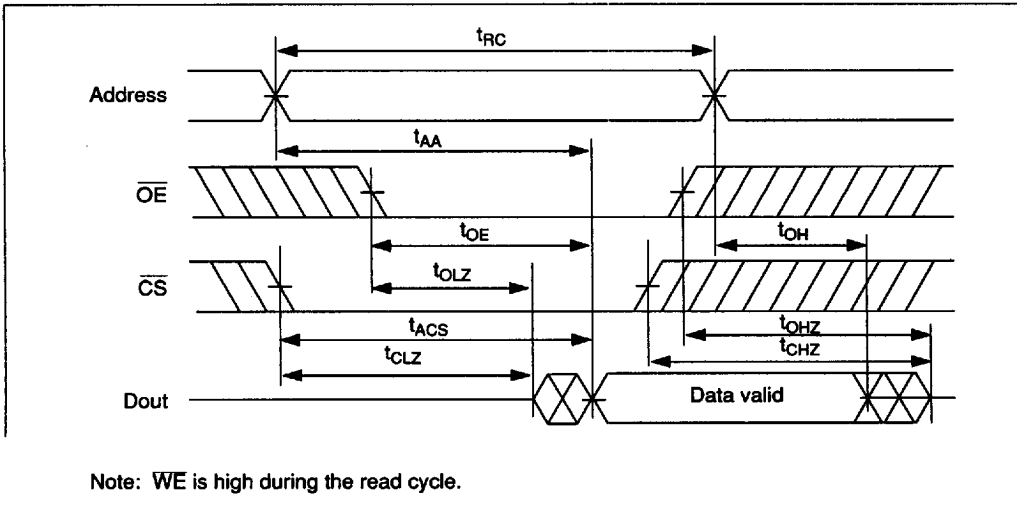
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Read Cycle

Parameter	Symbol	HM62256-8		HM62256-10		HM62256-12		HM62256-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	85	—	100	—	120	—	150	—	ns
Address access time	t_{AA}	—	85	—	100	—	120	—	150	ns
Chip select access time	t_{ACS}	—	85	—	100	—	120	—	150	ns
Output enable to output valid	t_{OE}	—	45	—	50	—	60	—	70	ns
Output hold from address change	t_{OH}	5	—	10	—	10	—	10	—	ns
Chip selection to output in low Z	t_{CLZ}	10	—	10	—	10	—	10	—	ns
Output enable to output in low Z	t_{OLZ}	5	—	5	—	5	—	5	—	ns
Chip deselection to output in high Z	t_{CHZ}	0	30	0	35	0	40	0	50	ns
Output disable to output in high Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns

Read Timing Waveform (1)



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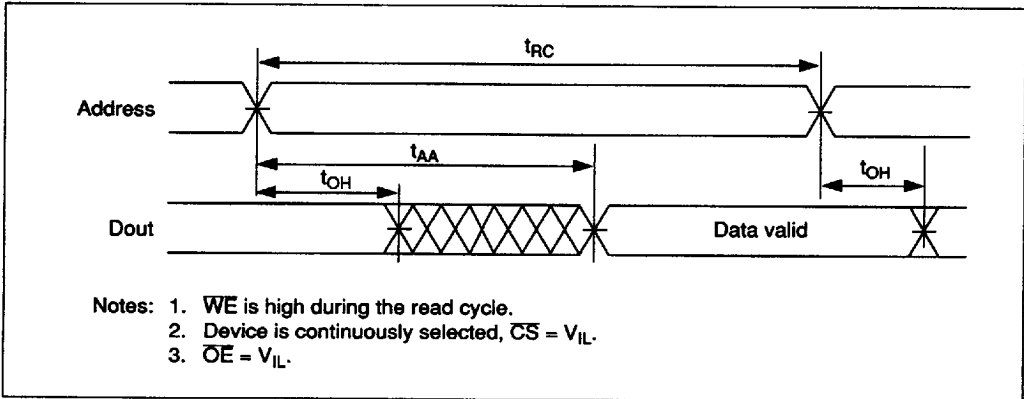
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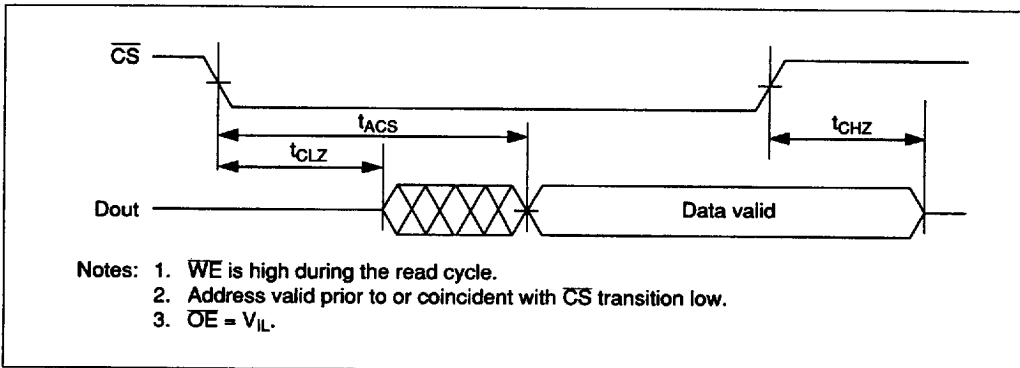
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HM62256 Series

Read Timing Waveform (2)



Read Timing Waveform (3)



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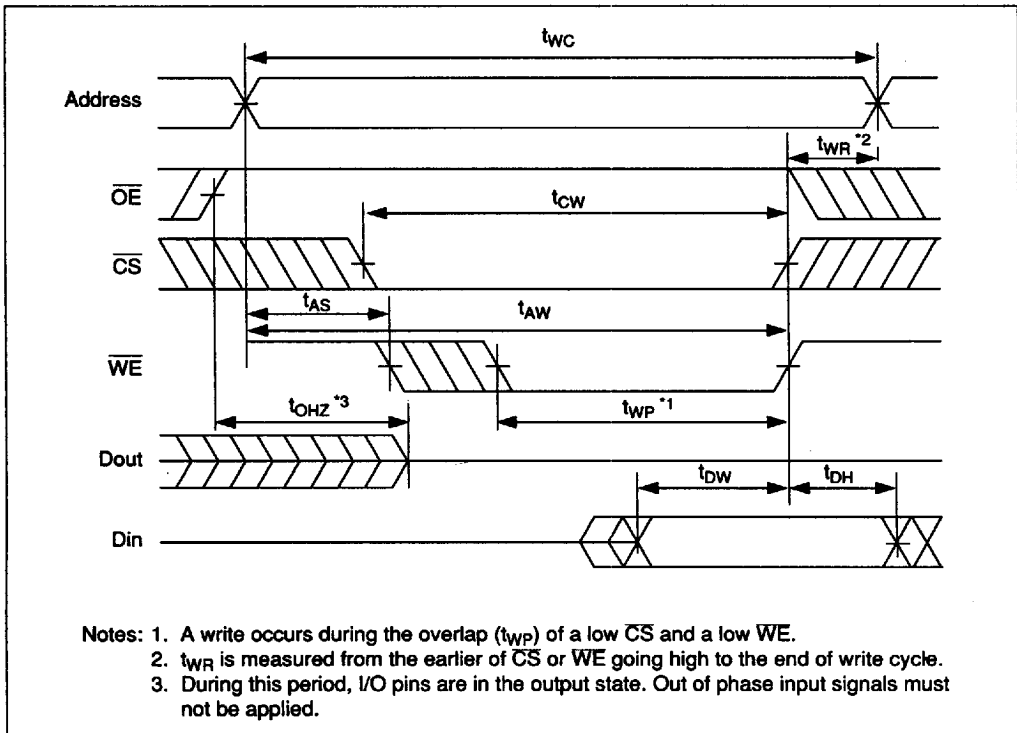
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Write Cycle

Parameter	Symbol	HM62256-8		HM62256-10		HM62256-12		HM62256-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write cycle time	t_{WC}	85	—	100	—	120	—	150	—	ns
Chip selection to end of write	t_{CW}	75	—	80	—	85	—	100	—	ns
Address valid to end of write	t_{AW}	75	—	80	—	85	—	100	—	ns
Address set up time	t_{AS}	0	—	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	60	—	60	—	70	—	90	—	ns
Write recovery time	t_{WR}	10	—	0	—	0	—	0	—	ns
Write to output in high Z	t_{WHZ}	0	30	0	35	0	40	0	50	ns
Data to write time overlap	t_{DW}	40	—	40	—	50	—	60	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns
Output disable to output in high Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns
Output active from end of write	t_{OW}	5	—	5	—	5	—	5	—	ns

Write Timing Waveform (1) (\overline{OE} Clock)



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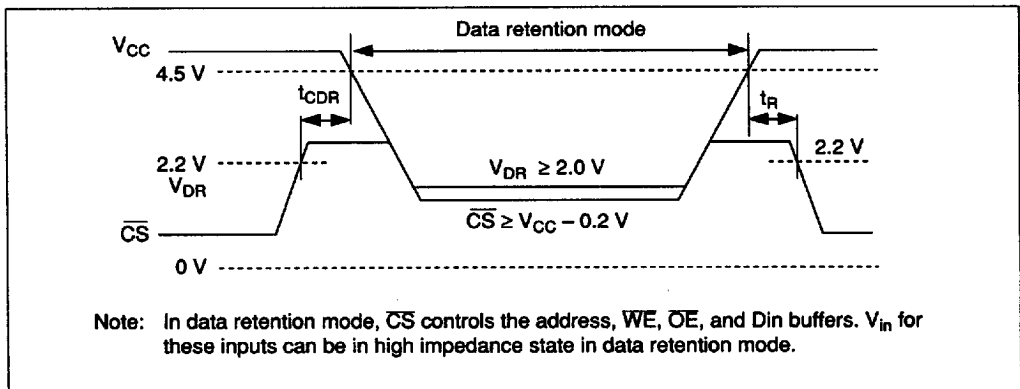
Low V_{CC} Data Retention Characteristics ($T_a = 0$ to $+70^\circ\text{C}$)

These characteristics are guaranteed only for L- and L-SL version.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{CC} for data retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}$	2.0	—	—	V
Data retention current	I_{CCDR}	$V_{CC} = 3.0 \text{ V}, \overline{CS} \geq 2.8 \text{ V}$ $0 \text{ V} \leq V_{IN}$	—	—	50^{*2} 10^{*3}	μA
Chip deselect to data retention time	t_{CDR}	See retention waveform	0	—	—	ns
Operation recovery time	t_R	See retention waveform	t_{RC}^{*1}	—	—	ns

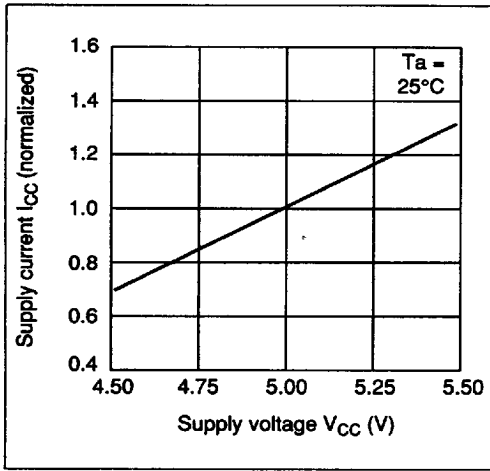
- Notes: 1. t_{RC} = read cycle time
 2. These characteristics are guaranteed only for L-version, $V_{IL} = -0.3 \text{ V}$ min, $20 \mu\text{A}$ max. at $T_a = 0$ to 40°C .
 3. These characteristics are guaranteed only for L-SL version, $V_{IL} = -0.3 \text{ V}$ min, $3 \mu\text{A}$ max. at $T_a = 0$ to 40°C .

Low V_{CC} Data Retention Waveform

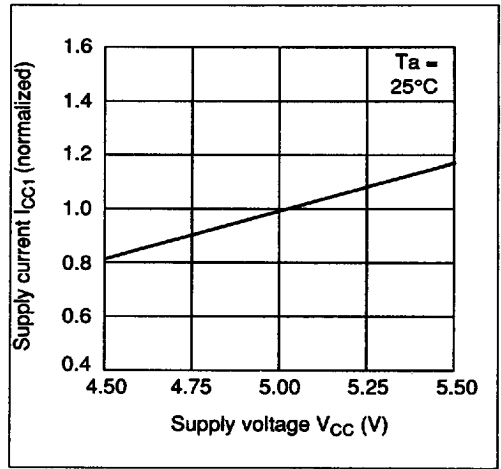


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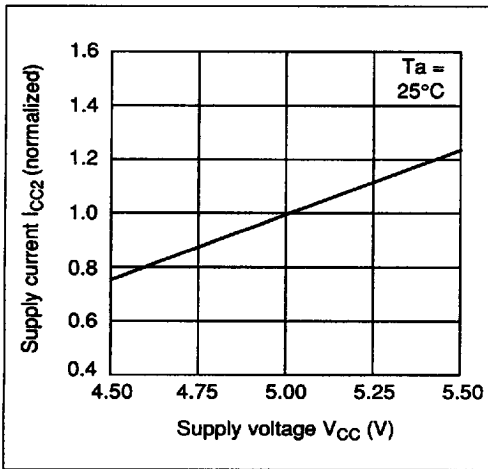
Characteristic Curves



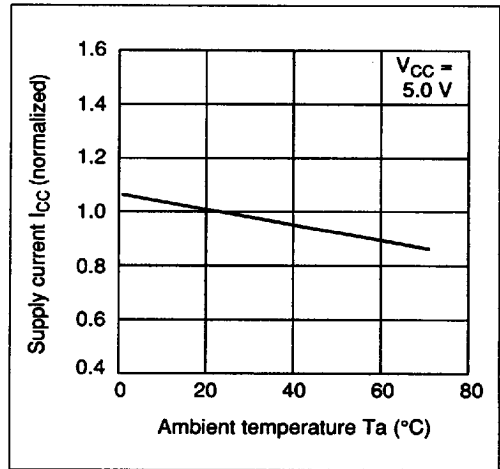
Supply Current vs. Supply Voltage (1)



Supply Current vs. Supply Voltage (2)



Supply Current vs. Supply Voltage (3)



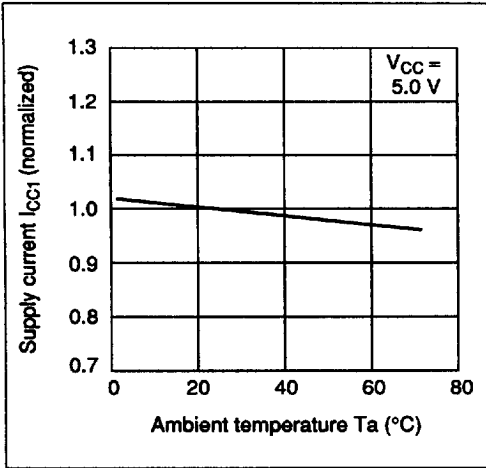
Supply Current vs. Ambient Temperature (1)

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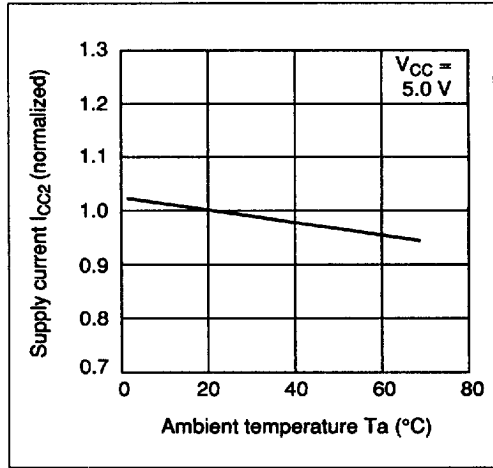
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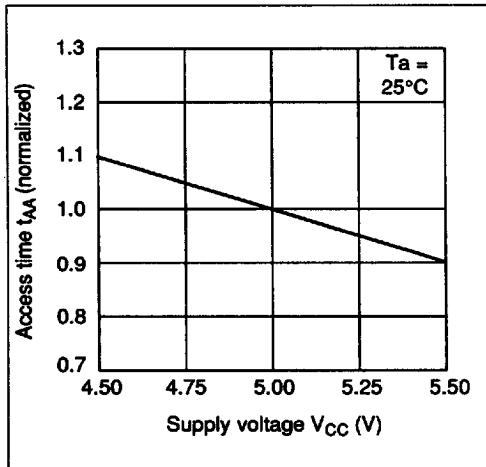
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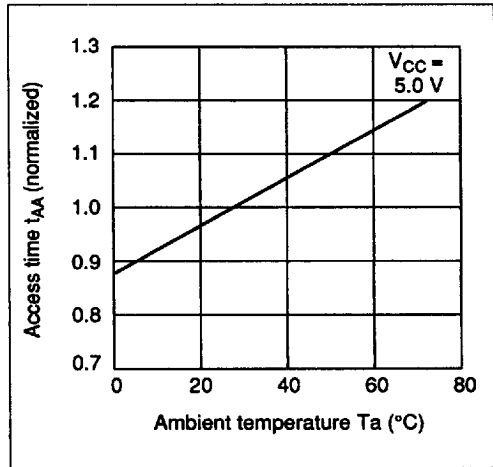
Supply Current vs. Ambient Temperature (2)



Supply Current vs. Ambient Temperature (3)



Access Time vs. Supply Voltage



Access Time vs. Ambient Temperature

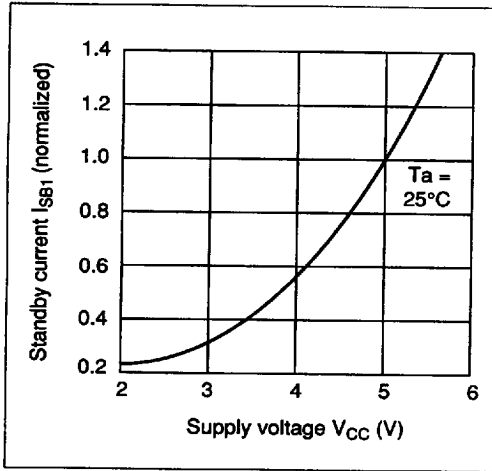
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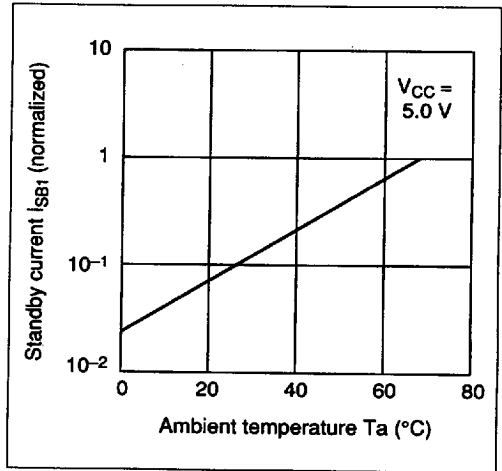
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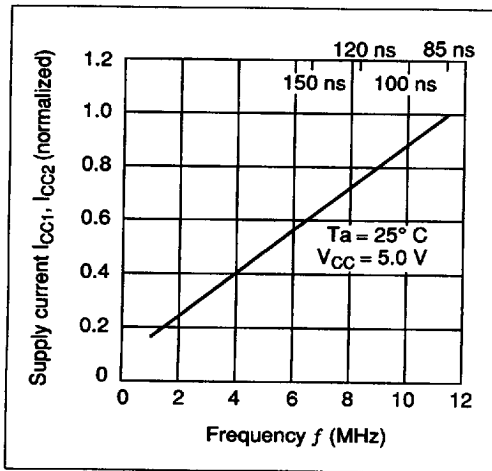
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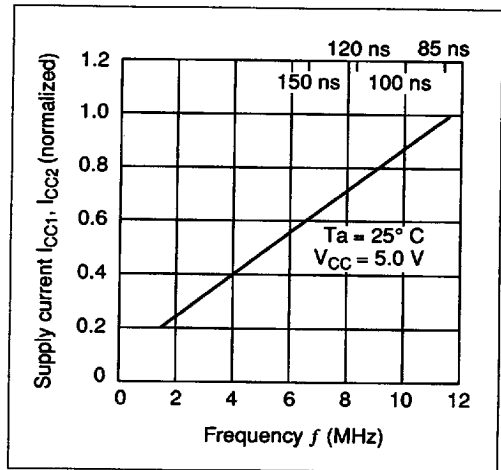
Standby Current vs. Supply Voltage



Standby Current vs. Ambient Temperature



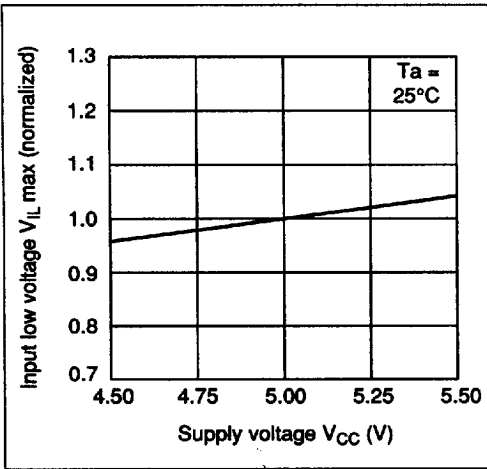
Supply Current vs. Frequency (Read)



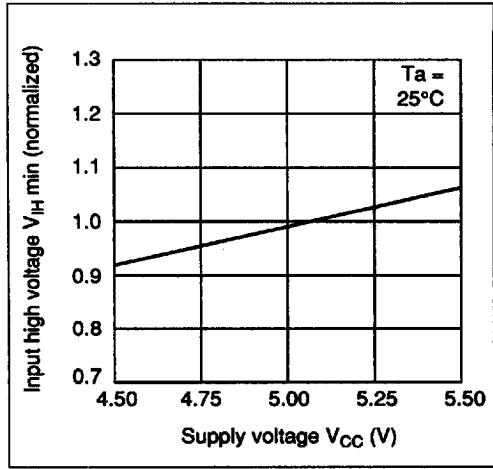
Supply Current vs. Frequency (Write)

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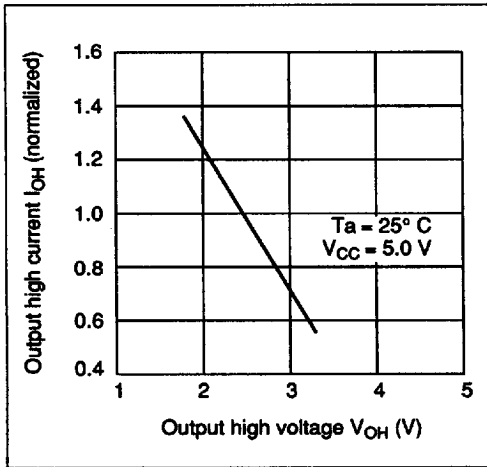
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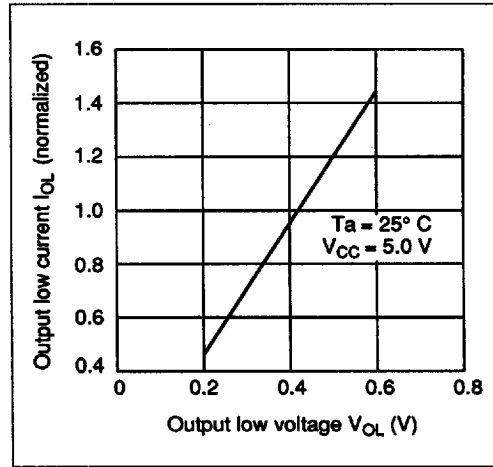
Input Low Voltage vs. Supply Voltage



Input High Voltage vs. Supply Voltage



Output Current vs. Output Voltage (High)



Output Current vs. Output Voltage (Low)

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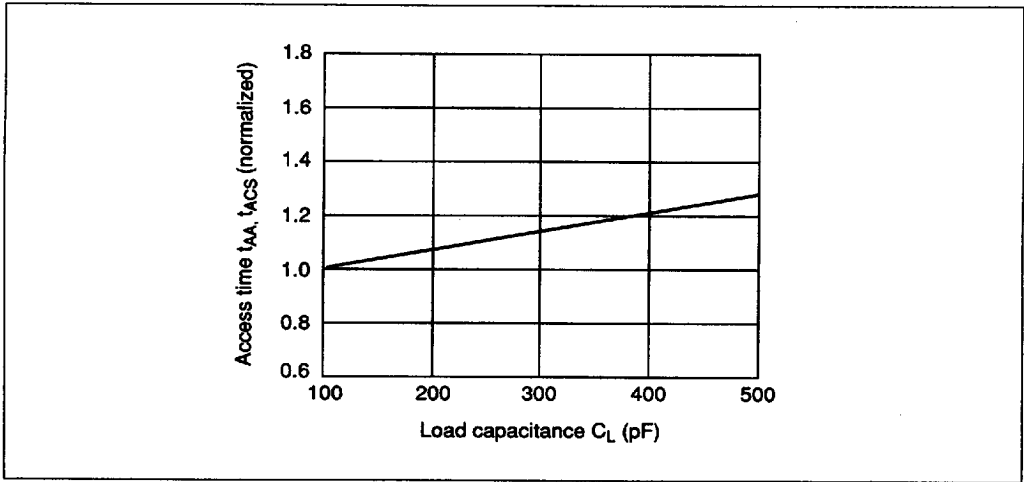
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Access Time vs. Load Capacitance

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