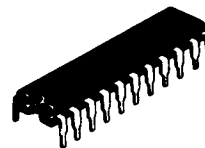


65536-word x 1-bit High Speed Hi-BiCMOS Static RAM

■ FEATURES

- Super Fast Access Time: 25ns/30ns (max.)
- Low Power Dissipation (DC):
Operating 180mW (typ)
- High Driving Capability: I_{OL} 16mA
- +5V Single Supply
- Completely Static Memory
No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output
- Skinny 22-pin Plastic Dip (300 mil) and 22-pin Chip Carrier

HM6787P Series

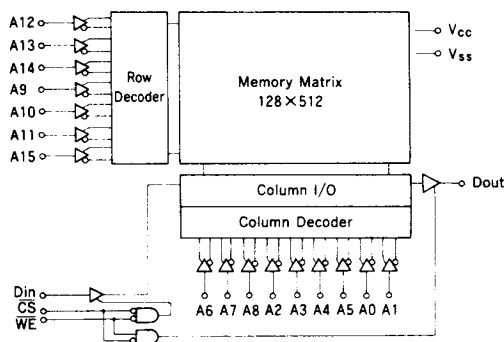


(DP-22NB)

■ ORDERING INFORMATION

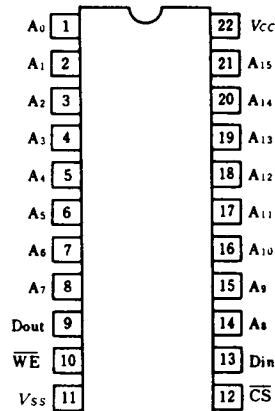
Type No.	Access Time	Package
HM6787P-25	25ns	300 mil 22 pin
HM6787P-30	30ns	Plastic DIP

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT

● HM6787P Series



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C



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■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin
H	X	Not Selected	I_{SB}, I_{SB1}	High Z
L	H	Read	I_{CC}	Dout
L	L	Write	I_{CC}	High Z

■ RECOMMENDED DC OPERATING CONDITIONS ($0^{\circ}C \leq T_a \leq 70^{\circ}C$)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	-0.5^{*1}	—	0.8	V

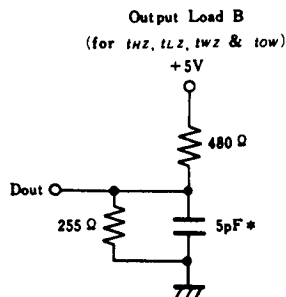
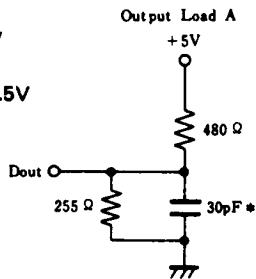
Note) *1. $-3.0V$ for pulse width $\leq 20ns$.

■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0^{\circ}C$ to $+70^{\circ}C$)

Item	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	$ I_{LI} $	$V_{CC} = 5.5V, V_{IN} = V_{SS}$ to V_{CC}	—	—	2	μA
Output Leakage Current	$ I_{LO} $	$\overline{CS} = V_{IH}, V_{OUT} = V_{SS}$ to V_{CC}	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS} = V_{IL}, I_{OUT} = 0mA$	—	—	100	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$	—	—	40	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$	—	—	20	mA
Output Low Voltage	V_{OL}	$I_{OL} = 16mA$	—	—	0.5	V
Output High Voltage	V_{OH}	$I_{OH} = -4mA$	2.4	—	—	V

■ AC TEST CONDITIONS

Input pulse levels: V_{SS} to 3.0V
Input rise and fall times: 4ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure



* Including scope and jig.



■ CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Item	Symbol	max	Unit	Conditions
Input Capacitance	C_{IN}	5.0	pF	$V_{IN} = 0\text{V}$
Output Capacitance	C_{OUT}	7.0	pF	$V_{OUT} = 0\text{V}$

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS ($V_{CC} = 5\text{V} \pm 10\%$, $T_a = 0^\circ\text{C}$ to 70°C , unless otherwise noted.)

● READ CYCLE

Item	Symbol	HM6787-25		HM6787-30		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	25	—	30	—	ns	
Address Access Time	t_{AA}	—	25	—	30	ns	
Chip Select Access Time	t_{ACS}	—	25	—	30	ns	
Output Hold from Address Change	t_{OH}	5	—	5	—	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	15	0	15	ns	1, 2
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns	2
Chip Deselection to Power Down Time	t_{PD}	—	25	—	30	ns	2
Input Voltage Rise/Fall Time	t_T	—	150	—	150	ns	3

- Notes) 1. Transition is measured $\pm 200\text{mV}$ from steady state voltage with specified loading in Load B.
 2. This parameter is sampled and not 100% tested.
 3. If t_T becomes more than 150ns, there is possibility of function fail.
 Please contact your nearest Hitachi's Sale Dept. regarding specification.

● WRITE CYCLE

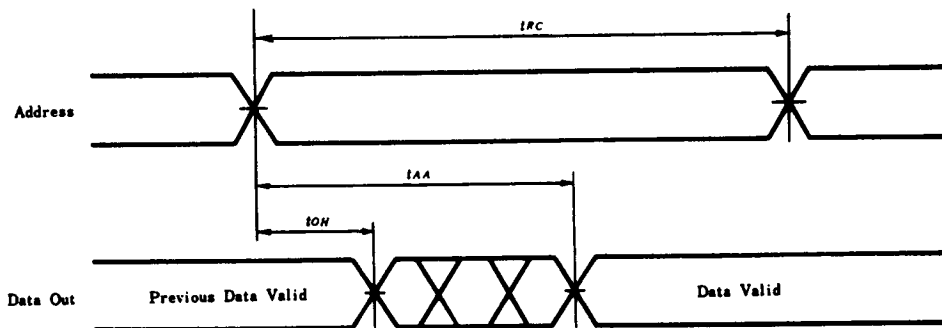
Item	Symbol	HM6787-25		HM6787-30		Unit	Notes
		min.	max.	min.	max.		
Write Cycle Time	t_{WC}	25	—	30	—	ns	2
Chip Selection to End of Write	t_{CW}	20	—	25	—	ns	
Address Valid to End of Write	t_{AW}	20	—	25	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	ns	
Write Pulse Width	t_{WP}	20	—	25	—	ns	
Write Recovery Time	t_{WR}	5	—	5	—	ns	
Data Valid to End of Write	t_{DW}	20	—	25	—	ns	
Data Hold Time	t_{DH}	0	—	0	—	ns	
Write Enable to Output in High Z	t_{WZ}	0	15	0	15	ns	3, 4
Output Active from End of Write	t_{OW}	0	—	0	—	ns	3, 4

- Note: 1. If $\overline{\text{CS}}$ goes high simultaneously with $\overline{\text{WE}}$ high, the output remains in a high impedance state.
 2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
 3. Transition is measured $\pm 200\text{mV}$ from steady state voltage with specified loading in Load B.
 4. This parameter is sampled and not 100% tested.

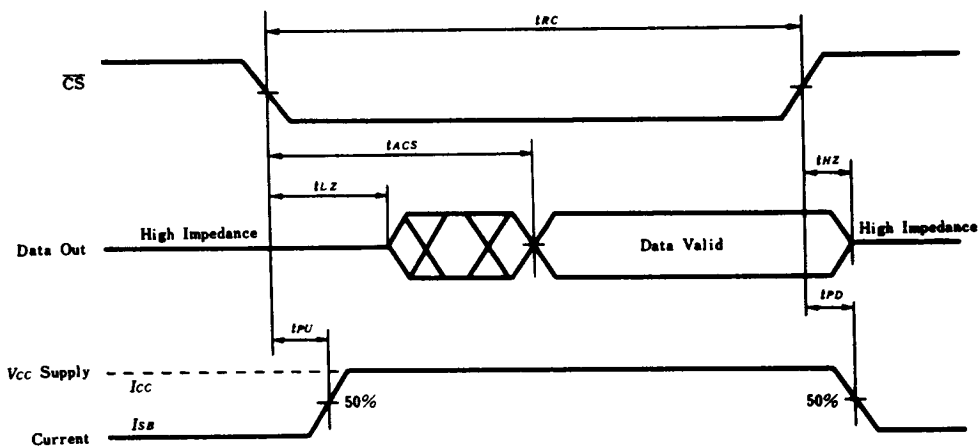


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• TIMING WAVEFORM OF READ CYCLE NO. 1^{1), 2)}



• TIMING WAVEFORM OF READ CYCLE NO. 2^{1), 3)}



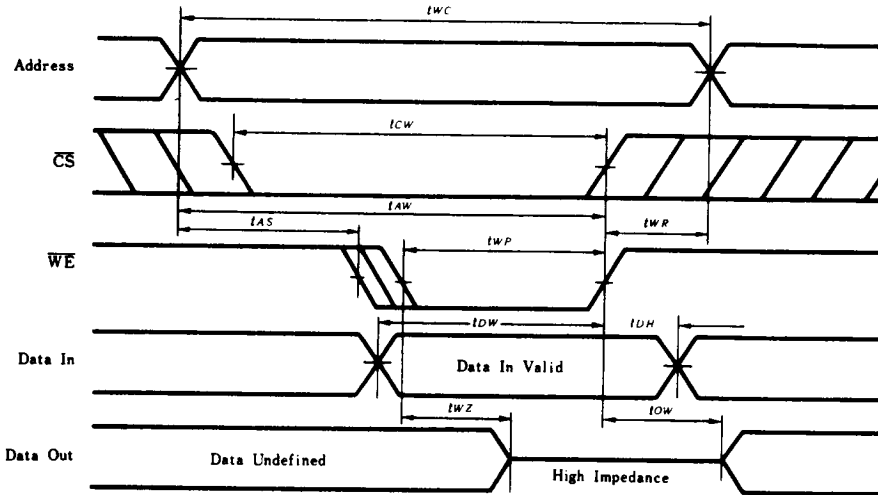
Note: 1. $\overline{WE}$ is high and $\overline{CS}$ is low for READ cycle.

2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.

3. Transition is measured $\pm 200\text{mV}$ from steady state voltage with specified loading in Load B.

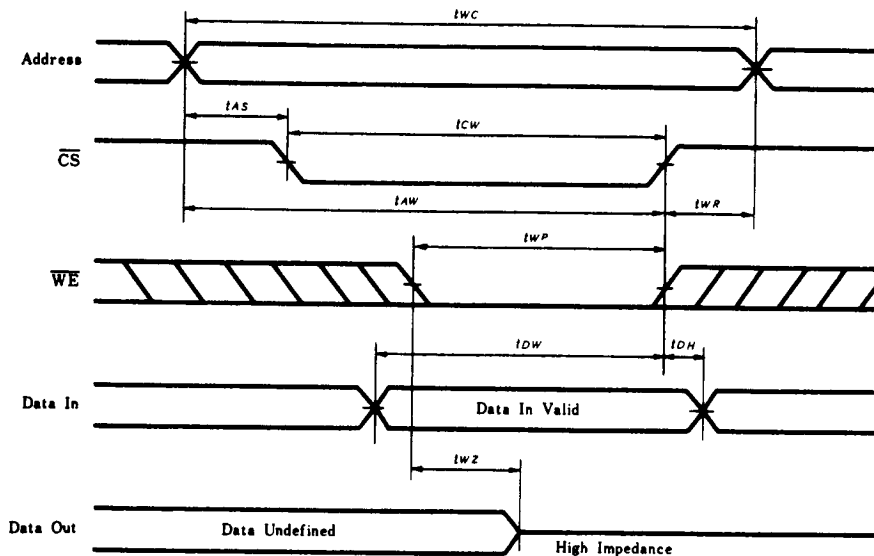


● TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)



Note: 1. Transition is measured $\pm 200\text{mV}$ from steady state voltage with specified loading in Load B.

● TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)



Note: 1. Transition is measured $\pm 200\text{mV}$ from steady state voltage with specified loading in Load B.



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