

DESCRIPTION

The HY53C256 is fast dynamic RAM organized 262,144 x 1-bit. The HY53C256 utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY53C256 to be packaged in a standard 300mil 16pin PDIP, 330mil 18pin PLCC.

The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of $5V \pm 10\%$ tolerance and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- Low power dissipation
Max. CMOS standby 5.5mW (L-part)
11.0mW
- Max. TTL standby 11.0mW (L-part)
16.5mW

Max. operating

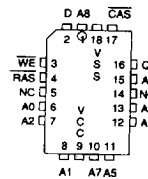
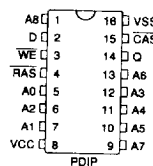
Speed	Power
70	385mW
80	330mW
10	275mW

- Single power supply of $5V \pm 10\%$
 - TTL compatible inputs and outputs
 - Fast access time
- | Speed | t _{RAC} | t _{CAC} | t _{PC} |
|-------|------------------|------------------|-----------------|
| 70 | 70ns | 15ns | 50ns |
| 80 | 80ns | 20ns | 55ns |
| 10 | 100ns | 25ns | 60ns |
- Fast page mode operation
 - Read-Modify-Write capability
 - CAS-before-RAS, RAS-only, Hidden refresh
 - 256 refresh cycles / 4ms

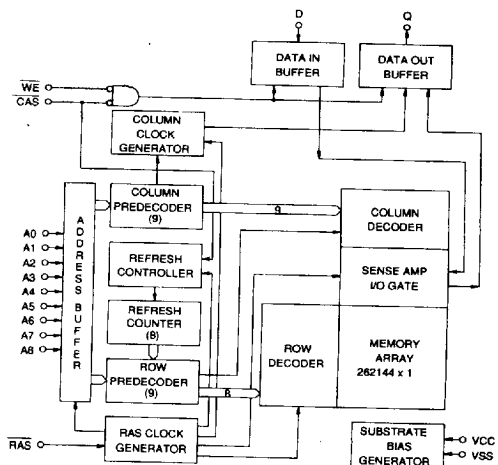
PIN DESCRIPTION

RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
A0-A8	Address Input
D	Data Input
Q	Data Output
Vcc	Power (+ 5V)
Vss	Ground

PIN CONNECTION



BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 125	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-1.0 to 7.0	V
Vcc	Voltage on Vcc Relative to Vss	-1.0 to 7.0	V
Ios	Short Circuit Output Current	50	mA
Pd	Power Dissipation	1.0	W
TSOLDER	Soldering Temperature• Time	260• 10	°C• sec

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Vcc	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	Vcc+ 1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to Vss.

DC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 5V± 10%, VSS= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pins)	VSS≤ VIN≤ VCC, All other pins not under test= VSS		-10	10	μA	
ILO	Output Leakage Current (High Impedance State)	VSS≤ VOUT≤ VCC, RAS & CAS at VIH		-10	10	μA	
ICC1	VCC Supply Current, Operating	tRC= tRC (min.)	70 80 100	- - -	70 60 50	mA	1,2,3
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at VIH, other inputs≥ VSS	L-part	- -	3 2	mA	4
ICC3	VCC Supply Current, RAS-only refresh	tRC= tRC (min.)	70 80 100	- - -	70 60 50	mA	1,3
ICC4	VCC Supply Current, Fast Page mode	tPC= tPC (min.)	70 80 100	- - -	45 40 35	mA	1,2,3
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS ≤ VCC-0.2V	L-part	- -	2 1	mA	4
ICC6	VCC Supply Current, CAS-before-RAS refresh	tRC= tRC (min.)	70 80 100	- - -	70 60 50	mA	1,3
VOL	Output Low Voltage	IOL= 4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH= -5mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4 and ICC6 depend on cycle rate.
2. ICC1 and ICC4 depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while RAS= VIL and CAS= VIH.
4. ICC2(max.)= 2mA and ICC5(max.)= 1mA are only applied to L-part only (HY53C256LS and HY53C256LF).

AC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 5V± 10%, VSS= 0V, unless otherwise noted.) NOTE : 1, 2, 3

(TA= 0°C to 70°C, VCC= 5V± 10%, VSS= 0V, unless otherwise noted.) NOTE : 1, 2, 3										
#	SYMBOL	PARAMETER	HY53C256S/F/LS/LF						UNIT	NOTE
			-70		-80		-10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	130	-	145	-	175	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	155	-	175	-	210	-	ns	
3	tPC	Fast Page Mode Cycle Time	50	-	55	-	60	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	75	-	85	-	95	-	ns	
5	tRAC	Access Time from RAS	-	70	-	80	-	100	ns	4,9,10
6	tCAC	Access Time from CAS	-	15	-	20	-	25	ns	4,9
7	tAA	Access Time from Column Address	-	35	-	40	-	45	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	45	-	50	-	55	ns	4
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	15	0	20	0	25	ns	5
11	tT	Transition Time (Rise and Fall)	3	25	3	25	3	25	ns	3
12	tRP	RAS Precharge Time	50	-	55	-	65	-	ns	
13	tRAS	RAS Pulse Width	70	75K	80	75K	100	75K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	70	75K	80	75K	100	75K	ns	
15	tRSH(W)	RAS Hold Time in Write Cycle	25	-	25	-	30	-	ns	
16	tCSH	CAS Hold Time	70	-	80	-	100	-	ns	
17	tCAS(W)	CAS Pulse Width in Write Cycle	20	-	25	-	30	-	ns	
18	tRCD	RAS to CAS Delay	25	55	25	60	25	75	ns	9
19	tRAD	RAS to Column Address Delay Time	20	35	20	40	20	55	ns	10
20	tCRP	CAS to RAS Precharge Time	15	-	15	-	15	-	ns	
21	tCP	CAS Precharge Time	15	-	15	-	20	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	15	-	15	-	15	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	15	-	15	-	20	-	ns	
26	tAR	Column Address Hold Time from RAS	55	-	60	-	70	-	ns	
27	tRAL	Column Address to RAS Lead Time	35	-	40	-	45	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to CAS	5	-	5	-	5	-	ns	6
30	tRRH	Read Command Hold Time Referenced to RAS	5	-	5	-	5	-	ns	6
31	tWCH	Write Command Hold Time	15	-	15	-	20	-	ns	
32	tWCR	Write Command Hold Time from RAS	55	-	60	-	70	-	ns	
33	tWP	Write Command Pulse Width	15	-	15	-	20	-	ns	
34	tRWL	Write Command to RAS Lead Time	20	-	25	-	30	-	ns	
35	tCWL	Write Command to CAS Lead Time	20	-	25	-	30	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	15	-	15	-	20	-	ns	7
38	tDHR	Data-In Hold Time Referenced to RAS	55	-	60	-	70	-	ns	
39	tREF	Refresh Period (256 cycles)	-	4	-	4	-	4	ms	
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

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AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY53C256S/F/LS/LF						UNIT	NOTE
			-70		-80		-10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	CAS to WE Delay Time	15	-	20	-	25	-	ns	8
42	tRWD	RAS to WE Delay Time	70	-	80	-	100	-	ns	8
43	tAWD	Column Address to WE Delay Time	35	-	40	-	45	-	ns	8
44	tCSR	CAS Set-up Time (CBR Cycle)	10	-	10	-	10	-	ns	
45	tCHR	CAS Hold Time (CBR Cycle)	20	-	25	-	30	-	ns	
46	tRPC	RAS to CAS Precharge Time	0	-	0	-	0	-	ns	
47	tCPT	CAS Precharge Time (CBR Counter Test)	15	-	15	-	20	-	ns	
48	tRSH(R)	RAS Hold Time in Read Cycle	15	-	20	-	25	-	ns	
49	tCAS(R)	CAS Pulse Width in Read Cycle	15	75K	20	75K	25	75K	ns	
50	tRRW	RAS Pulse Width (RMW)	95	-	110	-	135	-	ns	

NOTE :

1. An initial pause of 200 μ s is required after power-up followed by 8 RAS only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS cycles are required.
2. AC measurements assume $t_T = 5$ ns.
3. $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. $t_{OFF}(\text{max.})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in Read-Modify-Write cycles.
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}(\text{min.})$, $t_{CWD} \geq t_{CWD}(\text{min.})$ and $t_{AWD} \geq t_{AWD}(\text{min.})$ the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the $t_{RCD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
10. Operation within the $t_{RAD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .

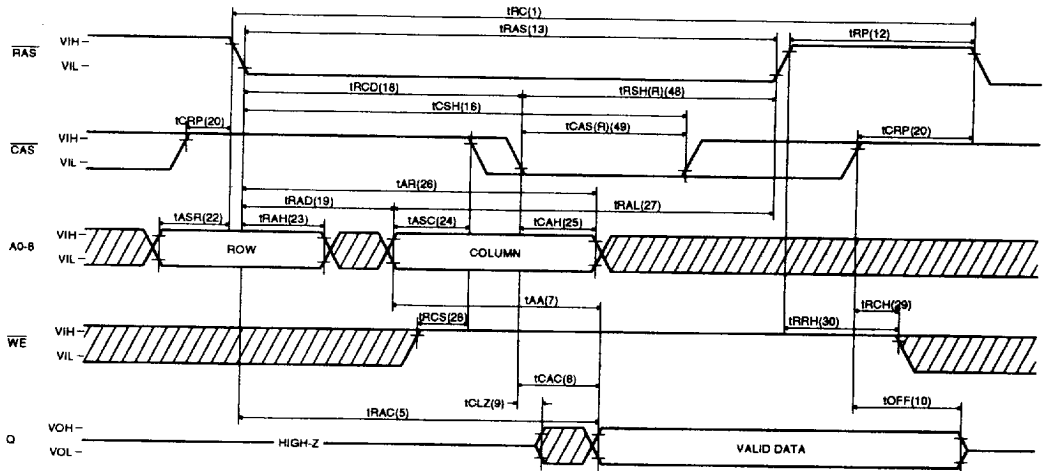
CAPACITANCE

($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, $f = 1\text{MHz}$, unless otherwise noted.)

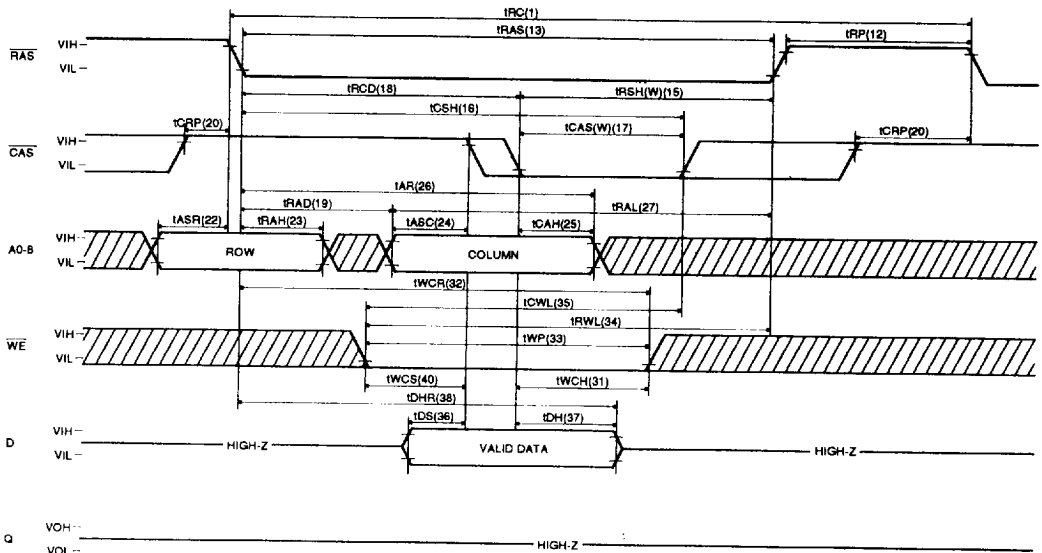
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A8, D)	-	6	pF
CIN2	Input Capacitance (RAS, CAS, WE)	-	8	pF
COUT	Output Capacitance (Q)	-	8	pF

TIMING DIAGRAM

READ CYCLE



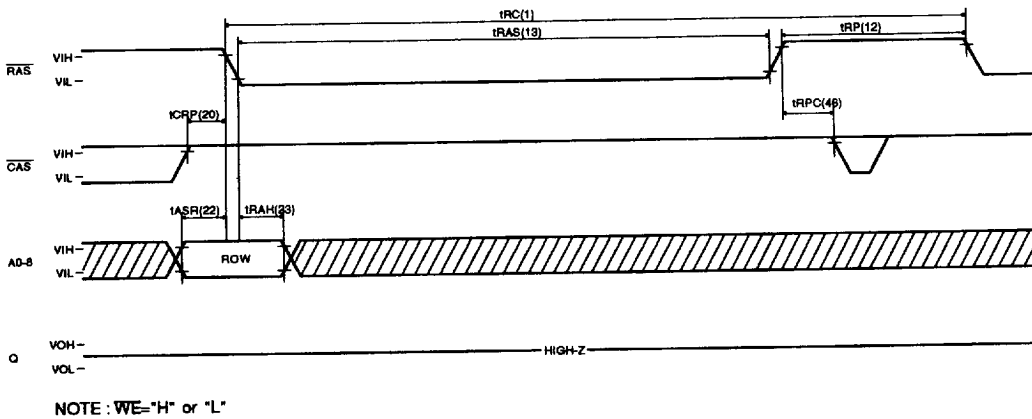
EARLY WRITE CYCLE



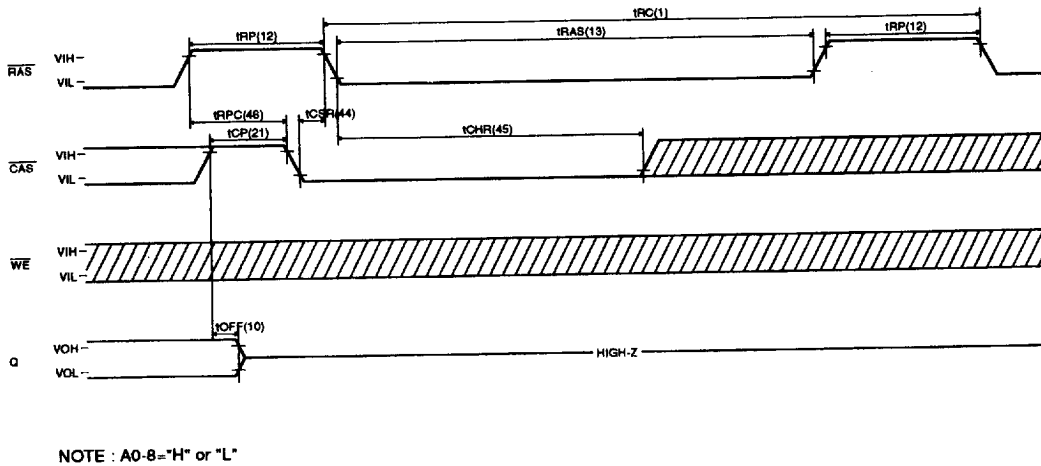
The timing diagram illustrates the relationship between several control and data signals for the 64160 device. The signals shown are RAS, CAS, A0-B, WE, D, and Q. The diagram includes various timing parameters such as $t_{RRW}(50)$, $t_{CSH}(16)$, $t_{RSH}(W)(15)$, $t_{CAS}(W)(17)$, $t_{RBP}(20)$, $t_{RCD}(18)$, $t_{RAD}(19)$, $t_{IAR}(26)$, $t_{IAL}(27)$, $t_{ASR}(22)$, $t_{IAH}(23)$, $t_{ASC}(24)$, $t_{CAH}(25)$, $t_{RSC}(28)$, $t_{CWD}(41)$, $t_{RWD}(42)$, $t_{AWD}(43)$, $t_{CWL}(35)$, $t_{RWL}(34)$, $t_{WIP}(33)$, $t_{AA}(7)$, $t_{CAC}(6)$, $t_{QS}(36)$, $t_{QH}(37)$, $t_{CLZ}(9)$, $t_{AC}(5)$, $t_{OFF}(10)$, and $t_{TRAC}(5)$. The diagram also shows the valid data period for the data bus (D) and the output (Q) during the HIGH-Z state.

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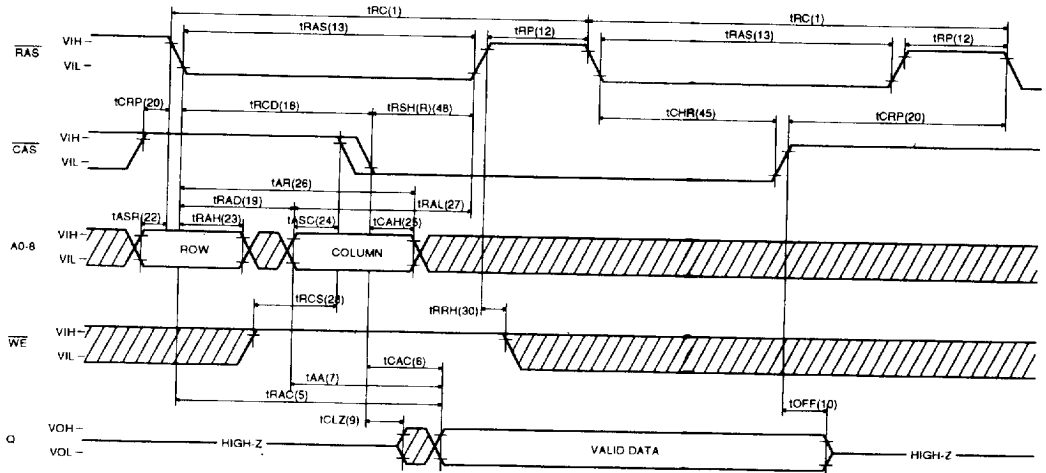
RAS-ONLY REFRESH CYCLE



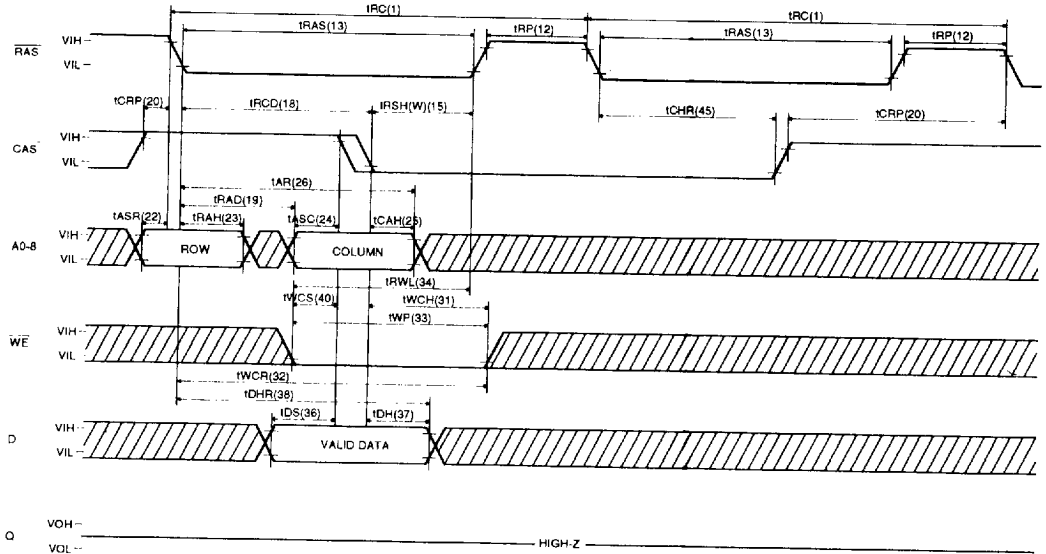
CAS-BEFORE-RAS REFRESH CYCLE



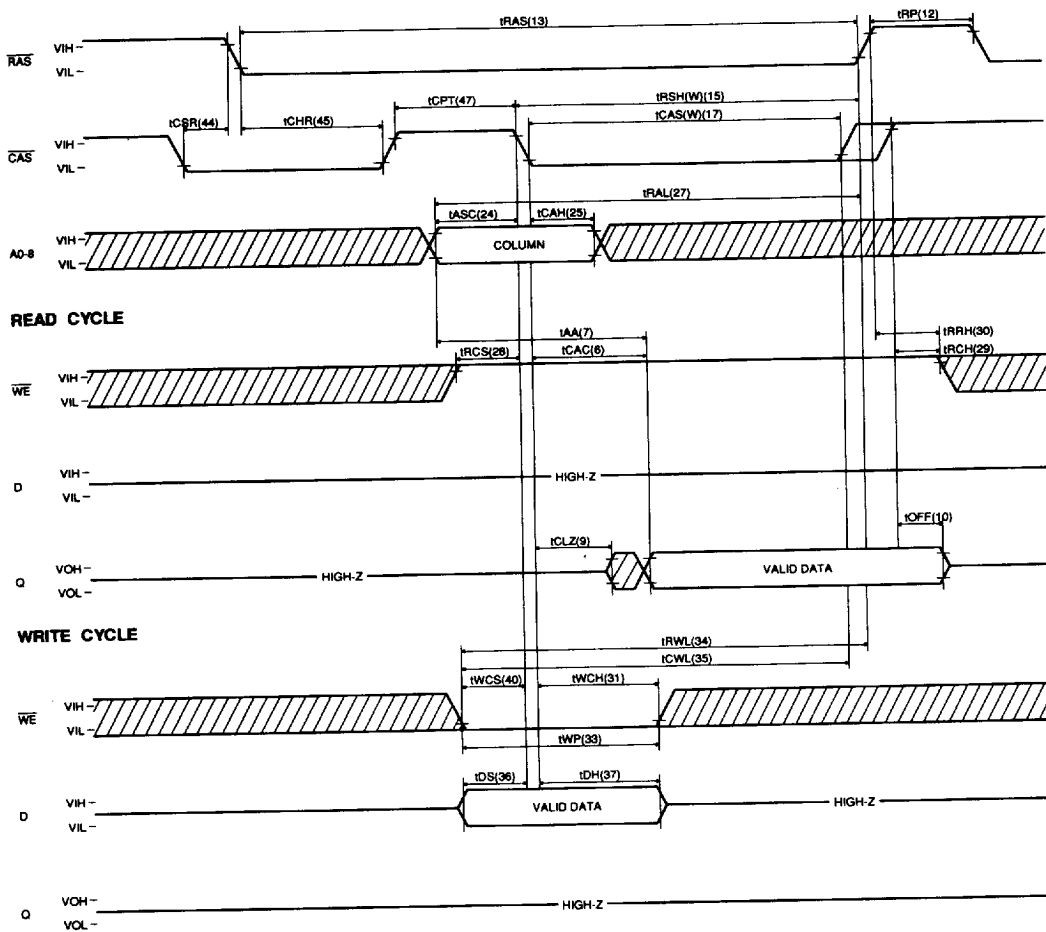
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

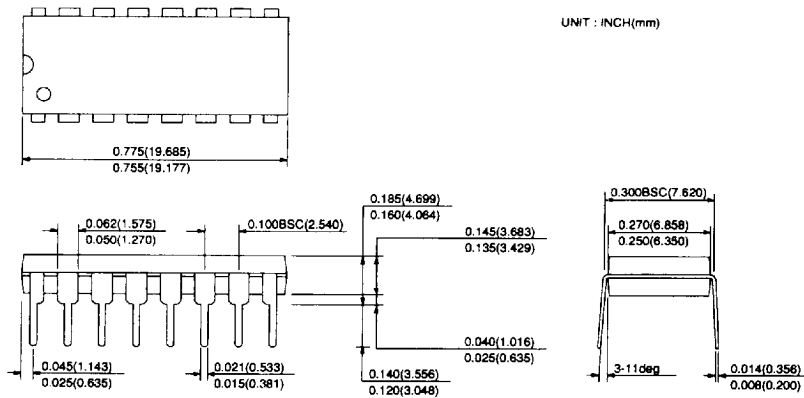


CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

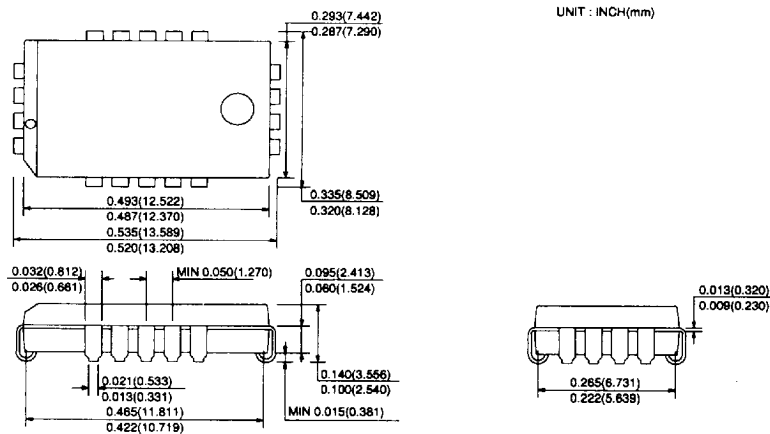


PACKAGE INFORMATION

300 mil 16 pin Plastic Dual In Line Package (S)



330 mil 18 pin Plastic Leaded Chip Carrier (F)



ORDERING INFORMATION

PART NO	SPEED	POWER	PACKAGE
HY53C256S	70/80/10		PDIP
HY53C256LS	70/80/10	L-part	PDIP
HY53C256F	70/80/10		PLCC
HY53C256LF	70/80/10	L-part	PLCC

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