HARRIS

IRFP9140R/P9141R IRFP9142R/P9143R

Avalanche Energy Rated P-Channel Power MOSFETs

August 1991

T-39-23

Features

- -19A and -16A, -60V and -100V
- $r_{DS(ON)}$ = 0.20Ω and 0.30Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

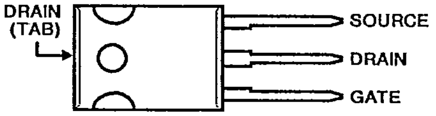
Description

The IRFP9140R, IRFP9141R, IRFP9142R and IRFP9143R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

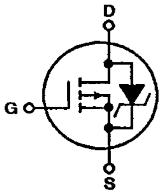
Package

TO-247
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRFP9140R	IRFP9141R	IRFP9142R	IRFP9143R	UNITS
Drain-Source Voltage (1) . . . . . V_{DS}	-100	-60	-100	-60	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) . . . . . V_{DGR}	-100	-60	-100	-60	V
Continuous Drain Current					
T_C = 25°C . . . . . I_D	-19	-19	-16	-16	A
T_C = 100°C . . . . . I_D	-12	-12	-10	-10	A
Pulsed Drain Current (3) . . . . . I_{DM}	-76	-76	-64	-64	A
Gate-Source Voltage . . . . . V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation . . . . . P_D (See Figure 14)	150	150	150	150	W
Linear Derating Factor . . . . . (See Figure 14)	1.2	1.2	1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (4) . . . . . E_{as}	960	960	960	960	mJ
Operating and Storage Junction . . . . . TJ, TSTG Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering . . . . . T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 4.2mHμ, R_G = 25Ω, Peak I_L = 19A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number 2292

Specifications IRFP9140R, IRFP9141R, IRFP9142R, IRFP9143R

Electrical Characteristics $T_C = +25^oC$, Unless Otherwise Specified

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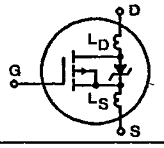
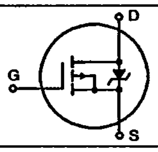
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage IRFP9140R, IRFP9142R	BV_{DSS}	$V_{GS} = 0V$, $I_D = -250\mu A$	-100	-	-	V
IRFP9141R, IRFP9143R			-60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, $I_D = -250\mu A$	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	$V_{GS} = 20V$	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	$V_{GS} = -20V$	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, $V_{GS} = 0V$	-	-	250	µA
		V_{DS} = Max Rating x 0.8, $V_{GS} = 0V$, $T_J = +125^oC$	-	-	1000	µA
On-State Drain Current (Note 2) IRFP9140R, IRFP9141R	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, $V_{GS} = -10V$	-19	-	-	A
IRFP9142R, IRFP9143R			-16	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFP9140R, IRFP9141R	$r_{DS(ON)}$	$V_{GS} = -10V$, $I_D = -10A$	-	0.14	0.20	Ω
IRFP9142R, IRFP9143R			-	0.20	0.30	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \leq -50V$, $I_D = -10A$	5.3	7.9	-	S(℧)
Input Capacitance	C_{ISS}	$V_{GS} = 0V$, $V_{DS} = -25V$, f = 1.0MHz See Figure 10	-	1200	-	pF
Output Capacitance	C_{OSS}		-	570	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	160	-	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = -50V$, $I_D = -19A$, $R_G = 9.1\Omega$ See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	16	20	ns
Rise Time	t_r		-	65	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	47	70	ns
Fall Time	t_f		-	28	70	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	$V_{GS} = -10V$, $I_D = -19A$, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	37	55	nC
Gate-Source Charge	Q_{gs}		-	8.7	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	22	-	nC
Internal Drain Inductance	L_D	Measured between contact screw on header that is closer to source & gate pins & center of die. Modified MOSFET symbol showing the internal device inductances.	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source pin, 6mm (0.25") from header & source bonding pad. 	-	13	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free Air Operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-19	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-76	A
Diode Forward Voltage (Note 2)	V_{SD}	$T_J = +25^oC$, $I_S = -19A$, $V_{GS} = 0V$	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	$T_J = +25^oC$, $I_F = -18A$, $dI_F/dt = 100A/\mu s$	-	210	-	ns
Reverse Recovered Charge	Q_{RR}		-	2.0	-	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	-	-	-	-

NOTES:
1. $T_J = +25^oC$ to $+150^oC$
2. Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. $V_{DD} = 50V$, Start $T_J = +25^oC$, $L = 4.2mH\mu$, $R_G = 25\Omega$, Peak $I_L = 19A$ (See Figures 15 and 16)

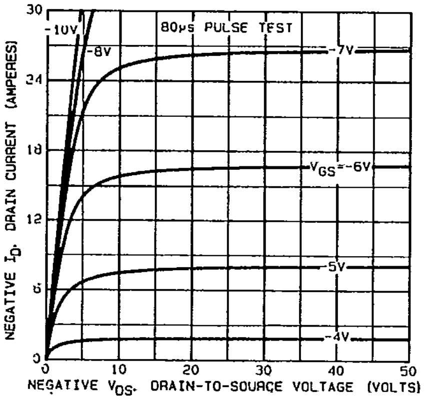


Fig. 1 - Typical output characteristics.

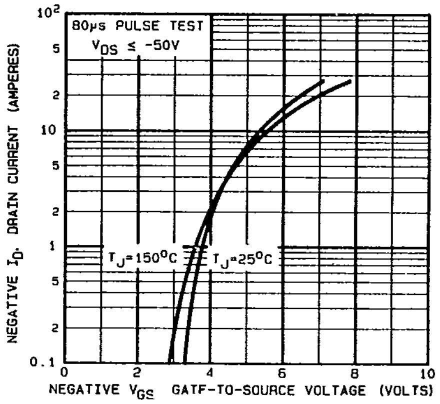


Fig. 2 - Typical transfer characteristics.

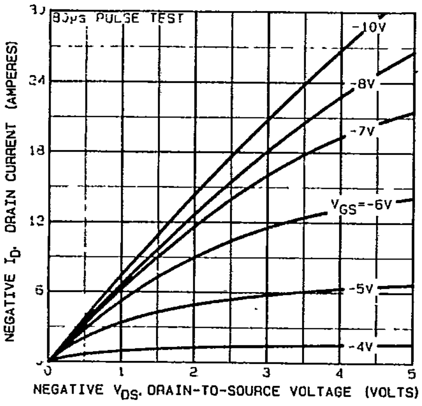


Fig. 3 - Typical saturation characteristics.

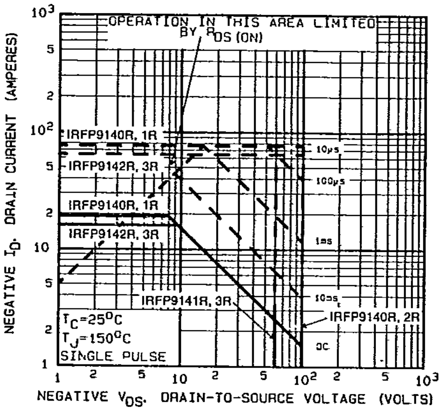


Fig. 4 - Maximum safe operating area.

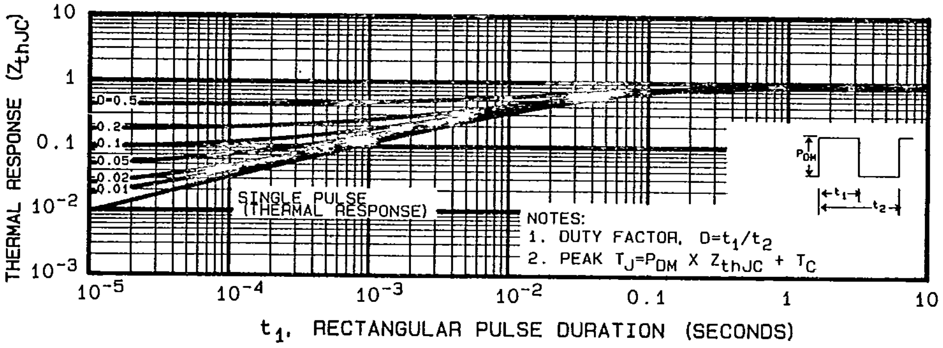


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

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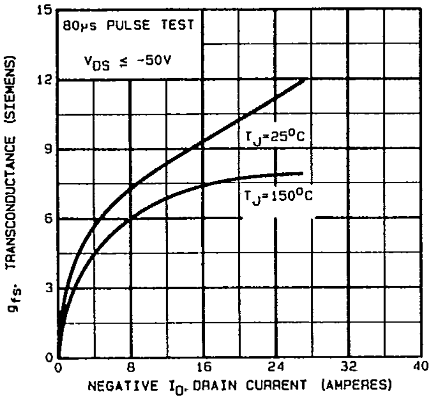

Fig. 6 - Typical transconductance vs. drain current.

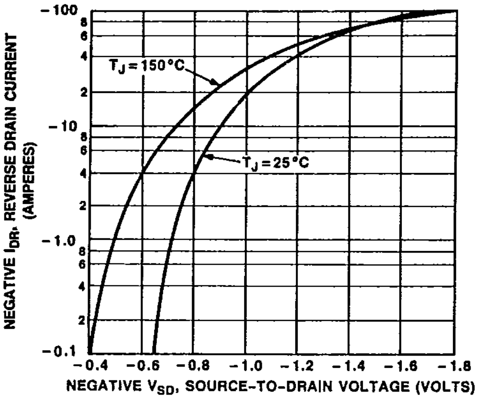

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Fig. 7 - Typical source-drain diode forward voltage.

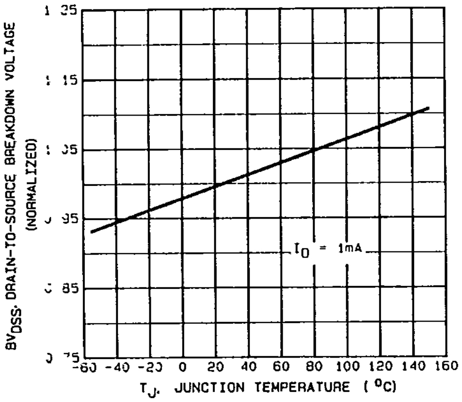

Fig. 8 - Breakdown voltage vs. temperature.

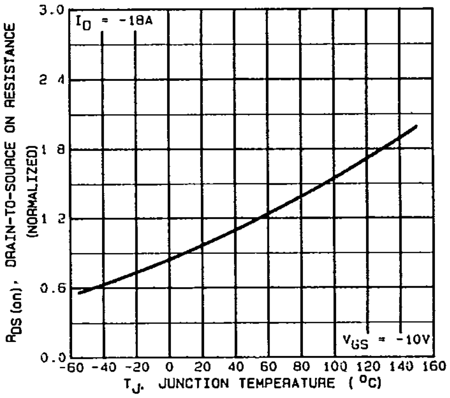

Fig. 9 - Normalized on-resistance vs. temperature.

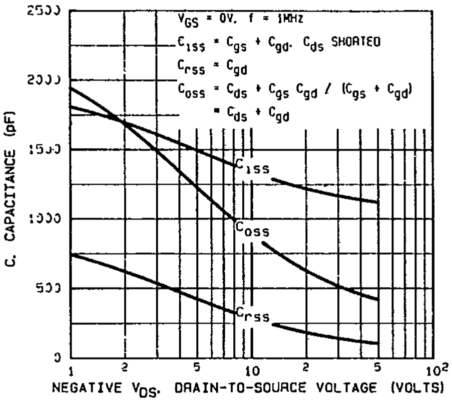

Fig. 10 - Typical capacitance vs. drain-to-source voltage.

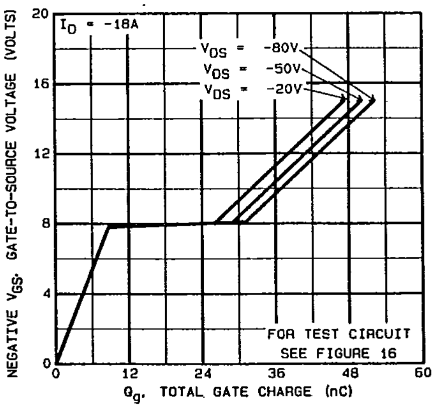

Fig. 11 - Typical gate charge vs. gate-to-source voltage.

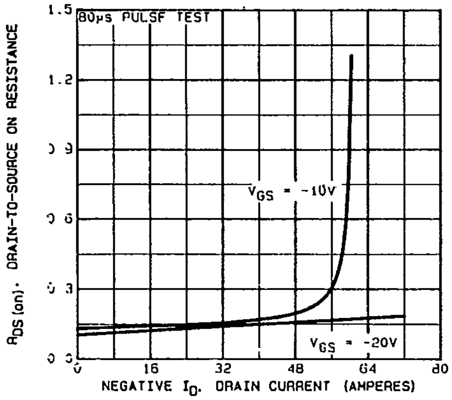

Fig. 12 - Typical on-resistance vs. drain current.

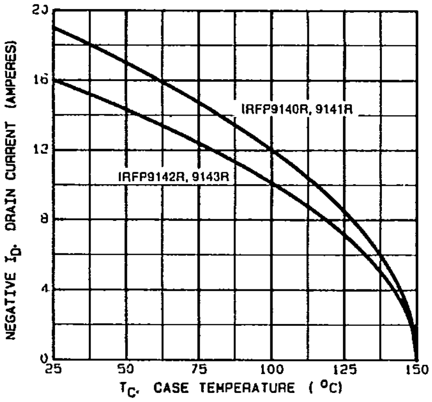

Fig. 13 - Maximum drain current vs. case temperature.

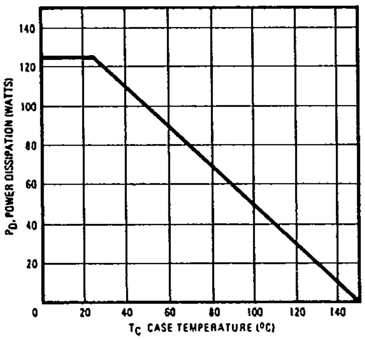

Fig. 14 - Power vs. temperature derating curve.

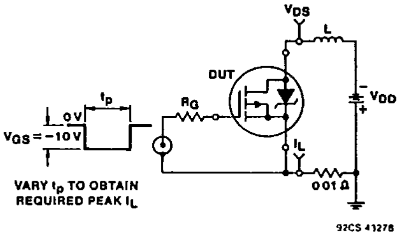

Fig. 15 - Unclamped inductive test circuit.

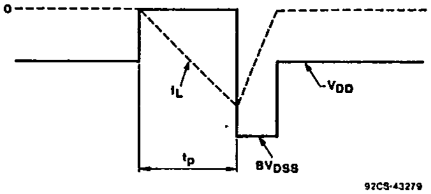

Fig. 16 - Unclamped inductive waveforms.

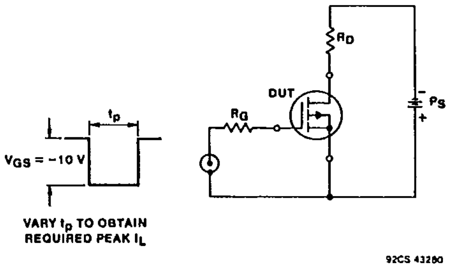

Fig. 17 - Switching time test circuit.

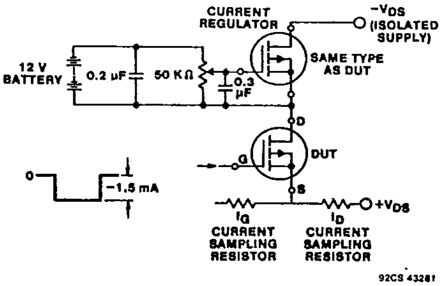

Fig. 18 - Gate charge test circuit.