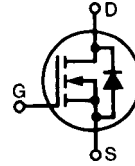


HiPerFET™ Power MOSFETs

N-Channel Enhancement Mode
High dv/dt, Low t_{rr} , HDMOS™ Family

IXFH/IXFM21N50
IXFH/IXFM/IXFT24N50
IXFH/IXFT26N50

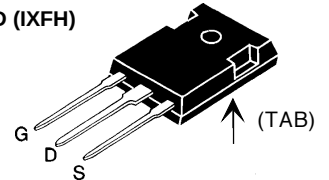


V_{DSS}	I_{D25}	$R_{DS(on)}$
500 V	21 A	0.25 Ω
500 V	24 A	0.23 Ω
500 V	26 A	0.20 Ω

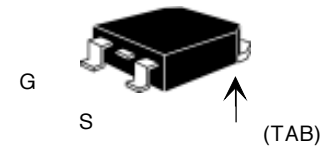
$t_{rr} \leq 250$ ns

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	500	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 1\text{ M}\Omega$	500	V
V_{GS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_C = 25^\circ\text{C}$	21N50	21 A
		24N50	24 A
		26N50	26 A
I_{DM}	$T_C = 25^\circ\text{C}$, pulse width limited by T_{JM}	21N50	84 A
		24N50	96 A
		26N50	104 A
I_{AR}	$T_C = 25^\circ\text{C}$	21N50	21 A
		24N50	24 A
		26N50	26 A
E_{AR}	$T_C = 25^\circ\text{C}$	30	mJ
dv/dt	$I_S \leq I_{DM}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ\text{C}$, $R_G = 2\ \Omega$	5	V/ns
P_D	$T_C = 25^\circ\text{C}$	300	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
T_L	1.6 mm (0.062 in.) from case for 10 s	300	$^\circ\text{C}$
M_d	Mounting torque	1.13/10	Nm/lb.in.
Weight		TO-204 = 18 g, TO-247 = 6 g	

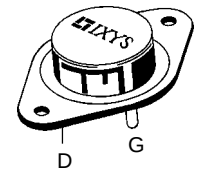
TO-247 AD (IXFH)



TO-268 (D3) Case Style



TO-204 AE (IXFM)



G = Gate, D = Drain,
S = Source, TAB = Drain

Features

- International standard packages
- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
- easy to drive and to protect
- Fast intrinsic Rectifier

Applications

- DC-DC converters
- Synchronous rectification
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- AC motor control
- Temperature and lighting controls
- Low voltage relays

Advantages

- Easy to mount with 1 screw (TO-247) (isolated mounting screw hole)
- High power surface mountable package
- High power density

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
V_{DSS}	$V_{GS} = 0\text{ V}$, $I_D = 250\ \mu\text{A}$	500		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 4\text{ mA}$	2		4 V
I_{GSS}	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0$			± 100 nA
I_{DSS}	$V_{DS} = 0.8 \cdot V_{DSS}$	$T_J = 25^\circ\text{C}$		200 μA
	$V_{GS} = 0\text{ V}$	$T_J = 125^\circ\text{C}$		1 mA



IXFH21N50
IXFM21N50

IXFH24N50
IXFM24N50
IXFT24N50

IXFH26N50
IXFM26N50
IXFT26N50

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 0.5 I_{D25}$ Pulse test, $t \leq 300\text{ }\mu\text{s}$, duty cycle $d \leq 2\%$	21N50 24N50 26N50		0.25 Ω 0.23 Ω 0.20 Ω
g_{fs}	$V_{DS} = 10\text{ V}$; $I_D = 0.5 I_{D25}$, pulse test	11	21	S
C_{iss} C_{oss} C_{rss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$		4200 450 135	pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	$V_{GS} = 10\text{ V}$, $V_{DS} = 0.5 V_{DSS}$, $I_D = 0.5 I_{D25}$ $R_G = 2\text{ }\Omega$ (External)		16 33 65 30	25 ns 45 ns 80 ns 40 ns
$Q_{g(on)}$ Q_{gs} Q_{gd}	$V_{GS} = 10\text{ V}$, $V_{DS} = 0.5 V_{DSS}$, $I_D = 0.5 I_{D25}$		135 28 62	160 nC 40 nC 85 nC
R_{thJC} R_{thCK}	(TO-247 Case Style)		0.25	0.42 K/W K/W

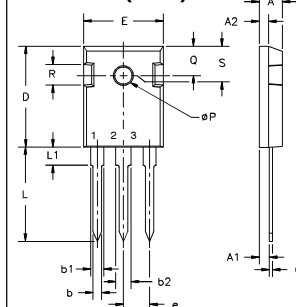
Source-Drain Diode

Characteristic Values
($T_J = 25^\circ\text{C}$, unless otherwise specified)

Symbol	Test Conditions	Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{ V}$	21N50 24N50 26N50		21 A 24 A 26 A
I_{SM}	Repetitive; pulse width limited by T_{JM}	21N50 24N50 26N50		84 A 96 A 104 A
V_{SD}	$I_F = I_S$, $V_{GS} = 0\text{ V}$, Pulse test, $t \leq 300\text{ }\mu\text{s}$, duty cycle $d \leq 2\%$			1.5 V
t_{rr}	$I_F = I_S$ $T_J = 25^\circ\text{C}$			250 ns
Q_{RM}	$-di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 125^\circ\text{C}$		1	400 ns
I_{RM}	$V_R = 100\text{ V}$ $T_J = 25^\circ\text{C}$		10	μC A
	$T_J = 125^\circ\text{C}$		15	A

Note 1: Add "S" suffix for TO-247 SMD package option (ex: IXFH24N50S)

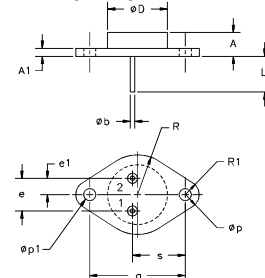
TO-247 AD (IXFH) Outline



Terminals:
1 - Gate
2 - Drain
3 - Source
Tab - Drain

Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.7	5.3	.185	.209
A ₁	2.2	2.54	.087	.102
A ₂	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b ₁	1.65	2.13	.065	.084
b ₂	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L ₁		4.50		.177
$\varnothing P$	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216
S	6.15	BSC	.242	BSC

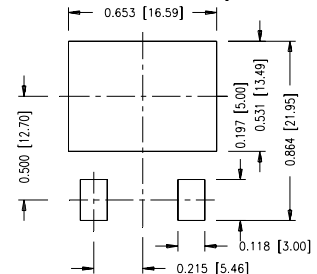
TO-204 AE (IXFM) Outline



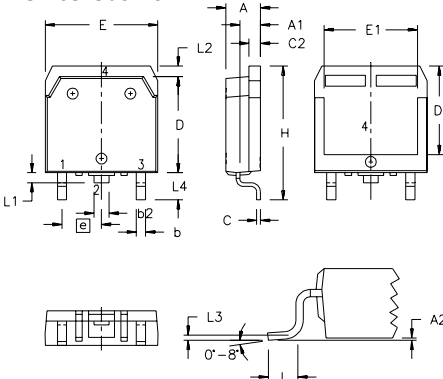
Pins: 1 - Gate, 2 - Source, Case - Drain

Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	6.4	11.4	.250	.450
A ₁	1.53	3.42	.060	.135
$\varnothing b$	1.45	1.60	.057	.063
$\varnothing D$		22.22		.875
e	10.67	11.17	.420	.440
e ₁	5.21	5.71	.205	.225
L	11.18	12.19	.440	.480
$\varnothing p$	3.84	4.19	.151	.165
$\varnothing p_1$	3.84	4.19	.151	.165
q	30.15	BSC	1.187	BSC
R	12.58	13.33	.495	.525
R ₁	3.33	4.77	.131	.188
s	16.64	17.14	.655	.675

Min. Recommended Footprint



TO-268 Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.193	.201	4.90	5.10
A ₁	.106	.114	2.70	2.90
A ₂	.001	.010	0.02	0.25
b	.045	.057	1.15	1.45
b ₂	.075	.083	1.90	2.10
C	.016	.026	0.40	0.65
C ₂	.057	.063	1.45	1.60
D	.543	.551	13.80	14.00
D ₁	.488	.500	12.40	12.70
E	.624	.632	15.85	16.05
E ₁	.524	.535	13.30	13.60
e		.215 BSC		5.45 BSC
H	.736	.752	18.70	19.10
L	.094	.106	2.40	2.70
L ₁	.047	.055	1.20	1.40
L ₂	.039	.045	1.00	1.15
L ₃		.010 BSC		0.25 BSC
L ₄	.150	.161	3.80	4.10

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,881,106 5,017,508 5,049,961 5,187,117 5,486,715
4,850,072 4,931,844 5,034,796 5,063,307 5,237,481 5,381,025

Fig. 1 Output Characteristics

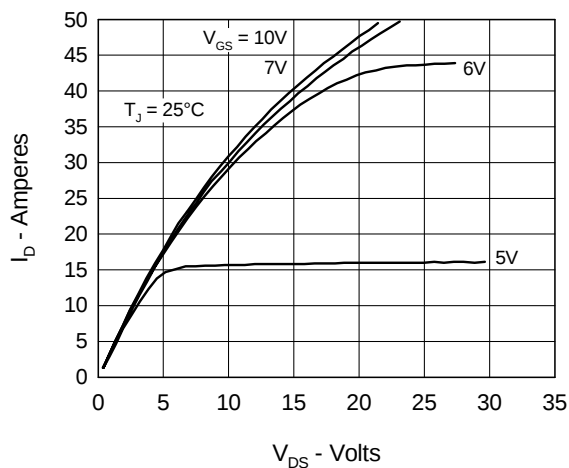


Fig. 2 Input Admittance

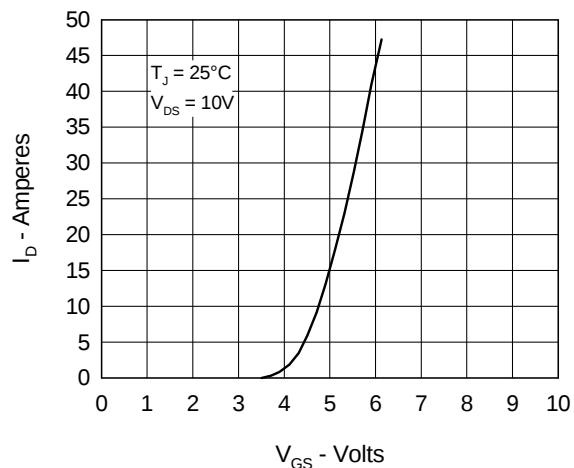
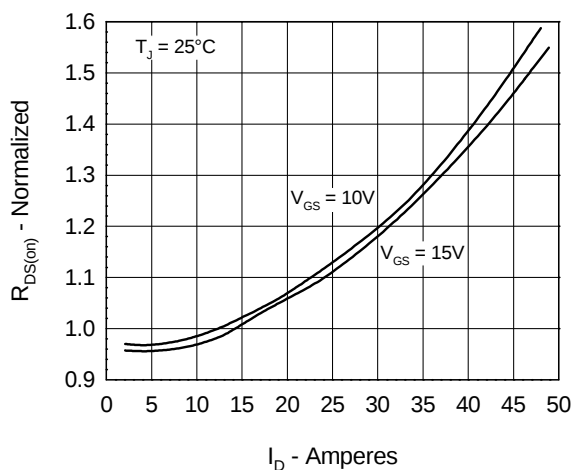

Fig. 3 $R_{DS(on)}$ vs. Drain Current


Fig. 4 Temperature Dependence of Drain to Source Resistance

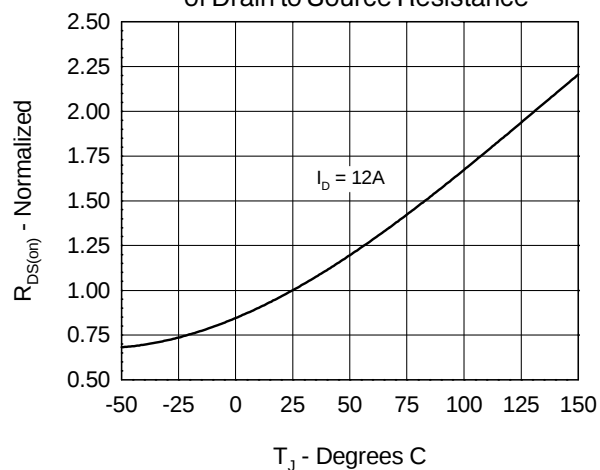


Fig. 5 Drain Current vs. Case Temperature

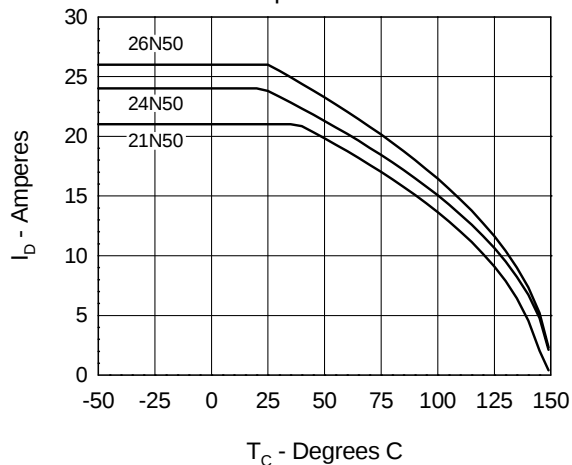


Fig. 6 Temperature Dependence of Breakdown and Threshold Voltage

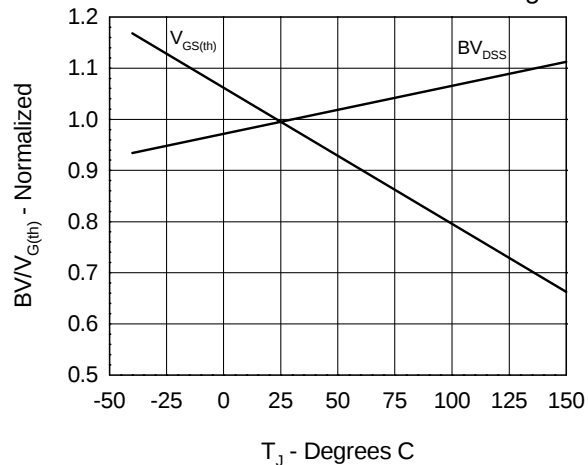


Fig.7 Gate Charge Characteristic Curve

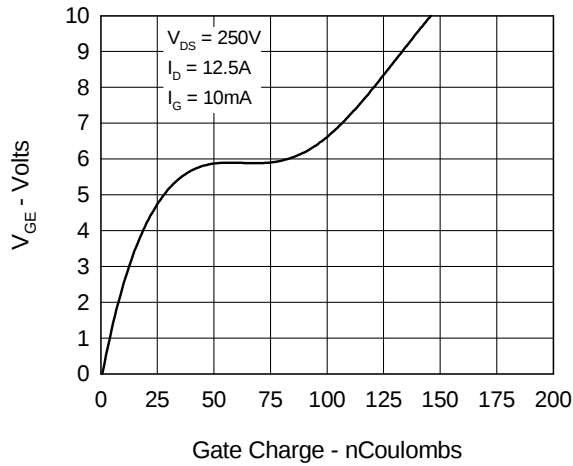


Fig.9 Capacitance Curves

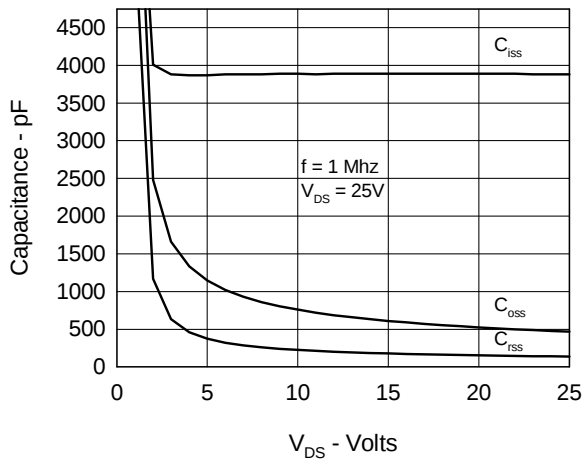


Fig.11 Transient Thermal Impedance

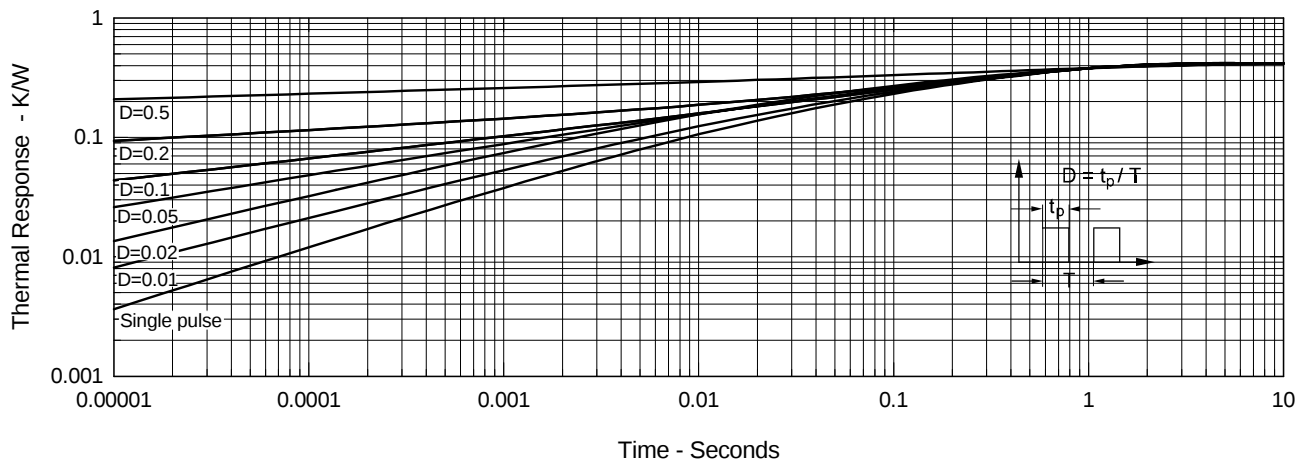


Fig.8 Forward Bias Safe Operating Area

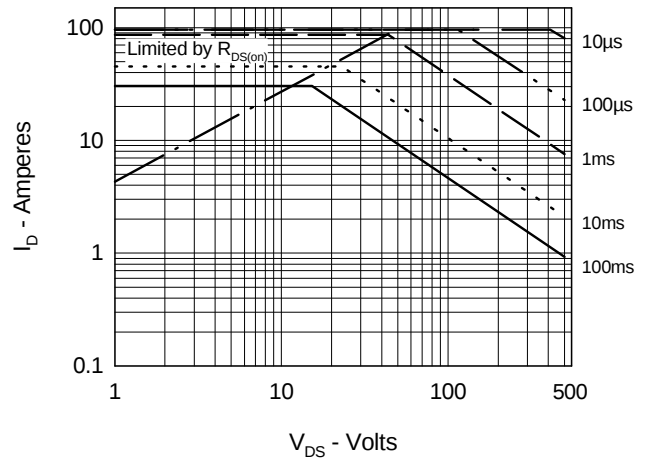


Fig.10 Source Current vs. Source to Drain Voltage

