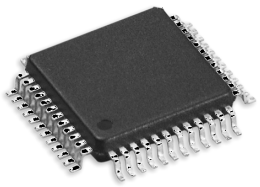
SPM + VCM 1 CHIP DRIVER

The KA2811C is a monolithic IC and an one-chip IC which includes SPM (Spindle motor) driver, VCM (Voice coil motor) driver and peripheral driver, designed for driving HDD motor. For high starting torque and high speed, SPM part employes WSS (Waltz step start) method for starting the motor and can drive up to 2A. VCM part is designed to drive up to 1.5A so that it is enabled to cope with the trends of HDD'S high speed. (Required external transistors).

48-QFPH-1414



FEATURES

SMP PART

- 3 phase sensorless BLDC motor driver with speed discriminator
- Built-in start-up circuit with WSS (Waltz step start) method
- Suitable for high and middle end set (Max. output current: 2A)
- Built-in dynamic brake circuit

VCM PART

- High output current driver with external NPN & PNP transistors. (Max. output current: 2A)
- No crossover distortion
- Low offset current

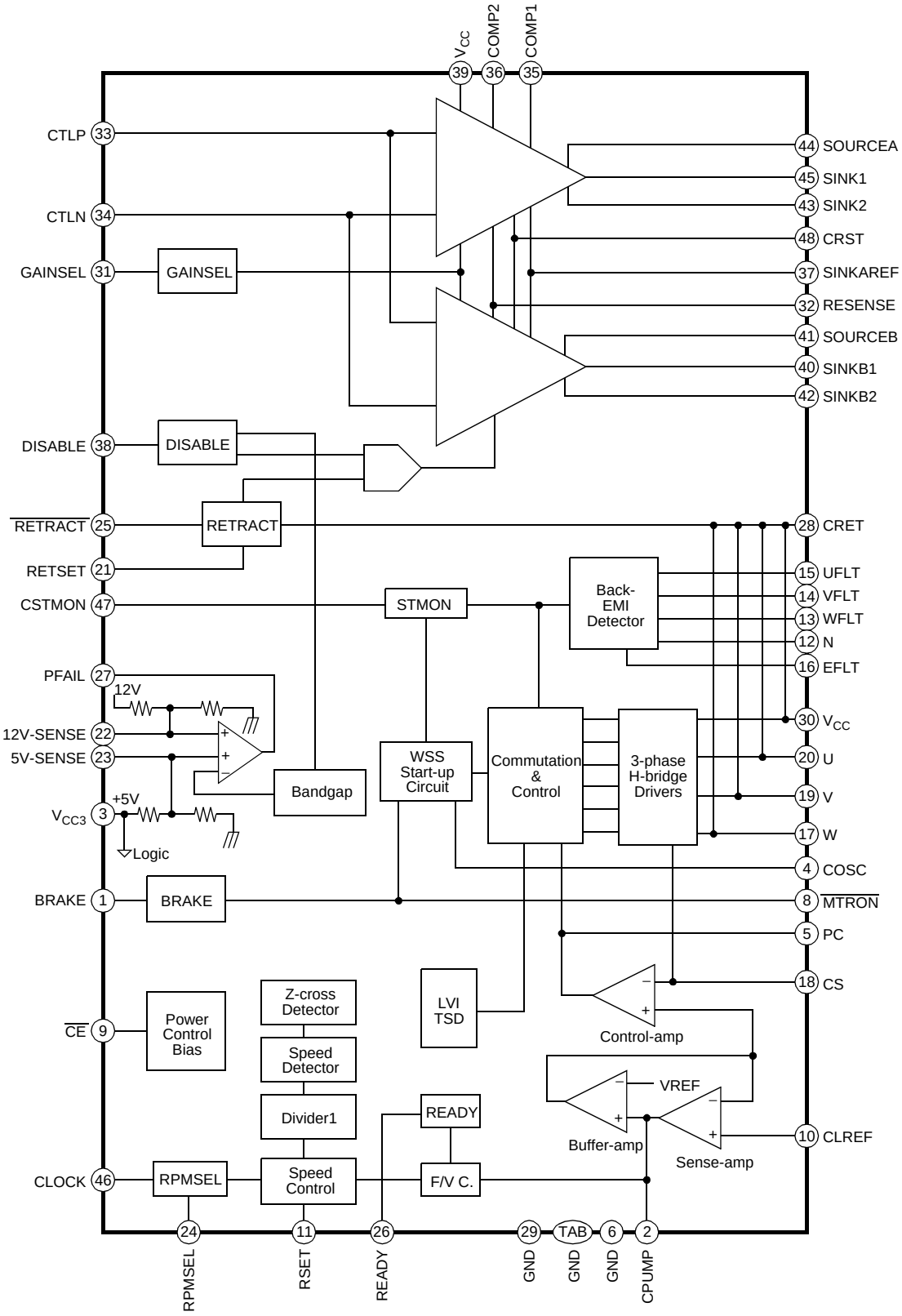
OTHER

- Low standby current
- Built-in precision power detectio circuit
- Built-in TSD

ORDERING INFORMATION

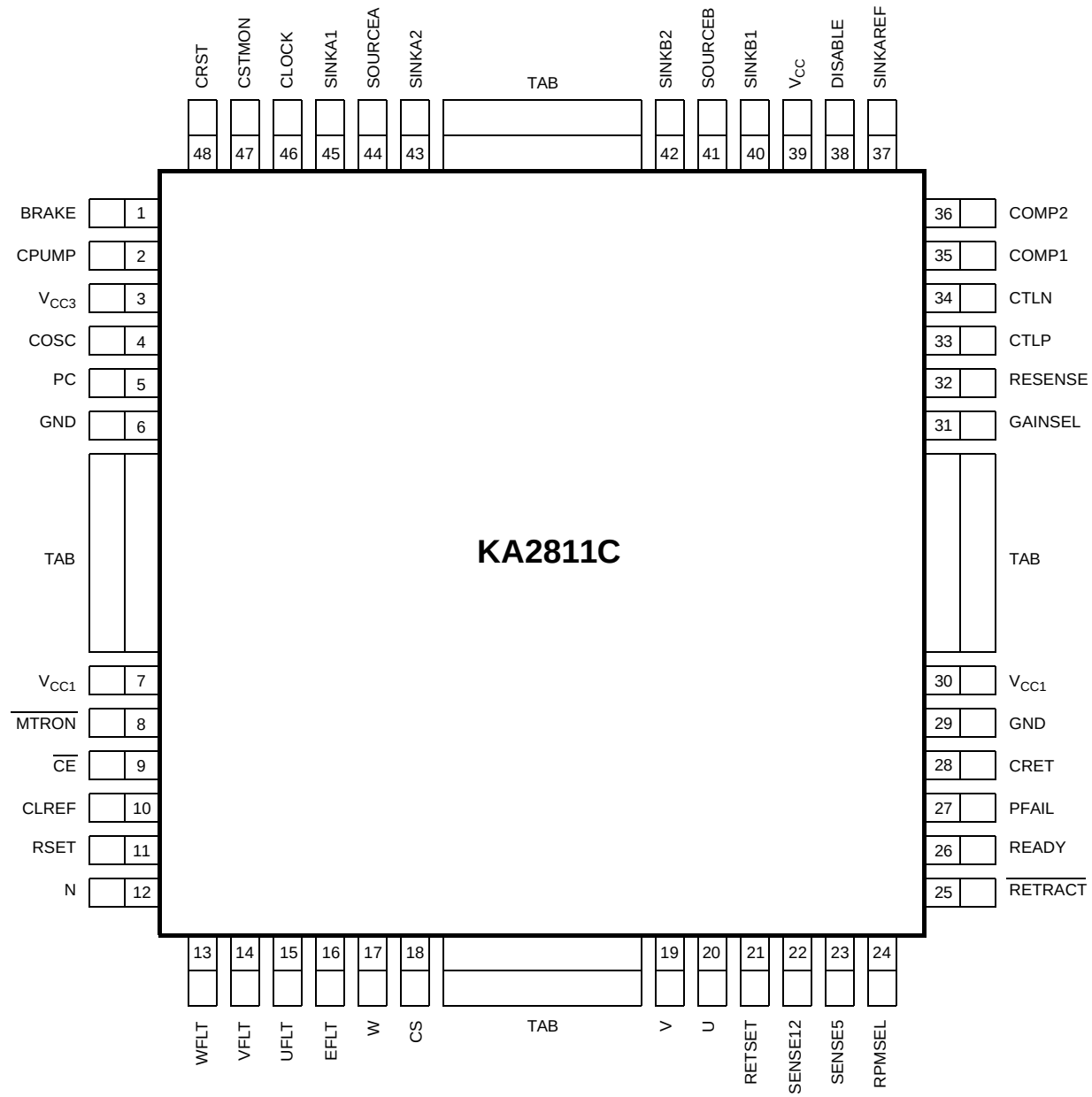
Device	Package	Operating Temperature
KA2811C	48-QFPH-1414	0 ~ 70°C

BLOCK DIAGRAM



PIN CONFIGURATION

48QFPH (48Quad Flat Package Heat-sink)



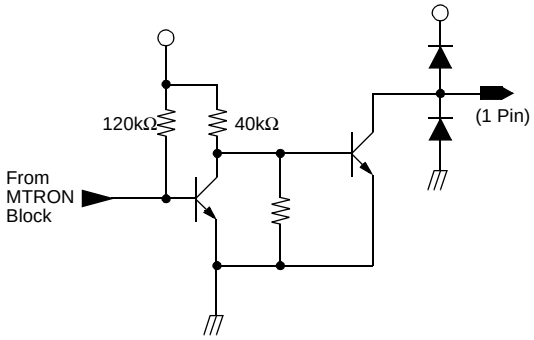
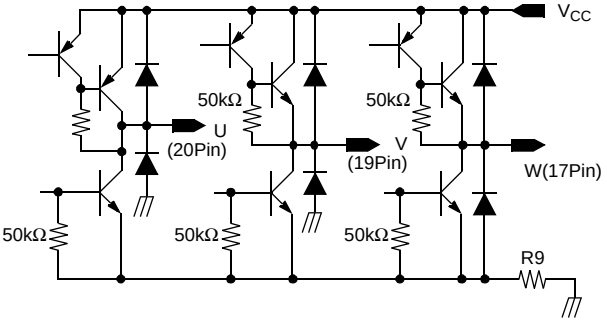
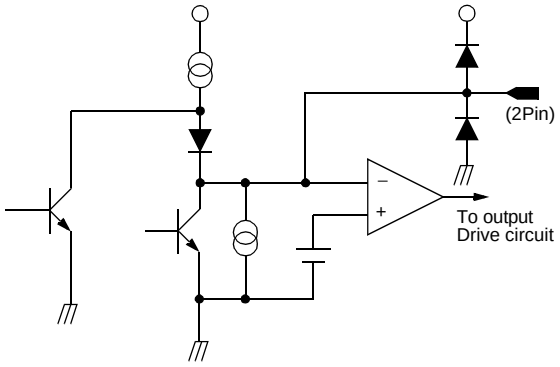
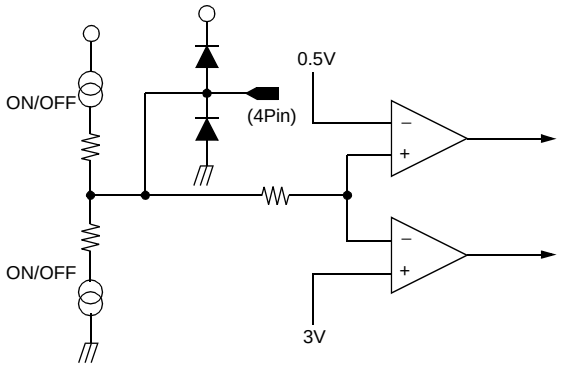
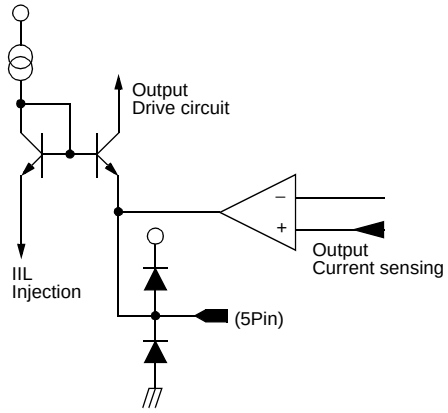
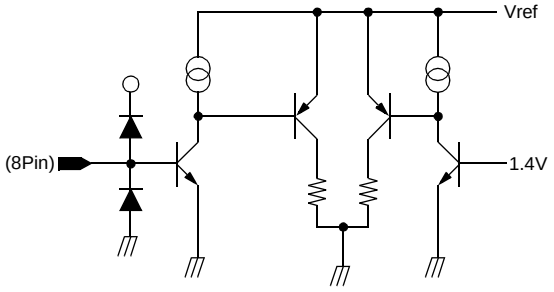
PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	BRAKE	O	Brake output
2	CPUMP	–	Charge pump capacitor
3	$V_{CC3(VDD)}$	–	5V power supply
4	COSC	–	Start-up OSC capacitor
5	PC	–	Phase compensation capacitor
6	GND	–	Ground
7	V_{CC1}	–	12V power supply
8	$\overline{\text{MTRON}}$	I	Motor on & off control input
9	$\overline{\text{CE}}$	I	Chip enable (Active low)
10	CLREF	I	Current limit reference voltage
11	RSET	I	Current & voltage setting resistor
12	N	I	Neutral
13	WFLT	I	Input filter of W-phase signal
14	VFLT	I	Input filter of V-phase signal
15	UFLT	I	Input filter of U-phase signal
16	EFLT	I	Back EMF output filter
17	W	O	W-phase output
18	CS	I	Current sensing resistor
19	V	O	V-phase output
20	U	O	U-phase output
21	RETSET	I	Retract voltage setting resistor
22	SENSE12	I	V_{CC}(12V) power supply sense
23	SEMSE5	I	V_{CC}(5V) power supply sense
24	RPMSEL	I	RPM selection
25	$\overline{\text{RETRACT}}$	I	Retract circuit control input
26	READY	O	Targer RPM locking output signal
27	PFAIL	O	Power fail output
28	CRET	I	Retract power charging capacitor
29	GND	–	Ground
30	V_{CC1}	–	12V power supply
31	GAINSEL	I	VCM gain setting (High, Low)
32	RSENSE	I	Current sensing resistor

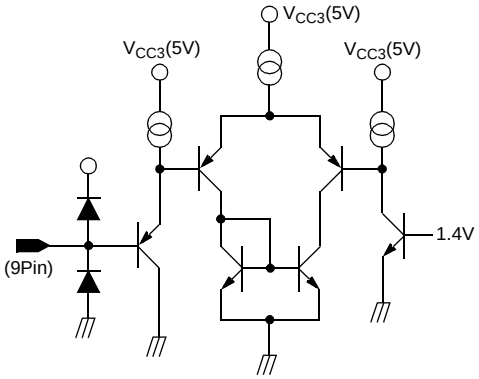
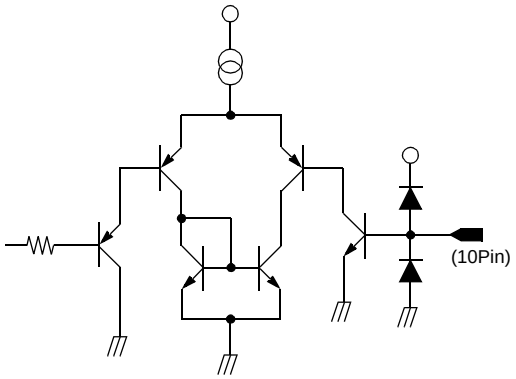
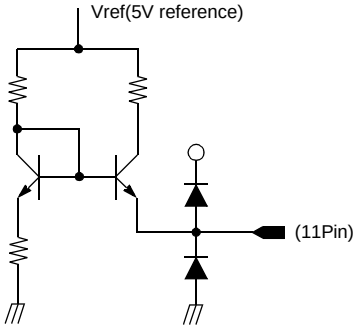
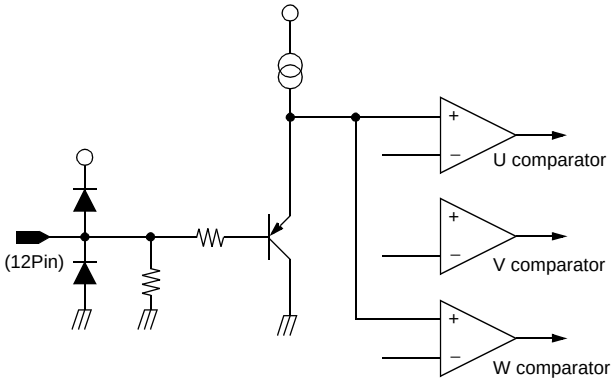
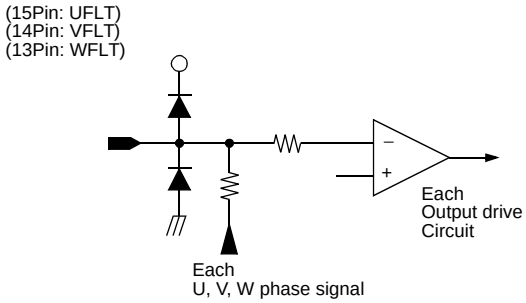
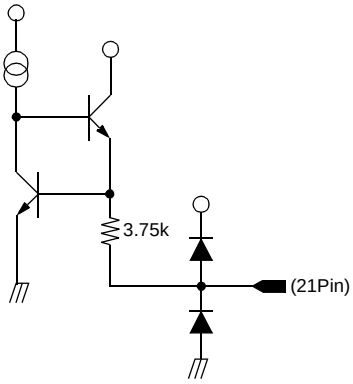
PIN DESCRIPTION (Continued)

Pin No.	Symbol	I/O	Description
33	CTLP	I	VCM amp positive input
34	CTLN	I	VCM amp negative input
35	COMP1	I	Compensation capacitor
36	COMP2	I	Compensation capacitor
37	SINKAREF	I	Kelvin sensing point for VCM amp
38	DISABLE	I	VCM part disable
39	V_{CC2}	–	VCM part power supply (12V)
40	SINKB1	I	External NPN-PNP transistor collector
41	SOURCEB	O	External PNP transistor base
42	SINKB2	O	External NPN transistor base
43	SINKA2	O	External NPN transistor base
44	SOURCEA	O	External PNP transistor base
45	SINKA1	I	External NPN-PNP transistor base
46	CLOCK	I	Reference clock input
47	CSTMON	–	Start-up monitoring
48	CRST	–	VCM amp gain adjustable resistor

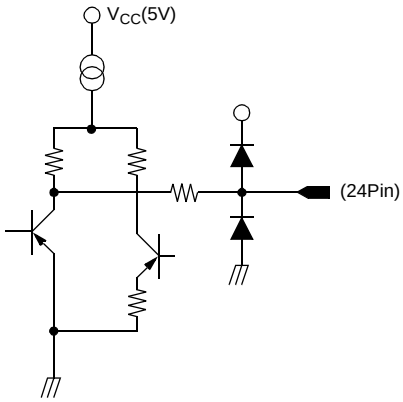
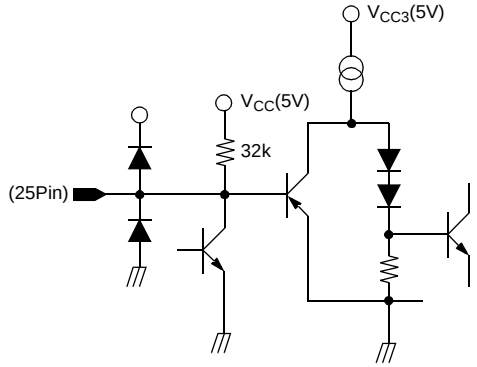
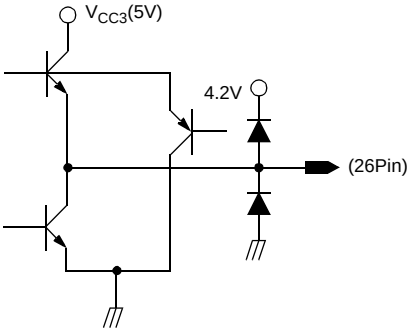
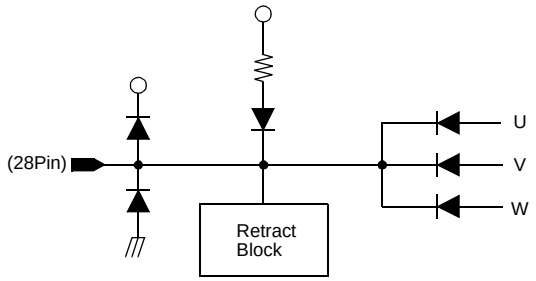
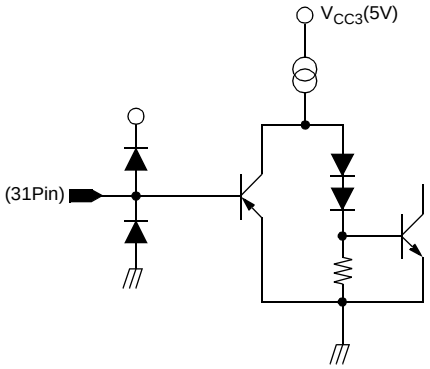
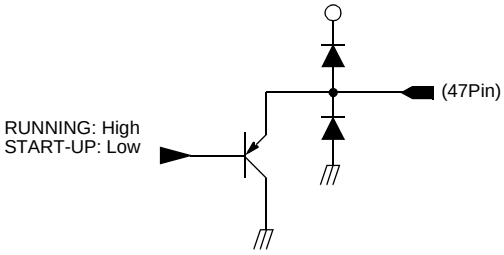
EQUIVALENT CIRCUITS

Brake output	U, V, W drive output
	
Cpump	**Cosc**
	
Pc	**$\overline{\text{Mtron}}$**
	

EQUIVALENT (Continued)

$\overline{CE}$ input	Clref
	
Rset	**N**
	
Uflt, Vflt, Wflt	**Retset**
	

EQUIVALENT (Continued)

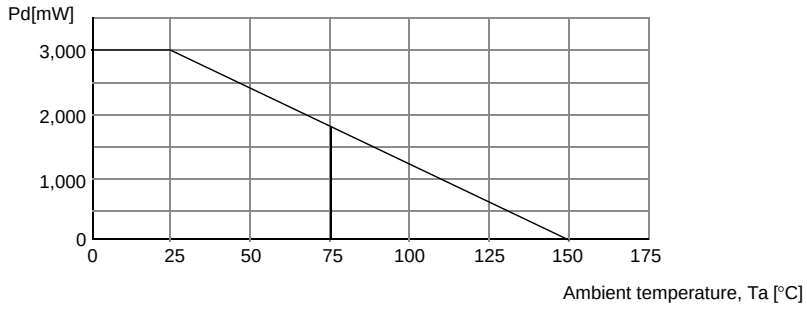
Rpmsel	$\overline{\text{Retract}}$
	
Ready	**Cret**
	
Gainsel	**Cstmon**
	

ABSOLUTE MAXIMUM RATING (Ta=25°C)

Characteristics	Symbol	Value	Unit
Maximum supply voltage	V_{CC1MAX}, V_{CC1MAX}	15.0	V
Maximum logic part supply voltage 2	V_{CC3MAX} (V_{DD})	7.0	V
Power dissipation	P_D	3.0	W
Maximum output drive current	I_{OMAX}	2.0	A
Logic control input voltage	V_{IN}	–3.0 ~ V_{CC3}	V
Operating temperature range	T_{OPR}	0 ~ 70	°C
Soldering temperature (5 seconds, 1/4 inch from pin)	T_{SOLD}	300	°C
Storage temperature range	T_{STG}	–55 ~ 150	°C

NOTES:

1. Absolute maximum ratings are those values beyond which the device may be damaged permanently. Normal operation is not guaranteed at or above those extremes.
2. All voltages are measured with respect to the GND voltage level unless otherwise specified.
3. When mounted on 50mm × 50mm × 1mm PCB (Phenolic resin material).
4. Do not exceed Pd and SOA.



RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{CC1}, V_{CC2}	10.8	12.0	13.2	V
Operating supply voltage in logic part	V_{CC3}	4.5	5.0	5.5	V
Ambient operating temperature range	Ta	0	–	+70	°C

ELECTRICAL CHARACTERISTICS

(Ta=25°C, V_{CC1}, V_{CC2}=12V, V_{CC3}=5V)

Characteristic	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Quiescent current	I_{CC2}	$\overline{CE}$=0V, DISABLE=0V	9	14	19	mA
	I_{CC3}	$\overline{CE}$=5V, DISABLE=5V	2	4.5	7	mA
SPM DRIVE						
$\overline{CE}$ input threshold voltage	V_{CETH}	–	0.8	–	2.0	V
$\overline{CE}$ input high current	I_{CEIH}	$\overline{CE}$=5V	–	–	±100	µA
$\overline{CE}$ input low current	I_{CEIL}	$\overline{CE}$=0V	–	–	±100	µA
$\overline{MTRON}$ input threshold voltage	V_{MOTH}	–	0.8	–	2.0	V
$\overline{MTRON}$ input high current	I_{MIH}	$\overline{MTRON}$=5V	–	–	±100	µA
$\overline{MTRON}$ input low current	I_{MIL}	$\overline{MTRON}$=0V	–	–	±100	µA
Start-up oscillation high threshold voltage	V_{STTHH}	C_{EXT}=0.068µF	2.6	3.0	3.4	V
Start-up oscillation low threshold voltage	V_{STTHL}	C_{EXT}=0.068µF	0.3	0.5	0.7	V
Start-up oscillation frequency	FST	C_{EXT}=0.068µF	100	145	190	Hz
Start-up oscillation high frequency charging current	I_{HIFCHA}	C_{STMON}=0V	–68	–52	–36	µA
Start-up oscillation high frequency discharging current	I_{HIFDCH}	C_{STMON}=0V	32	48	64	µA
Start-up oscillation low frequency charging current	I_{LOFCHA}	C_{STMON}=5V	–	–1.5	–8	µA
Start-up oscillation low frequency discharging current	I_{LOFDCH}	C_{STMON}=5V	36	48	64	µA
Start-up monitor low voltage	V_{SML}	I_O=1mA	–	1	0.4	V
Start-up monitor switching voltage	V_{START}	–	2.0	2.5	3.0	V
Charge pump R1 setup voltage	V_{CP}	R1=10kΩ	0.85	1.0	1.15	V
Charge pump discharge current	I_{CPDCH}	–	20	50	80	µA
Charge pump charging current	I_{CPCHA}	–	–65	–50	–35	µA
Charge pump leakage current	I_{CPLKG}	–	–	–	±1	µA
Ready output high voltage	V_{R1}	I_O=–1.0mA, UFLT=300Hz	3.6	4.2	4.8	V
Ready output high voltage	V_{R2}	I_O=–1.0mA, UFLT=360Hz	3.6	4.2	4.8	V
Ready output low voltage	V_{READY}	–	–	–	0.4	V

ELECTRICAL CHARACTERISTICS (Continued)

(Ta=25°C, V_{CC1}, V_{CC2}=12V, V_{CC3}=5V)

Characteristic	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Output leakage current 1	I_{LKG}	V_{CC}=12.0V (Up U)	–	–	±200	µA
	I_{LEA2}	V_{CC}=12.0V (Up V)	–	–	±200	µA
	I_{LEA3}	V_{CC}=12.0V (Up W)	–	–	±200	µA
	I_{LEA11}	V_{CC}=12.0V (Low U)	–	–	±200	µA
	I_{LEA12}	V_{CC}=12.0V (Low V)	–	–	±200	µA
	I_{LEA13}	V_{CC}=12.0V (Low W)	–	–	±200	µA
Output saturation voltage	V_{SAT} (U, V, W)	I_O=100mA	–	–	0.8	V
		I_O=300mA	–	–	1.2	V
		I_O=500mA	–	–	1.5	V
		I_O=1A	–	–	2.0	V
		I_O=1.5mA	–	–	3.0	V
RPMSEL input low current	I_{RPML}	RPMSEL=0V	–80	–45	–10	µA
RPMSEL input high current	I_{RPMH}	RPMSEL=5V	10	40	70	µA
Brake output low voltage	V_{BRK}	I_O=0.5mA	–	–	0.4	V
Low voltage inhibit	V_{LVI}	–	6	–	8	V
VCM DRIVE						
Offset current	I_{OFF}	RSENSE=1Ω	–9	–	9	mA
1/4 gain	G1/4	GAINSEL=2V	227	250	278	mA/V
1/16 gain	G1/16	GAINSEL=0.8V	53	63	73	mA/V
Sinking saturation 11 voltage	V_{NSAT11}	I_O=100mA	–	0.3	–	V
Sinking saturation 12 voltage	V_{NSAT12}	I_O=300mA	–	0.4	–	V
Sinking saturation 13 voltage	V_{NSAT13}	I_O=500mA	–	0.5	–	V
Sinking saturation 21 voltage	V_{NSAT21}	I_O=100mA	–	0.3	–	V
Sinking saturation 22 voltage	V_{NSAT22}	I_O=300mA	–	0.4	–	V
Sinking saturation 23 voltage	V_{NSAT23}	I_O=500mA	–	0.5	–	V
Sourcing saturation 11 voltage	V_{PSAT11}	I_O=100mA	–	0.3	–	V
Sourcing saturation 12 voltage	V_{PSAT12}	I_O=300mA	–	0.4	–	V
Sourcing saturation 13 voltage	V_{PSAT13}	I_O=500mA	–	0.5	–	V
Sourcing saturation 21 voltage	V_{PSAT21}	I_O=100mA	–	0.3	–	V
Sourcing saturation 22 voltage	V_{PSAT22}	I_O=300mA	–	0.4	–	V
Sourcing saturation 23 voltage	V_{PSAT23}	I_O=500mA	–	0.5	–	V
SOURCEA base drive current	I_{SOAB}	–	20	–	–	mA
SOURCEB base drive current	I_{SOBB}	–	20	–	–	mA

ELECTRICAL CHARACTERISTICS (Continued)

(Ta=25°C, V_{CC1}, V_{CC2}=12V, V_{CC3}=5V

Characteristic	Symbol	Test conditions	Min.	Typ.	Max.	Unit
SINK2 base drive current	I_{SIAB}	–	20	–	–	mA
SINKB2 base dirve current	I_{SIBB}	–	20	–	–	mA
RETSET voltage	V_{RETSET}	–	0.5	0.75	0.95	V
SOURCE voltage	V_{SRC}	C_{RET}=3V	1.0	1.6	2.2	V
$\overline{\text{SINK}}$ current	I_{SIN}	SINKB1=0.5V	36	48	60	–
RETRACT output low voltage	V_{RETOUT}	I_{SINKB1}=1mA	–	–	0.4	mA
12V threshold voltage	V_{TH2}	–	9.0	10	11	V
12V hysteresis voltage	V_{HYS12}	–	–	150	–	mV
5V threshold voltage	V_{TH5}	–	1.2	4.6	4.85	V
5V hysteresis voltage	V_{HYS5}	–	–	75	–	mV
Power fail output low voltage	V_{OPF}	–	–	–	0.4	V
GAINSEL high input voltage	V_{IHGAIN}	–	2.0	–	–	V
$\overline{\text{DISABLE}}$ high input voltage	V_{IHDIS}	–	2.0	–	–	V
RETRACT high input voltage	V_{IHRET}	–	2.0	–	–	V
$\overline{\text{GAINSEL}}$ low input voltage	V_{ILGAIN}	–	–	–	0.8	V
DISABLE low input voltage	V_{ILDIS}	–	–	–	0.8	V
RETRACT low input voltage	V_{ILRET}	–	–	–	0.8	V
DISABLE high input current	I_{IHDIS}	V_{IN}=5V	–	10	40	µA
$\overline{\text{GAINSEL}}$ high input current	I_{IHGAIN}	V_{IN}=5V	–	–	±10	µA
RETRACT high input current	I_{IHRET}	V_{IN}=5V	–	–	±10	µA
DISABLE low input current	I_{ILDIS}	V_{IN}=0V	–	–	±10	µA
GAINSEL low input current	I_{ILGAIN}	V_{IN}=0V	–40	–10	–	µA
RETRACT low input current	I_{ILRET}	V_{IN}=0V	–250	–160	–	µA

APPLICATION INFORMATION

1. SPM RART

1. Bias

The rart biases the spindle block and is configured of a bandgap circuit as illustrated in figure 1 below.

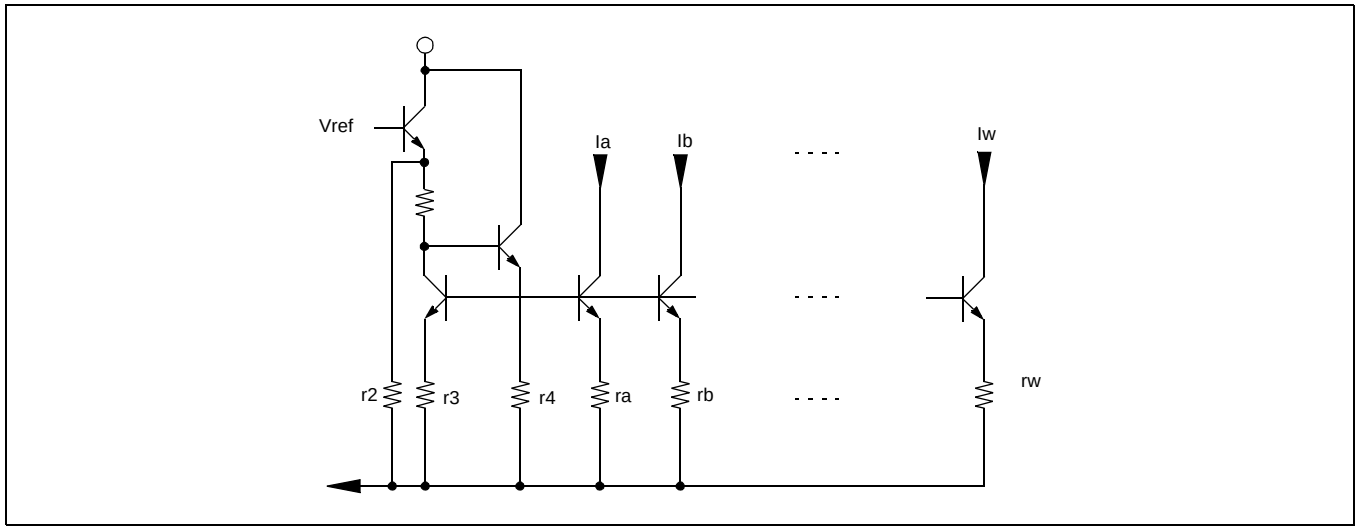


Figure 1. Bias block internal circuit

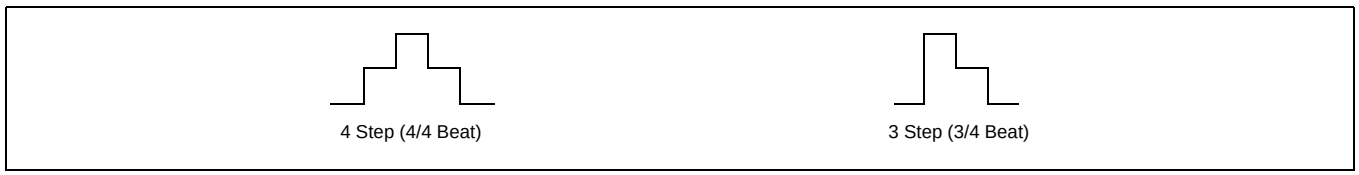
Where r3 = ra = rb ..... = rw.

Pin no.9 (CE) is capable to enable or disable the spindle block.

2. Start-up

It is the block that concerns initial drive of the spindle motor. The Waltz Step start (WSS) method has been applied to obtain high torque.

The WSS starts the 3-phase spindle motor in 3 steps just like a waltzing rhythm rather than the 4 step fashion as shown below.



The start-up is effected by driving output stage of the block with the sliding COSC clock and setting the signals of $\overline{CE}$ and $\overline{MTRON}$ at the low state (See the start-up timing chart).

When the spindle motor is in start-up mode, the voltage at pin no. 47 should measure 1.4V and that of the running mode 2.5V. The equations below represent the timing of each mode.

Transition time from start-up high frequency to low frequency:

$$\text{Vpin no. 47} \ (\cong 1.4V) \ = \ 5V \times \left(1 - e^{-\frac{t}{\tau}}\right)$$

$$t \ = \ \tau \ \text{In} \ (3.6/5)$$

Delay time from the start-up start-up to running modes:

$$\text{Vpin no. 47} \ (\cong 2.5V) \ = \ 5V \times \left(1 - e^{-\frac{t}{\tau}}\right)$$

$$t \ = \ -\tau \ \text{In} \ 0.5$$

3. BEMF detector

The block detects the signals to $\overline{\text{CE}}$ and $\overline{\text{MTRON}}$ to determine BEMF (Back Electromotive force) generation in sufficient level required to maintain self-commutation of the spindle motor. The block is configured of BEMF amplifier and voltage detector circuits.

4. Zero cross detector

The block controls the rotating speed of the spindle motor with the output obtained from the comparator process which compare the U phase voltage among U, V, W phase voltages that are the actual elements of BEMF of the motor with the natural voltage of the motor.

5. RPM selector

The selection mode at the pin no. 24 and the clock at the Pin no. 48 enables to run the motor at specific RPM within the range of 3600/4500/5400 as follows

Pin no. 24 (RPMSEL)	Pin no. 46 (CLOCK)	Target rpem	Remark
Low (0V)	4MHz	3600	–
	5MHz	4500	–
	6MHz	5400	–
High (5V)	5MHz	5400	–
Open	–	–	Not use

6. Speed control

It compares input reference clock with the output phase of zero cross detector which is proportional to motor speed by means of PLL (Phase lock loop) circuit.

After that, it provides the data of speed error to the F/V block as pulse.

RPM of Motor

$$N_O = \frac{fck \times 60 \times D1}{Ncnt \times P_O \times D2}$$

Here,
N_O = RPM
fck = Reference clock (Pin no. 46),
D1 = Divided clock ratio,
D2 = Divided zero cross signal ratio,
P_O = Motor pair pole (8 pole motor: $P_O = 4$)
Ncnt = PLL counted value
Pin 24 = 0V $\rightarrow$ Ncnt = 2084
Pin 24 = 5V $\rightarrow$ Ncnt = 1736

ex)

$$fck = 5MHz, \text{ Pin no. } 24 = 5\text{V, Mode (Ncnt = 1736)}$$
$$N_O = \frac{fck}{Ncnt} \times 1.875 = 5400.346rpm \cong 5400rpm$$

Speed error (%)

$$RPMerror = \frac{I_{HOLD}}{Ncnt} \times 100$$
$$= I_{HOLD} \times (R10 + R11) \times 100$$

Here, I_{HOLD} = Leakage current (Pin no. 2)

ex) At the KA2811C

RPMerror = 100μA × 10kΩ × 100 = 0.1%

7. F/V converter

The block converts the digital output signals from the speed control block into DC voltages and then feeds the voltages to buffer amplifier.

8. Control amp

It compensates the total gain and phase of SPM part.

It operates sense amp during starting-up, and incorporates output voltage and feedback loop by F/V input during running.

9. Sense amp

It determines maximum output current during the start-up.

10. Ready

It generates high output when motor speed reaches target RPM.

11. Brake

While the spindle motor is in rotation at the target RPM.

The signal voltage at the pin no. 1 becomes set to the low state that the brake function is not activated.
If however, the power is turned off or the chip is disabled, the internal circuit of the pin no. 1 will be opened.
In this way, the voltage at the capacitor C4 will be discharged through the resistor R4 and triggers the dual MOSFET turned on.

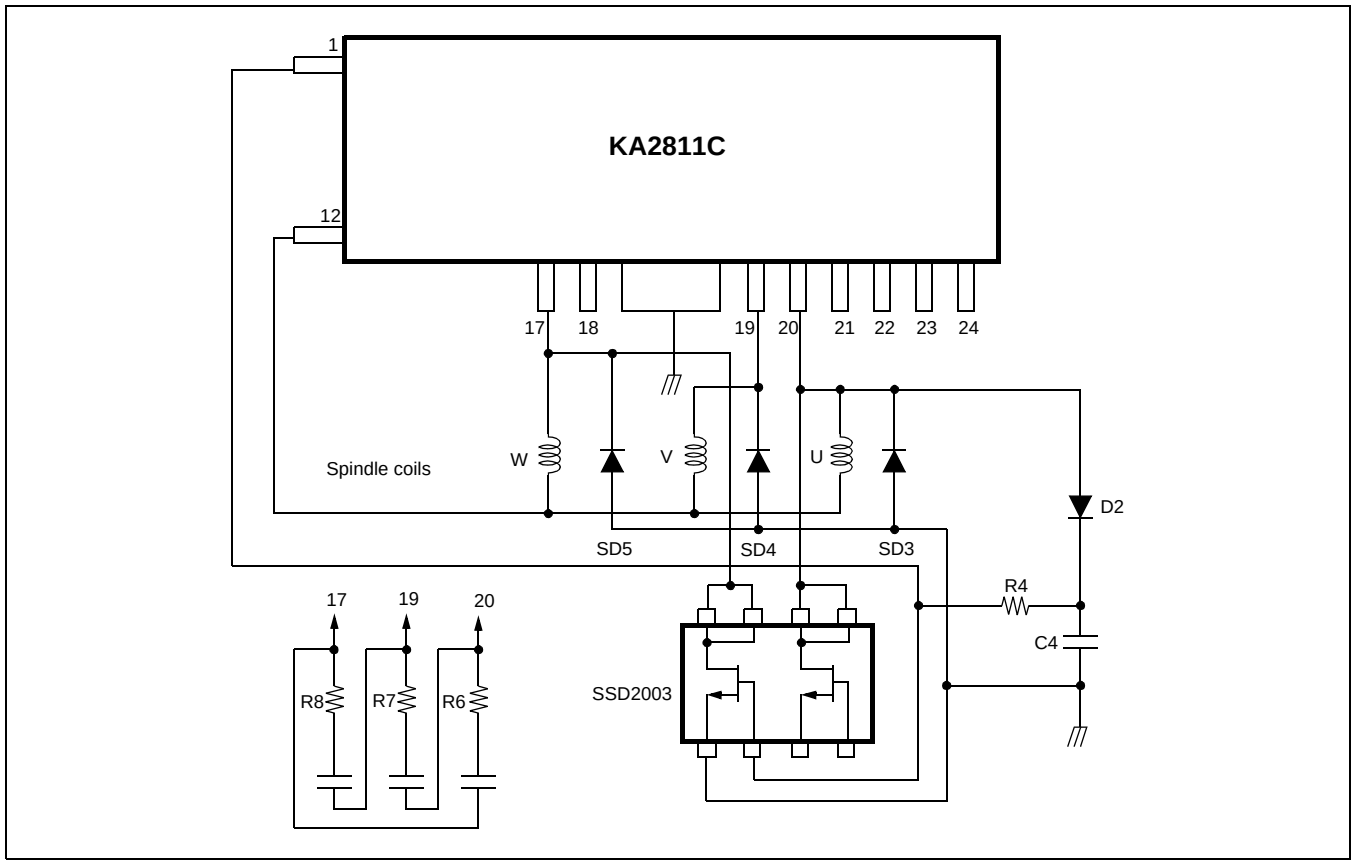


Figure 2. Brake circuit

12. Protector

UVLO (Under voltage lockout)
The protector shuts down internal bias by the function of UVLO when the power supply voltage falls below 6V (min).

TSD (Thermal shutdown)

It shuts down the driver in case the chip temperature should rise upto 150°C by the function of thermal shutdown (TSD) circuitry.

2. VCM PART

1. Current Amplifier

Current amplifier is designed to be capable of gain adjustment with use of six external resistors.

The design is implemented in a configuration that ensures minimum crossover distortion characteristics.

As for the power transistors, for instance, it externally employs dual transistors of NPN & PNP types of Imax = 3A current rating in order to minimize IC loss and maximize output driving capability.
(Dual NPN: SSD1001, Dual PNP: SSD1002)

2. Retract

The power supply for this block is obtained by the spindle motor BEMF after having filtered by 3 diodes self-contained and the capacitor C3 of the pin no. 28(CRET).

Retract function is performed when the “Low” applied to the input (Pin no. 25) turns the pin no. 40 (SINKB1) to “Low” state and sets the bias voltage of pin no. 32 (RSENSE) as expressed below:

$$Vpin32[V] = \frac{0.7[V]}{3.75[k\Omega] + R5[k\Omega]} \times 3 \times 3.75[k\Omega]$$

It is obvious that the current running in VCM during the retraction is determined by the resistor R5.

3. DISABLE

It choose enable or disable of VCM part.

4 GAINSEL

The function selects the gain mode.

When the input to pin no. 31 (GAINSEL) is at high state, it becomes high gain mode, and if low, it becomes low gain mode.

Gain selectio method

$$High \text{ gain (Pin31 = 5V)} = \frac{R2P + RFP}{R!P}$$

$$Low \text{ gain (Pin32 = 0V)} = \frac{RFP}{R1P + R2P}$$

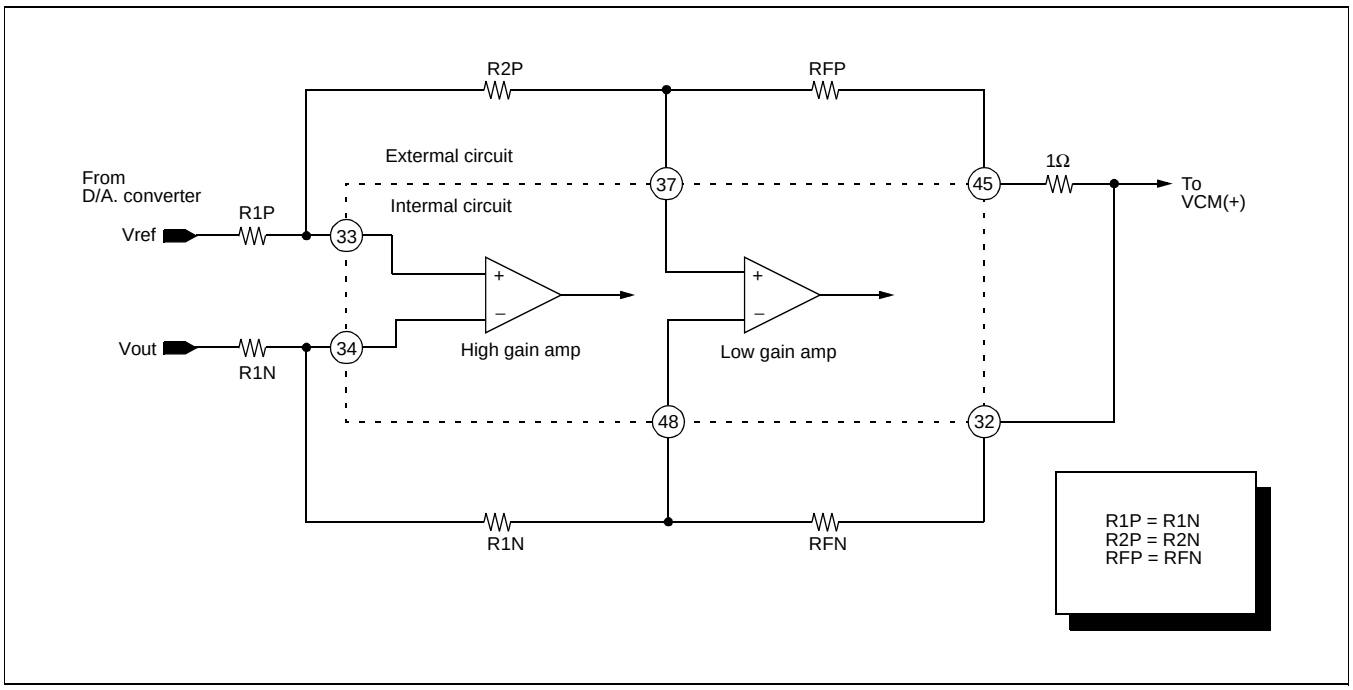


Figure 3. VCM gain amp circuit

5. Power Fail Detector

It checks the power of 12V and 5V.

The bandgap reference circuit is used to maintain internal reference voltage.

Assume in Fig.4 that the bandgap reference voltage is 1.5V and the normal voltage level of $V_{CC}1$ & 2 (12V) or $V_{CC}3$ (5V) is decreased.

In case the voltage at any one side of pins no. 22 and no. 23 drops down to 1.5V level, the comparator output (PFAIL) then turns to low from high which is normal running state.

In this workouts, the voltages of $V_{CC}1$ & 2 and $V_{CC}3$ will be obtained by the following expressions:

$$V_{CC}1,2 = Vpin\ \text{no. } 22 \times \frac{R1 + R2}{R2}$$

$$= 1.5[V] \times \frac{12.75[k\Omega] + 2.25[k\Omega]}{2.25[k\Omega]}$$

$$= 9.999[V]\ \text{or less}$$

$$V_{CC}3 = Vpin\ \text{no. } 23 \times \frac{R3 + R4}{R4}$$

$$= 1.5[V] \times \frac{3.075[k\Omega] + 1.5[k\Omega]}{1.5[k\Omega]}$$

$$= 4.757[V]\ \text{or less}$$

Hysteresis: $V_{CC}1, 2 = 90mV$ (Typ)
$V_{CC}3 = 45mV$ (Typ)

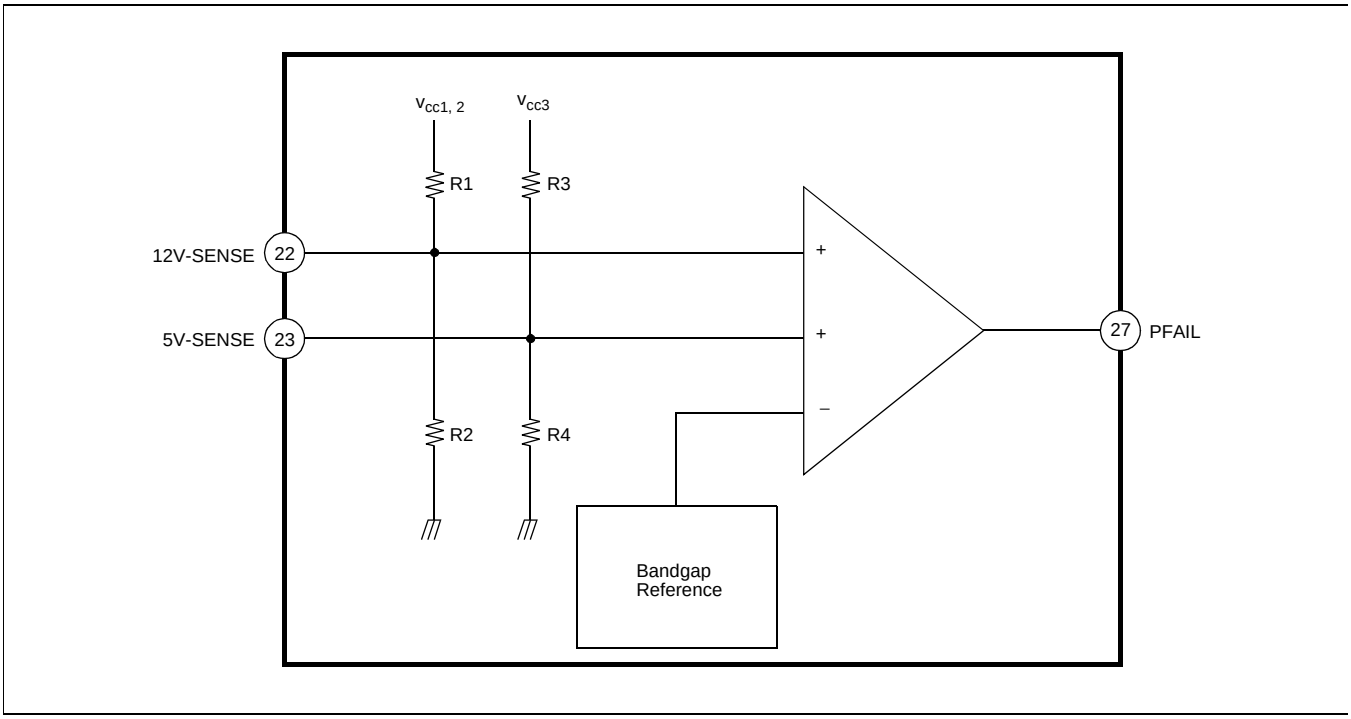
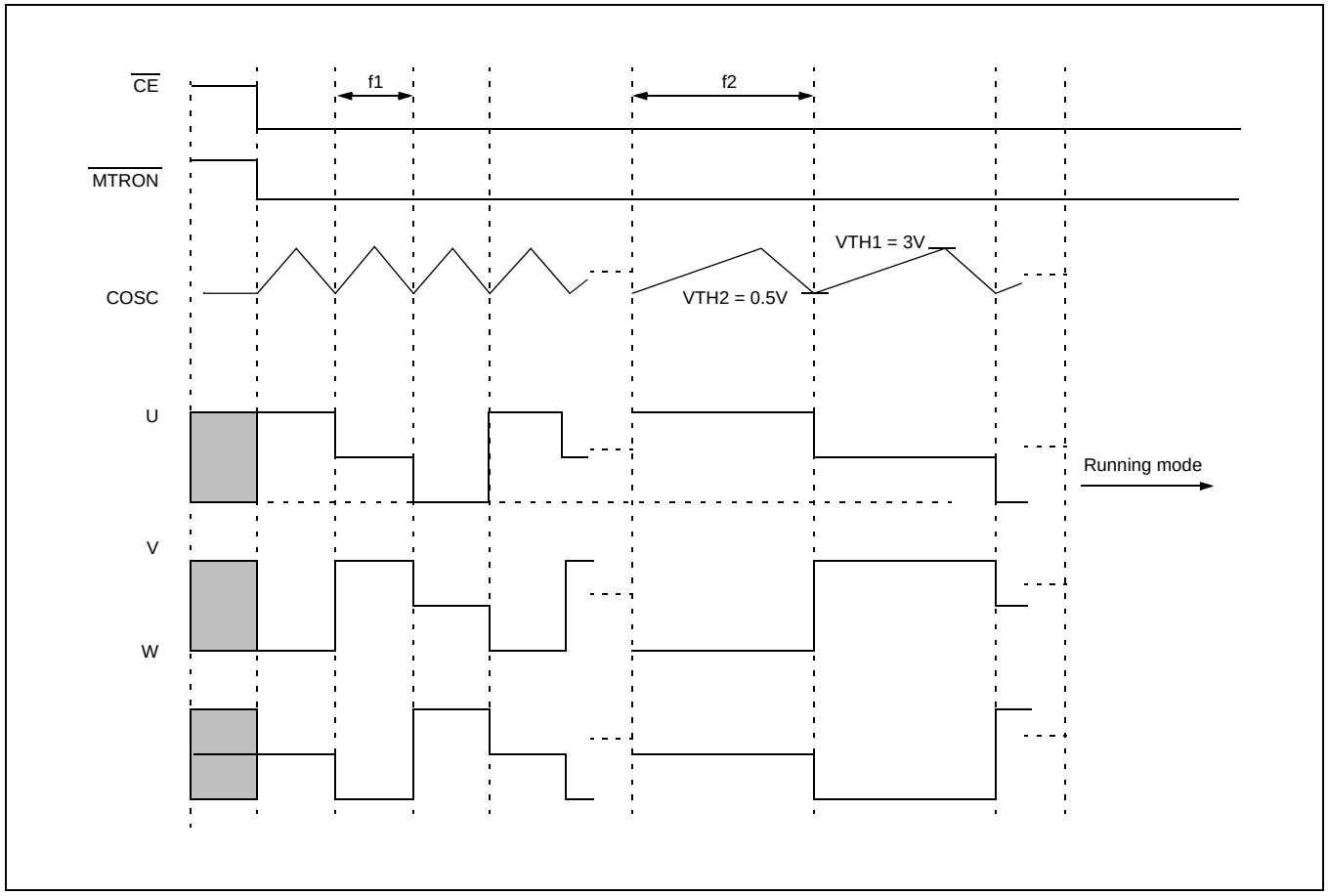


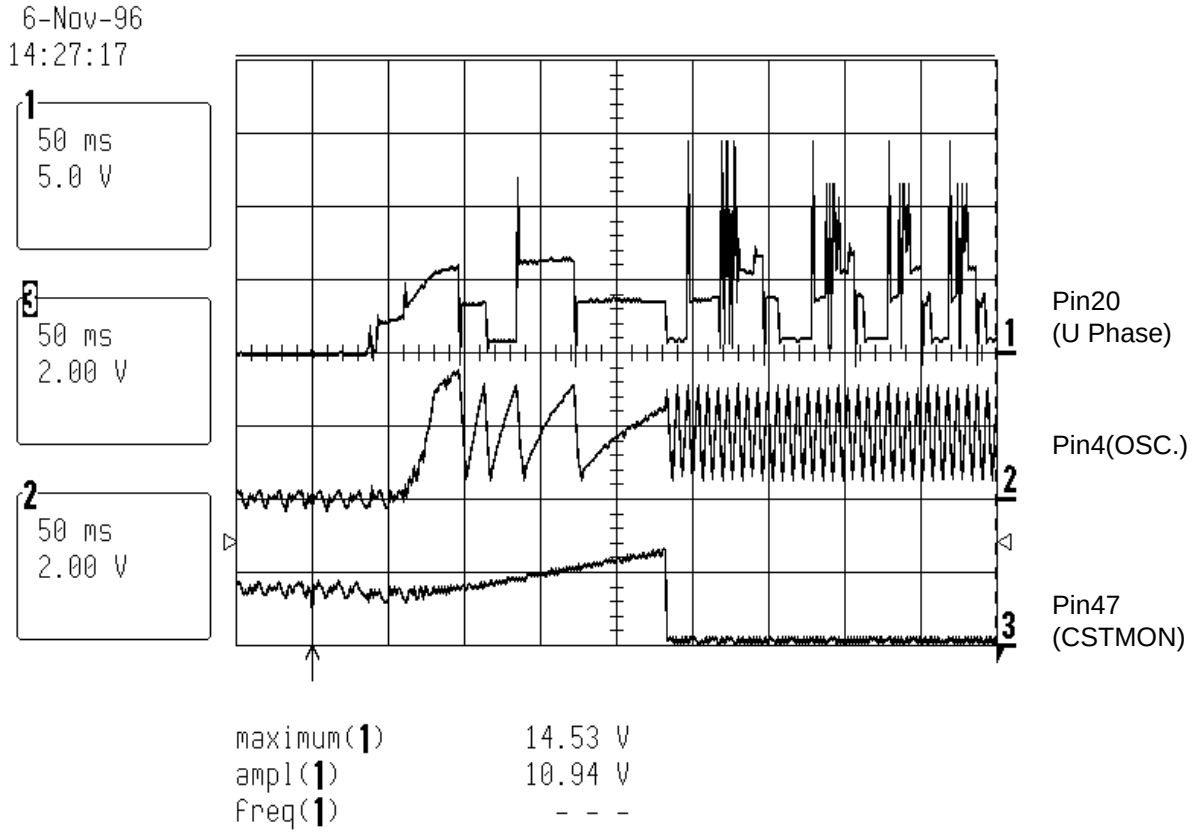
Figure 4. Power fail circuit

TIMMING CHART

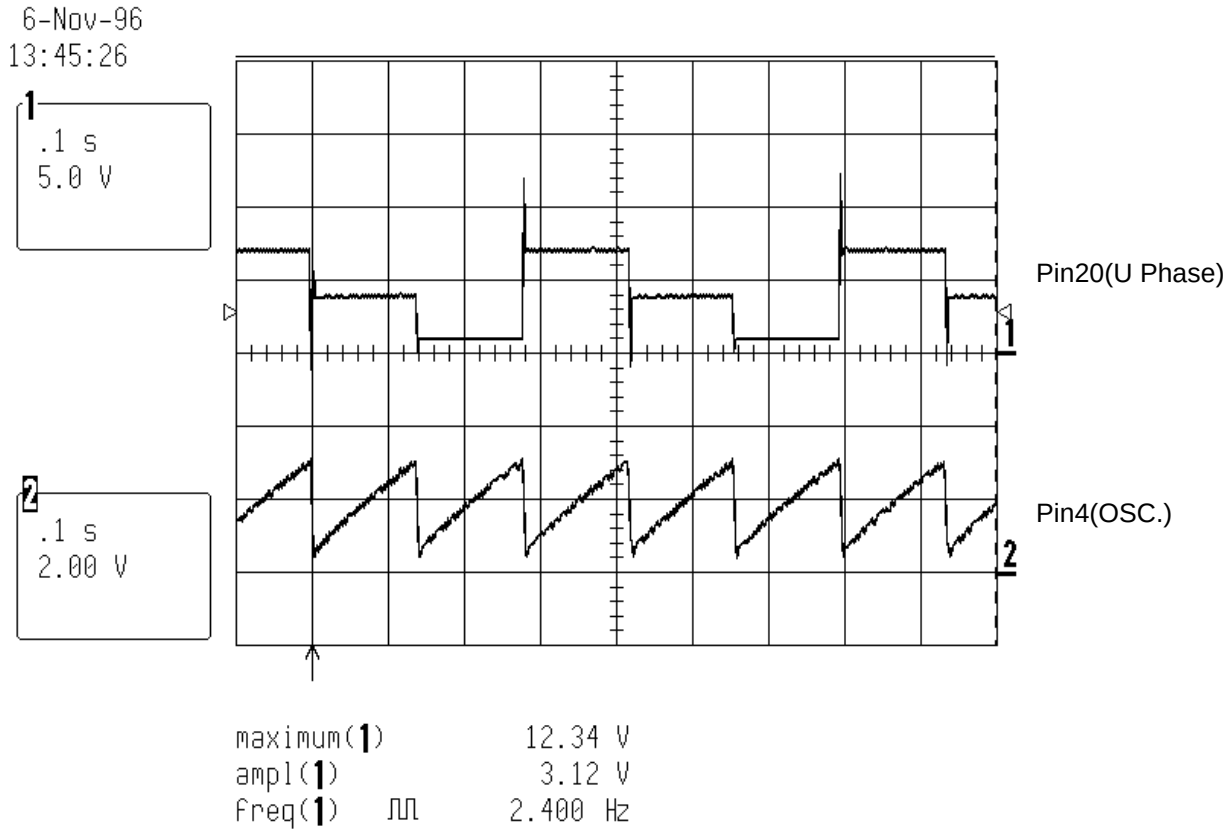
Start-up



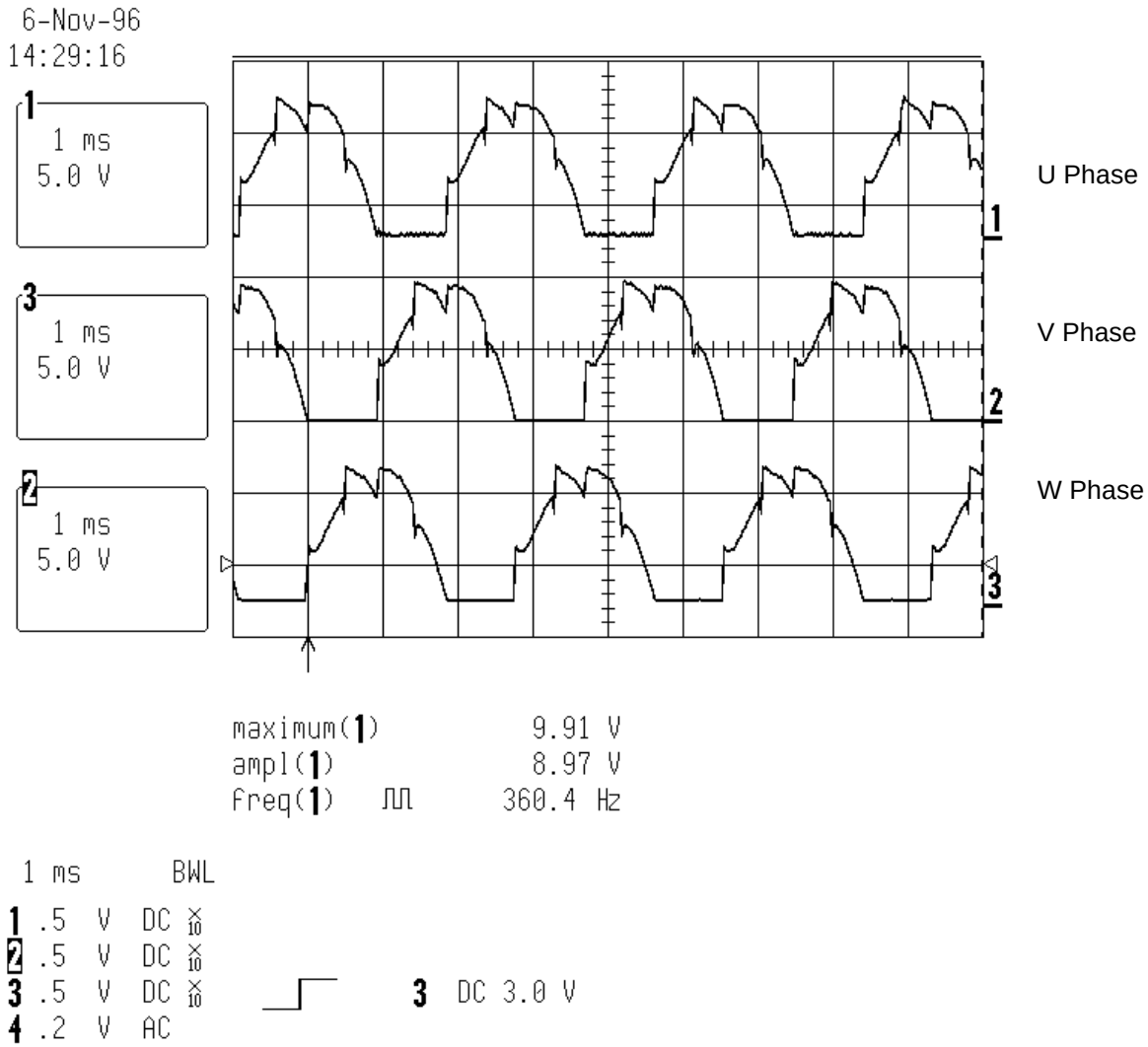
FROM START-UP MODE TO RUNNING MODE WAVEFORM



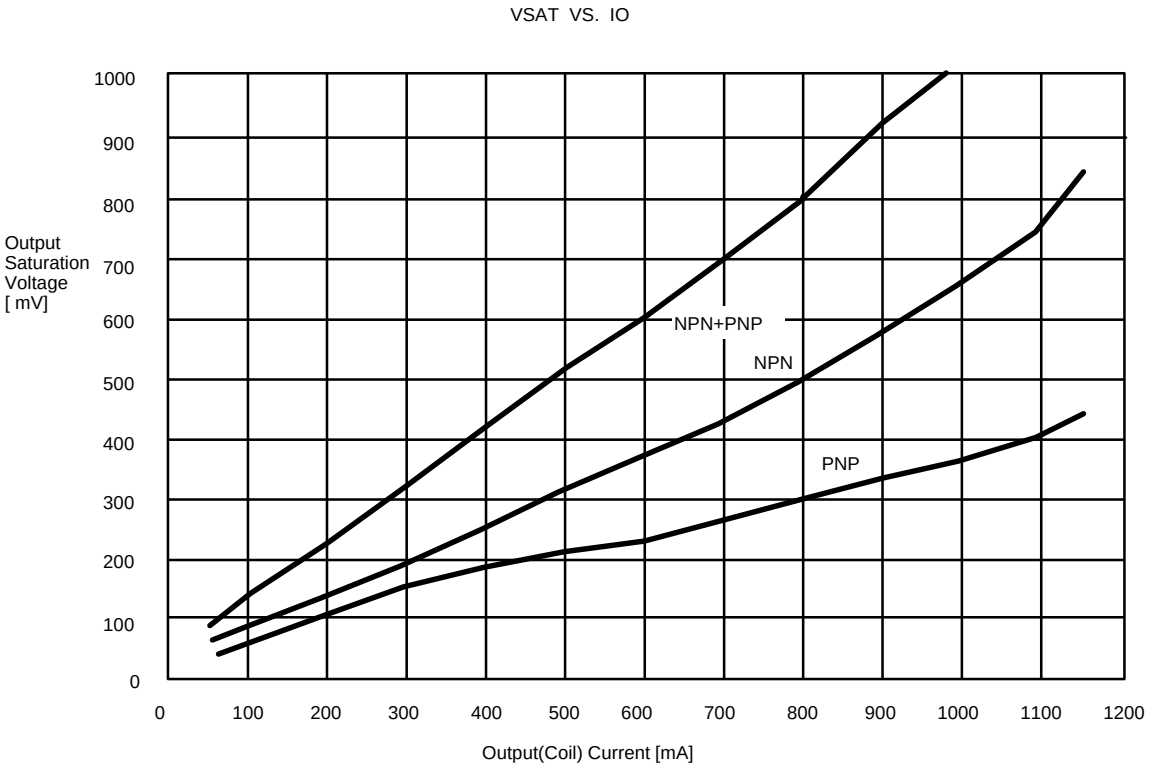
SYNCHRONOUS DRIVING WAVEFORM (START-UP MODE)



RUNNING MODE WAVEFORM

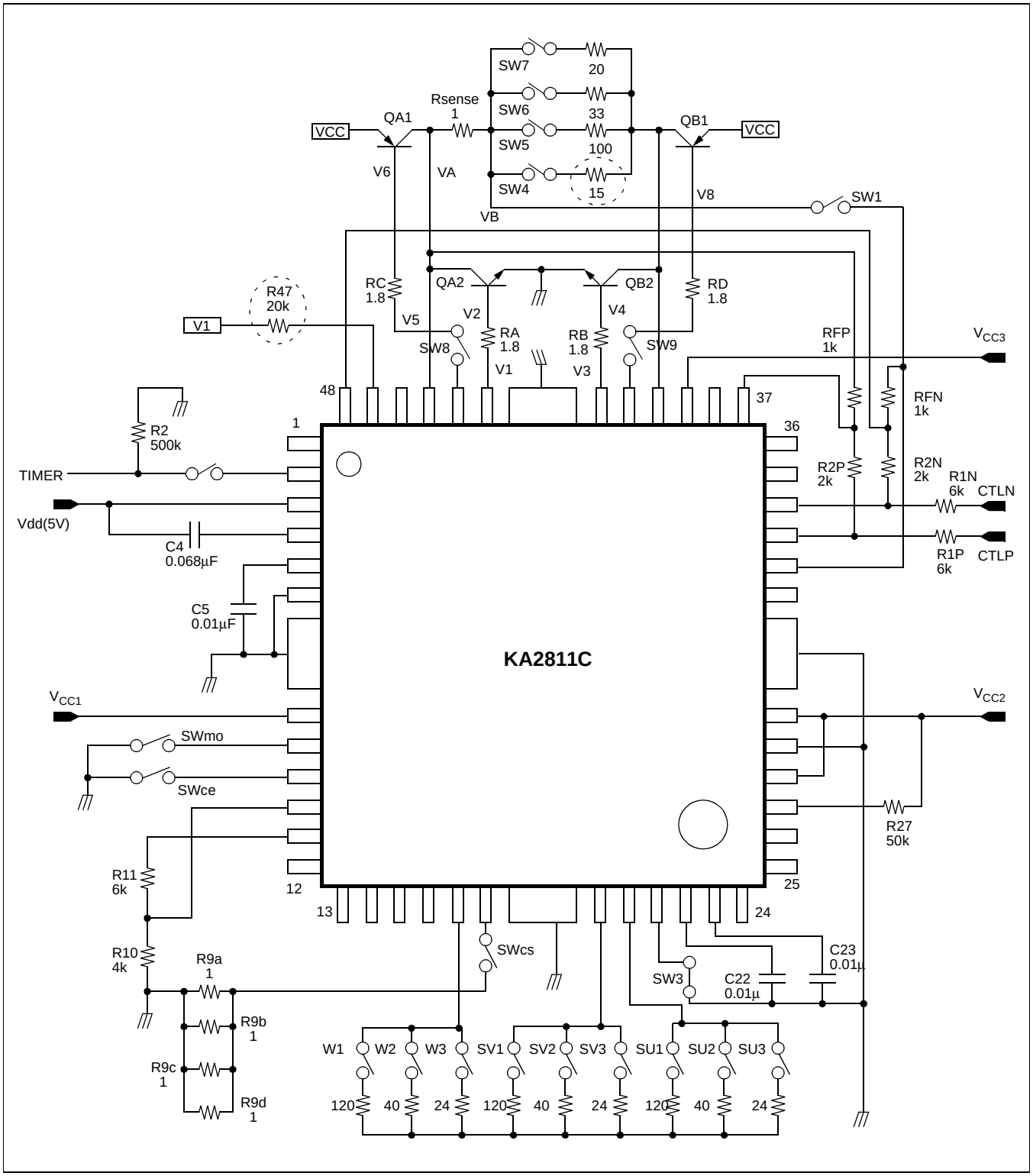


GRAPH

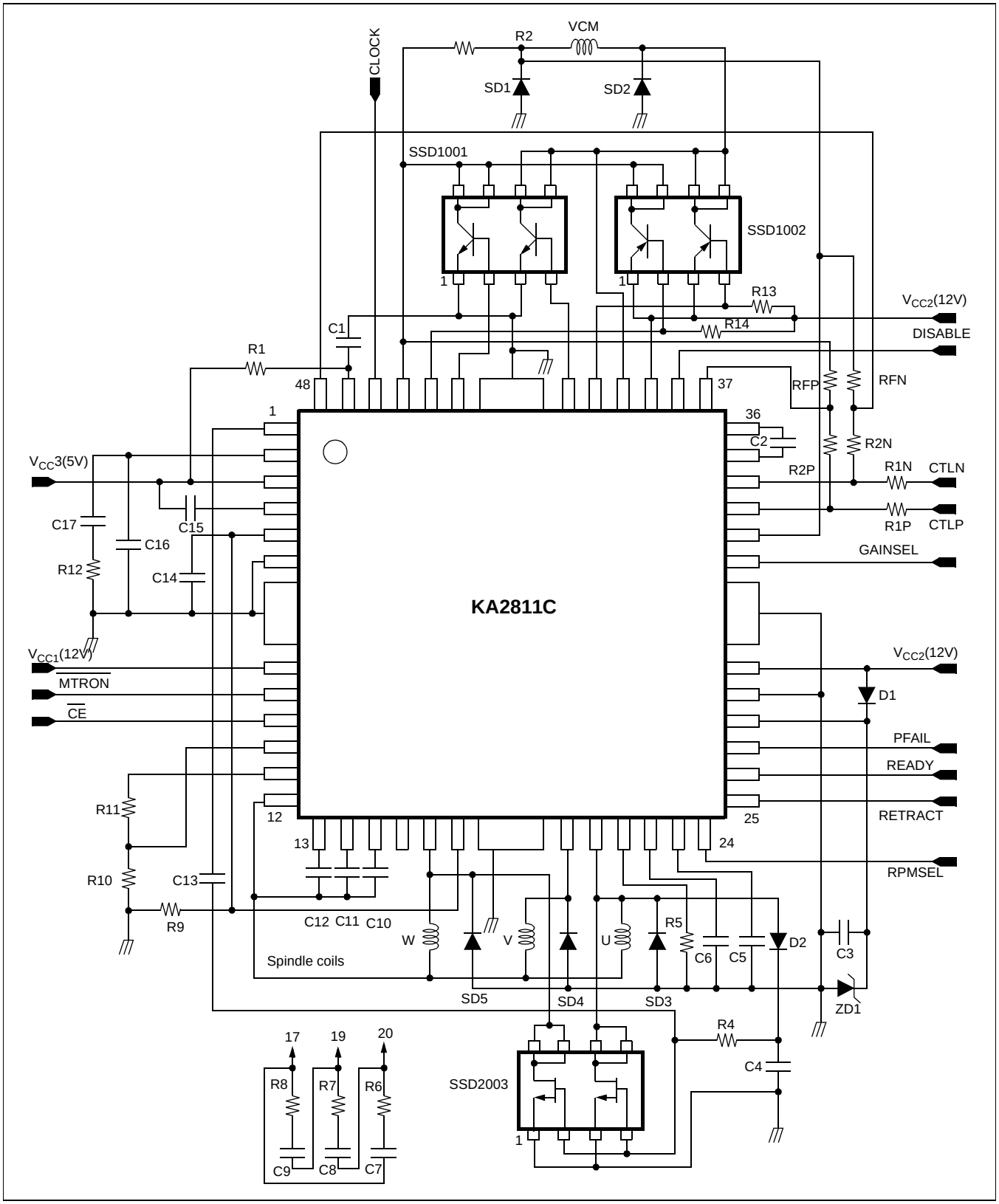


VCM Output Saturation Voltage vs. VCM Output Current
(NPN TRs = SSD1001, PNP TRs =SSD1002)

TEST CIRCUIT



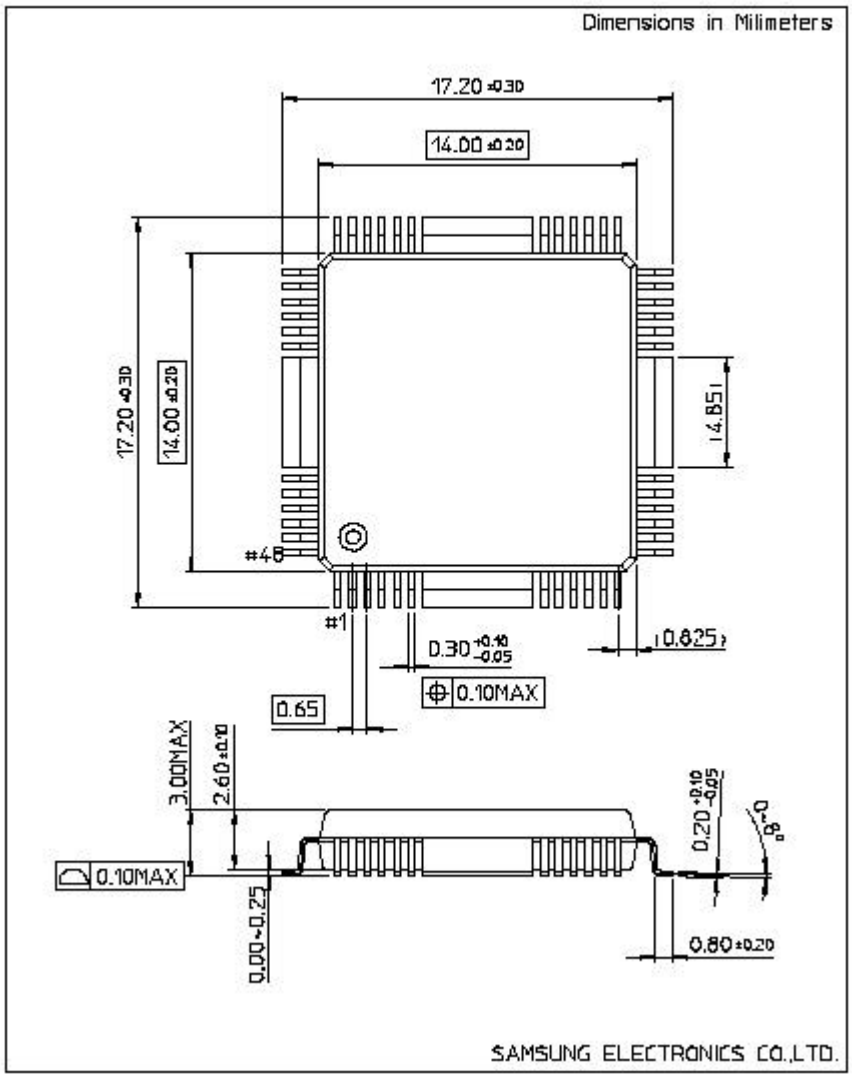
APPLICATION CIRCUIT



NOTE: Break down voltage of ZD1 < maximum supply voltage (15V).

PACKAGE DIMENSION

48-QFPH-1414



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