

## 6-CH MOTOR DRIVER

The KA3031 is a monolithic integrated circuit suitable for a 6-ch motor driver which drives the tracking actuator, focus actuator, sled motor, tray motor, change motor and spindle motor of the CDP/CAR-CD systems.



## FEATURES

- 4-CH balanced transformerless (BTL) driver
- 2-CH (forward-reverse) control DC motor driver
- Operating supply voltage (4.5V ~ 16V)
- Built-in thermal shut down circuit (TSD)
- Built-in under voltage lockout circuit (UVLO)
- Built-in over voltage protection circuit (OVP)
- Built-in mute circuit (CH1, CH2, CH3 and CH4)
- Built-in normal op-amp
- Built-in 5V regulator with reset

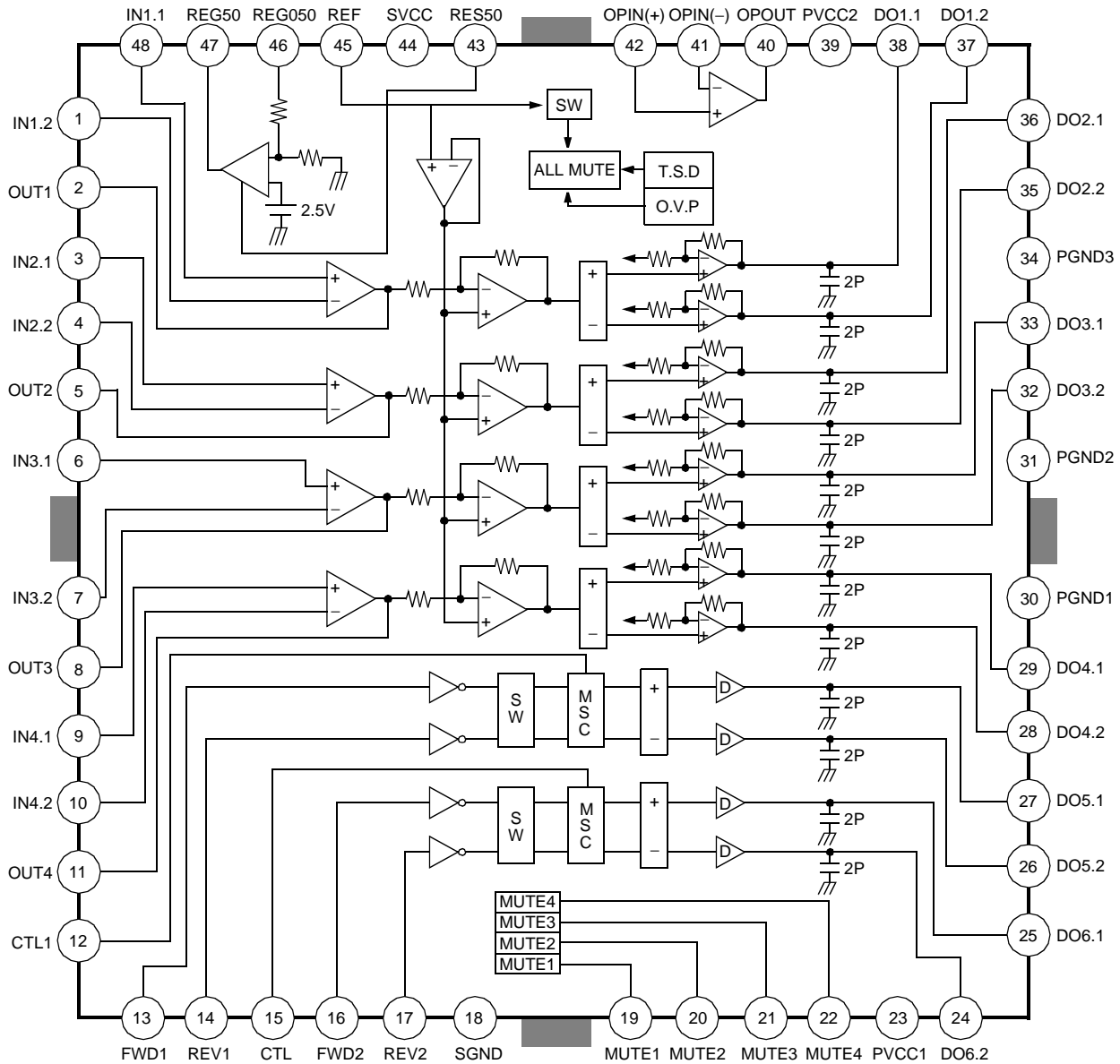
## ORDERING INFORMATION

Device	Package	Operating Temperature
KA3031	48-QFPH-1414	-35°C ~ +85°C

## TARGET APPLICATIONS

- CD-PLAYER (TRAY, CHANGE)
- VIDEO-CD (TRAY, CHANGE)
- CAR CD-PLAYER (TRAY, CHANGE)

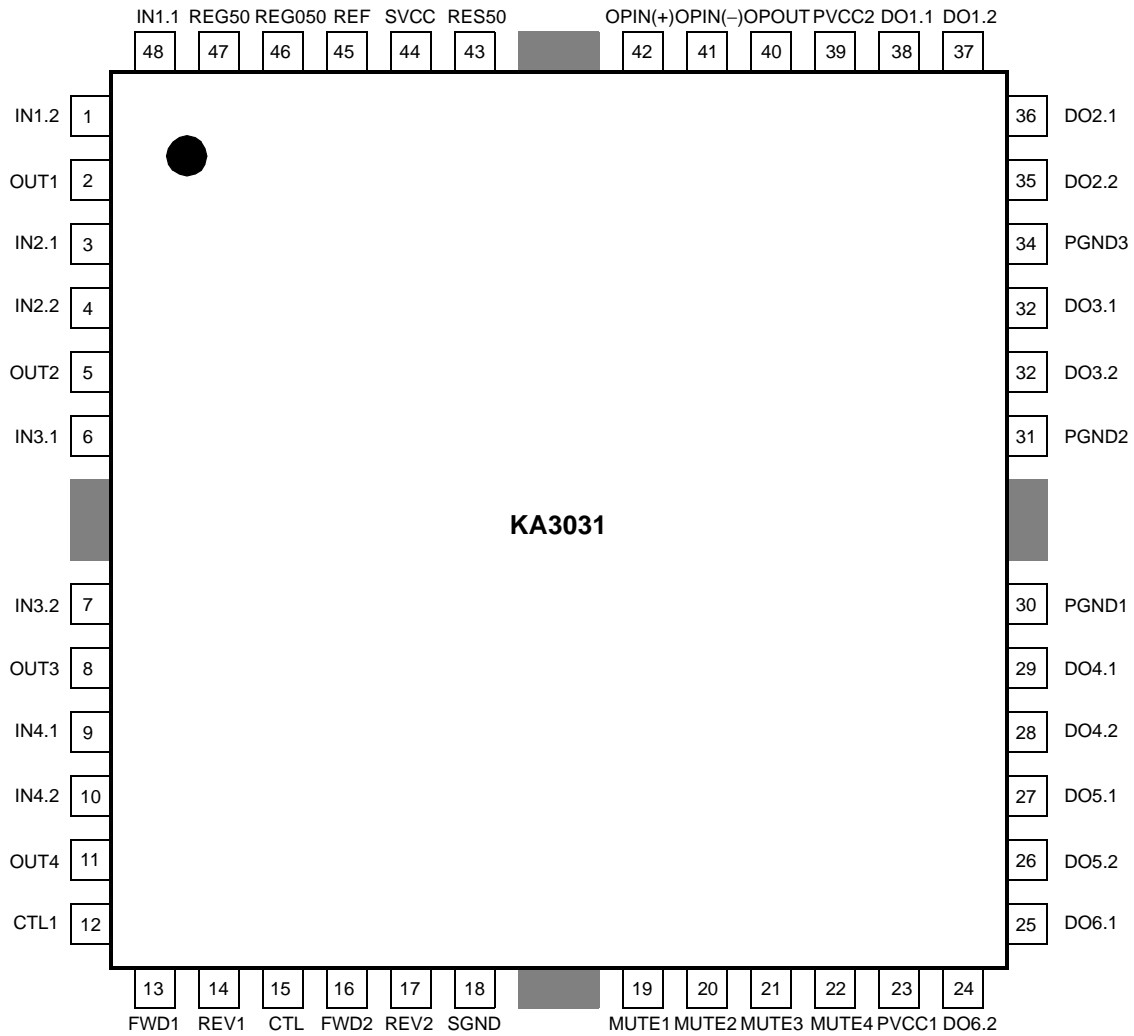
**BLOCK DIAGRAM**



**NOTES:**

1. SW = Logic switch
2. MSC = Motor speed control
3. D = Output driver

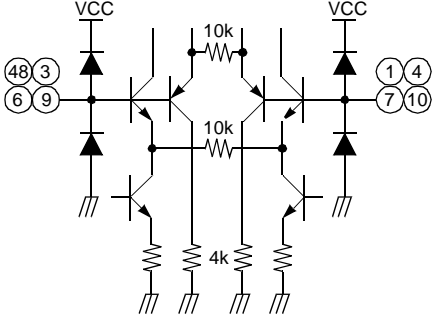
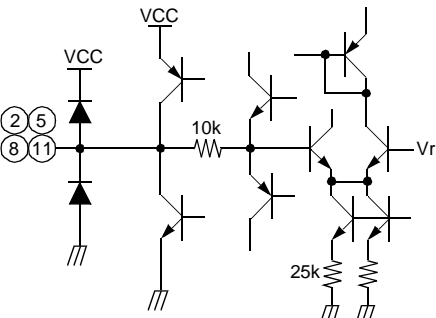
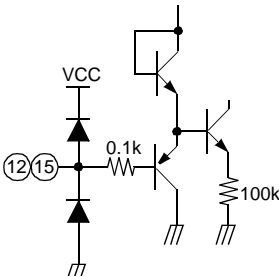
PIN CONFIGURATION



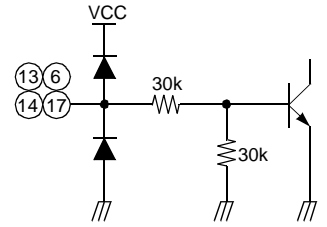
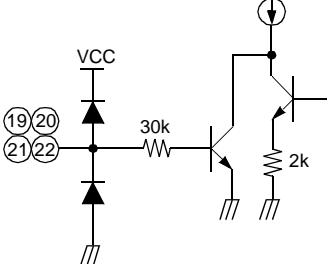
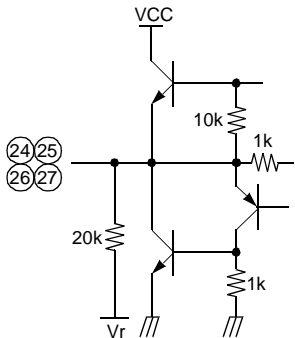
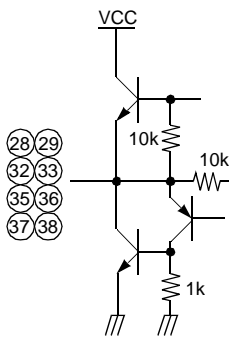
## PIN DESCRIPTION

Pin No.	Symbol	I/O	Description	Pin No.	Symbol	I/O	Description
1	IN1.2	I	CH 1 op-amp input (-)	25	DO6.1	O	CH 6 drive output
2	OUT1	O	CH 1 op-amp output	26	DO5.2	O	CH 5 drive output
3	IN2.1	I	CH 2 op-amp input (+)	27	DO5.1	O	CH 5 drive output
4	IN2.2	I	CH 2 op-amp input (-)	28	DO4.2	O	CH 4 drive output
5	OUT2	O	CH 2 op-amp output	29	DO4.1	O	CH 4 drive output
6	IN3.1	I	CH 3 op-amp input (+)	30	PGND	-	Power ground
7	IN3.2	I	CH 3 op-amp input (-)	31	PGND	-	Power ground
8	OUT3	O	CH 3 op-amp output	32	DO3.2	O	CH 3 drive output
9	IN4.1	I	CH 4 op-amp input (+)	33	DO3.1	O	CH 3 drive output
10	IN4.2	I	CH 4 op-amp input (-)	34	PGND	-	Power ground
11	OUT4	O	CH 4 op-amp output	35	DO2.2	O	CH 2 drive output
12	CTL1	I	CH 5 motor speed control	36	DO2.1	O	CH 2 drive output
13	FWD1	I	CH 5 forward input	37	DO1.2	O	CH 1 drive output
14	REW1	I	CH 5 reverse input	38	DO1.1	O	CH 1 drive output
15	CTL2	I	CH 6 motor speed control	39	PVCC2	-	Power supply voltage (For CH 1, CH 2, CH 3, CH 4)
16	FWD2	I	CH 6 forward input	40	OPOUT	O	Opamp output
17	REW2	I	CH 6 reverse input	41	OPIN(-)	I	Opamp input (-)
18	SGND	-	Signal ground	42	OPIN(+)	I	Opamp input (+)
19	MUTE1	I	CH 1 mute	43	RES50	I	Regulator 5V reset
20	MUTE2	I	CH 2 mute	44	SVCC	-	Signal supply voltage
21	MUTE3	I	CH 3 mute	45	REF	I	Bias voltage input
22	MUTE4	I	CH 4 mute	46	REG050	O	Regulator 5V output
23	PVCC1	-	Power supply voltage (For CH 5, CH 6)	47	REG50	O	Regulator output
24	DO6.2	O	CH 6 drive output	48	IN1.1	I	CH 1 opamp input (+)

EQUIVALENT CIRCUIT

Description	Pin No.	Internal circuit
Input OPIN (+) OPIN (-)	48, 3, 6, 9 1, 4, 7, 10	
Input opout	2, 5, 8, 11	
CTL	12, 15	

EQUIVALENT CIRCUIT (Continued)

Description	Pin No.	Internal circuit
Logic drive FWD input REV input	13, 16 14, 17	
CH mute	19, 20 21, 22	
Logic drive output	24, 25 26, 27	
4-CH drive output	28, 29 32, 33 35, 36 37, 38	

EQUIVALENT CIRCUIT (Continued)

Description	Pin No.	Internal circuit
Normal opout	40	
Normal OPIN(+) OPIN(-)	42 41	
Ref	45	

EQUIVALENT CIRCUIT(Continued)

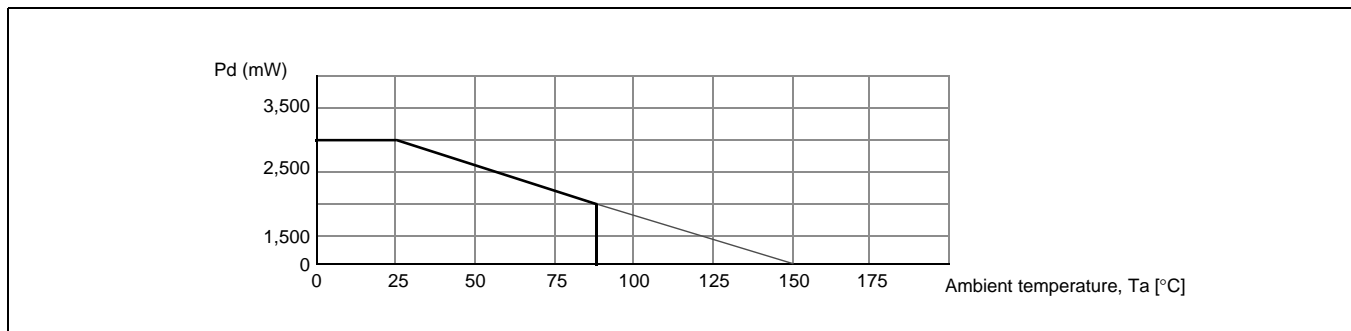
Description	Pin No.	Internal circuit
RES50	43	
REG050	46	
REG50	47	

**ABSOLUTE MAXIMUM RATINGS (Ta=25°C)**

Characteristics	Symbol	Value	Unit
Maximum supply voltage	V <sub>CC</sub>	18	V
Power dissipation	P <sub>D</sub>	3 note	W
Operating temperature	T <sub>OPR</sub>	-35 ~ +85	°C
Storage temperature	T <sub>STG</sub>	-55 ~ +150	°C
Maximum output current	I <sub>OMAX</sub>	1	A

**NOTE:**

1. When mounted on 70mm × 70mm × 1.6mm PCB.
2. Power dissipation reduces 16mW / °C for using above Ta=25°C.
3. Do not exceed Pd and SOA.



**RECOMMENDED OPERATING CONDITIONS (Ta=25°C)**

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Operating supply voltage	V <sub>CC</sub>	4.5	-	16	V

## ELECTRICAL CHARACTERISTICS

(SV<sub>CC</sub>=PV<sub>CC1</sub>=PV<sub>CC2</sub>=8V, Ta=25°C, unless otherwise specified)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Quiescent circuit current	I <sub>CC</sub>	under no-load	9	12	16	mA
All mute on current	I <sub>MUTE ALL</sub>	Pin 45=GND	–	6	10	mA
All mute on voltage	V <sub>MON ALL</sub>	Pin 45=Variation	–	–	0.5	V
All mute off voltage	V <sub>MOFF ALL</sub>	Pin 45=Variation	2	–	–	V
CH mute on voltage	V <sub>MON CH</sub>	Pin 19, 20, 21, 22=Variation	2	–	–	V
CH mute off voltage	V <sub>MOFF CH</sub>	Pin 19, 20, 21, 22=Variation	–	–	0.5	V
<b>DRIVER PART (R<sub>L</sub>=8Ω)</b>						
Input offset voltage	V <sub>IO</sub>	–	–20	–	+20	mV
Output offset voltage	V <sub>OO</sub>	V <sub>IN</sub> =2.5V	–50	–	+50	mV
Maximum output voltage 1	V <sub>OM1</sub>	V <sub>CC</sub> =8V, R <sub>L</sub> =8Ω	4.0	5.5	–	V
Maximum output voltage 2	V <sub>OM2</sub>	V <sub>CC</sub> =13V, R <sub>L</sub> =24Ω	7	9	–	V
Closed-loop voltage gain	A <sub>VF</sub>	V <sub>IN</sub> =0.1V <sub>RMS</sub>	9	10.5	12	dB
Ripple rejection ratio	RR	V <sub>IN</sub> =0.1V <sub>RMS</sub> , f=120kHz	–	50	–	dB
Slew rate	SR	Square, V <sub>out</sub> =2Vp-p, f=120kHz	–	0.8	–	V/μs
<b>NORMAL OPAMP PART</b>						
Input offset voltage	V <sub>OF1</sub>	–	–10	–	+10	mV
Input bias current	I <sub>B1</sub>	–	–	–	300	nA
High level output voltage	V <sub>OH1</sub>	R <sub>L</sub> =50Ω	6	6.8	–	V
Low level output voltage	V <sub>OL1</sub>	R <sub>L</sub> =50Ω	–	1.0	1.8	V
Output sink current	I <sub>SINK1</sub>	V <sub>IN</sub> =–75dB, f=1kHz	10	40	–	mA
Output source current	I <sub>SOURCE1</sub>	V <sub>IN</sub> =–20dB, f=120kHz	10	40	–	mA
Open loop voltage gain	GV <sub>O1</sub>	Square, V <sub>out</sub> =2Vp-p, f=120kHz	–	75	–	dB
Ripple rejection ratio	RR1	V <sub>IN</sub> =–20dB, f=1kHz	–	65	–	dB
Slew rate	SR1	–	–	1	–	V/μs
Common mode rejection ratio	CMRR1	–	–	80	–	dB

**ELECTRICAL CHARACTERISTICS (Continued)**(SV<sub>CC</sub>=PV<sub>CC1</sub>=PV<sub>CC2</sub>=8V, Ta=25°C, unless otherwise specified)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
<b>INPUT OPAMP PART</b>						
Input offset voltage	V <sub>OF2</sub>	–	–10	–	+10	mV
Input bias current	I <sub>B2</sub>	–	–	–	400	nA
High level output voltage	V <sub>OH2</sub>	–	7	7.7	–	V
Low level output voltage	V <sub>OL2</sub>	–	–	0.2	0.5	V
Output sink current	I <sub>SINK2</sub>	–	500	800	–	μA
Output source current	I <sub>SOURCE2</sub>	–	500	800	–	μA
Open loop voltage gain	GV <sub>O2</sub>	V <sub>IN</sub> =–75dB, f=1kHz	–	80	–	dB
Slew rate	SR2	Square, V <sub>out</sub> =2Vp-p, f=120kHz	–	1	–	V/μs
Common mode rejection ratio	CMRR2	V <sub>IN</sub> =–20dB, f=1kHz	–	80	–	dB
<b>5V REGULATOR PART</b>						
Regulator output voltage	V <sub>reg</sub>	I <sub>L</sub> =100mA	4.75	5	5.25	V
Load regulation	ΔV <sub>R1</sub>	I <sub>L</sub> =0→200mA	–40	0	+10	mV
Line regulation	ΔV <sub>CC</sub>	I <sub>L</sub> =200mA, V <sub>CC</sub> =6V→9V	–20	0	+30	mV
Reset on voltage	Reson	–	–	–	0.5	V
Reset off voltage	Resoff	–	2	–	–	V
<b>TRAY, CHANGER DRIVER PART (R<sub>L</sub>=45Ω)</b>						
Input high level voltage	V <sub>IH</sub>	–	2	–	–	V
Input low level voltage	V <sub>IH</sub>	–	–	–	0.5	V
Output voltage 1	V <sub>O1</sub>	V <sub>CC</sub> =8V, V <sub>CTL</sub> =3.5V	5.2	6.0	6.8	V
Output voltage 2	V <sub>O2</sub>	V <sub>CC</sub> =13V, V <sub>CTL</sub> =4.5V	7.5	8.5	9.5	V
Output load regulation	ΔV <sub>R1</sub>	–	–	300	700	mV
Output offset voltage 1	V <sub>OO1</sub>	V <sub>IN</sub> =5V, 5V	–10	–	+10	mV
Output offset voltage 2	V <sub>OO2</sub>	V <sub>IN</sub> =0V, 0V	–10	–	+10	mV

## APPLICATION INFORMATION

### 1. REFERENCE INPUT & ALL MUTE FUNCTION

Pin 45 (REF) can use the reference Input pin or the all mute signal input pin.

- Reference input  
In the case of the reference input pin, you must keep the applied voltage range between 2[V] and 6.5[V] at  $V_{CC} = 8[V]$ .
- All mute input  
When using the all mute function pin, applied voltage condition is as follows.

All mute on voltage	Below 0.5[V]	Mute function operation
All mute off voltage	Above 2[V]	Normal operation

### 2. SEPARATED CHANNEL MUTE FUNCTION

These pins are used for individual channel mute operation.

- When the mute pins (pin19, 20, 21 and 22) are high level, the mute circuits are activated so that the output circuit is muted.
- When the voltage of the mute pins (pin19, 20, 21 and 22) are low level, the mute circuit is stopped and output circuits operate normally.
- If the chip temperature rises above 175°C, then the thermal shutdown (TSD) circuit is activated and the output circuits are muted.
  - Mute 1 (pin 19)-CH1 mute control input pin.
  - Mute 2 (pin 20)-CH2 mute control input pin.
  - Mute 3 (pin 21)-CH3 mute control input pin.
  - Mute 4 (pin 22)-CH4 mute control input pin.

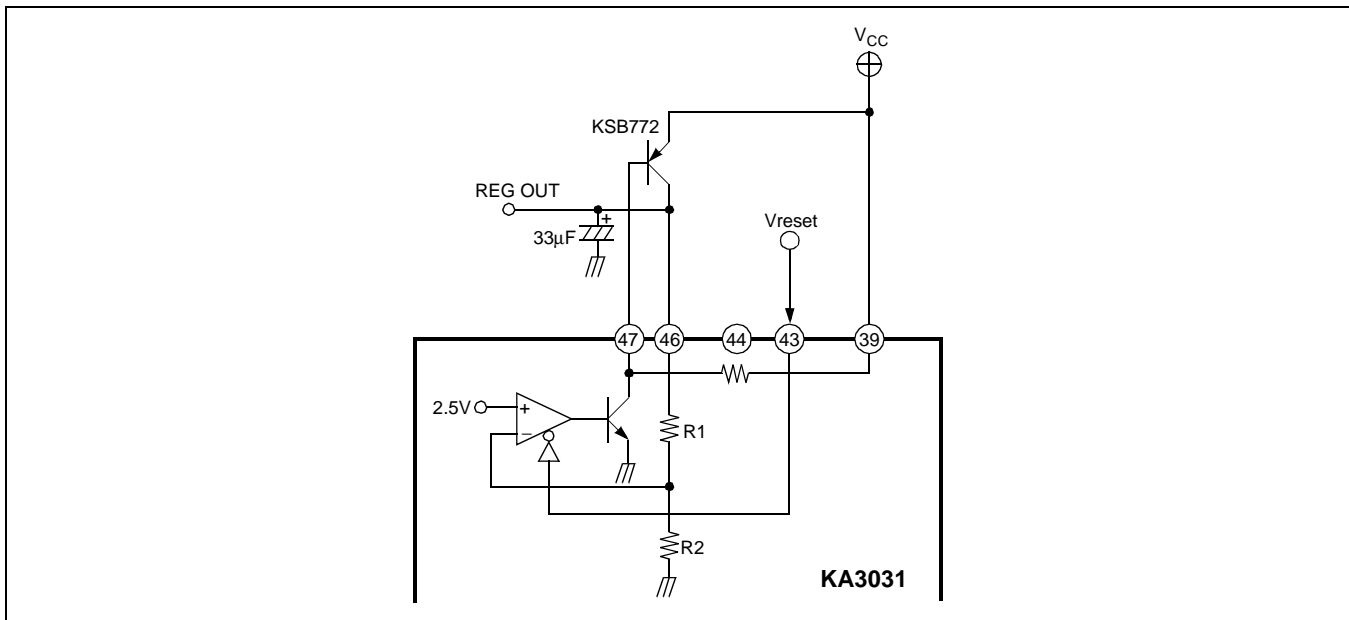
### 3. PROTECTION FUNCTION

- Thermal shutdown (TSD)  
If the chip temperature rises above 175°C, then the thermal shutdown (TSD) circuit is activated and the output circuit is will be mute. The TSD circuit is temperature hysteresis 25°C.
- Under voltage lockout (UVLO) and over voltage protection (OVP)  
It is designed to mute-operate the internal bias by the function of UVLO and OVP, when the power supply voltage falls below 3.5[V] or above 20[V].

**4. REGULATOR & RESET FUNCTION**

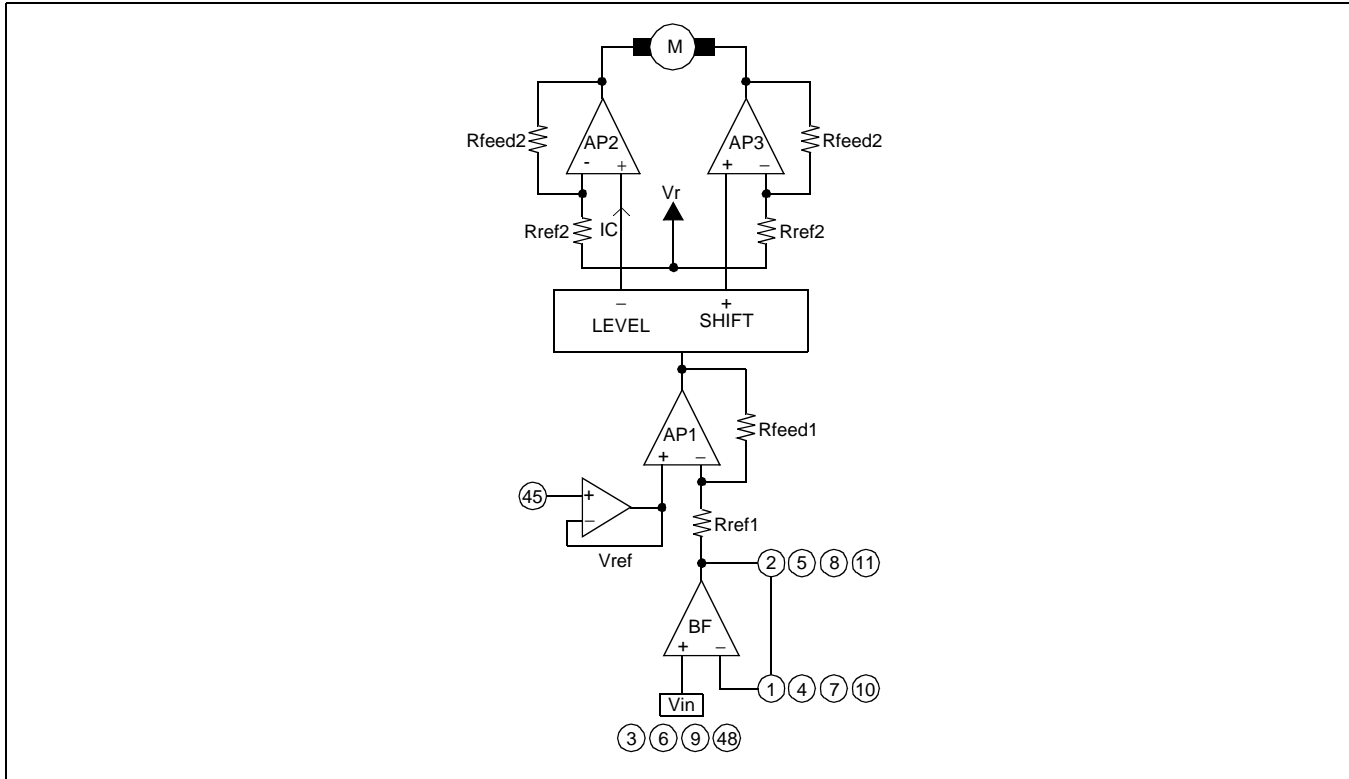
The regulator and reset circuits are as illustrated in Figure 1. where R1=R2.

- The external circuit is composed of the transistor, KSB772 and a capacitor, about 33[μF]. The capacitor is used as a ripple eliminator and should have good temperature characteristics.
- The regulator output voltage (pin 46) is decided as follows.  
 $V_{out} = 2 \times 2.5 = 5[V]$  (where R1 = R2)
- When the voltage of pin 43 (Vreset) is at 5[V], the regulator output voltage (pin 46) because 5[V]. If the voltage of pin 43 is 0[V], the output voltage of pin 46 because 0[V].



**Figure 1. Regulator circuit**

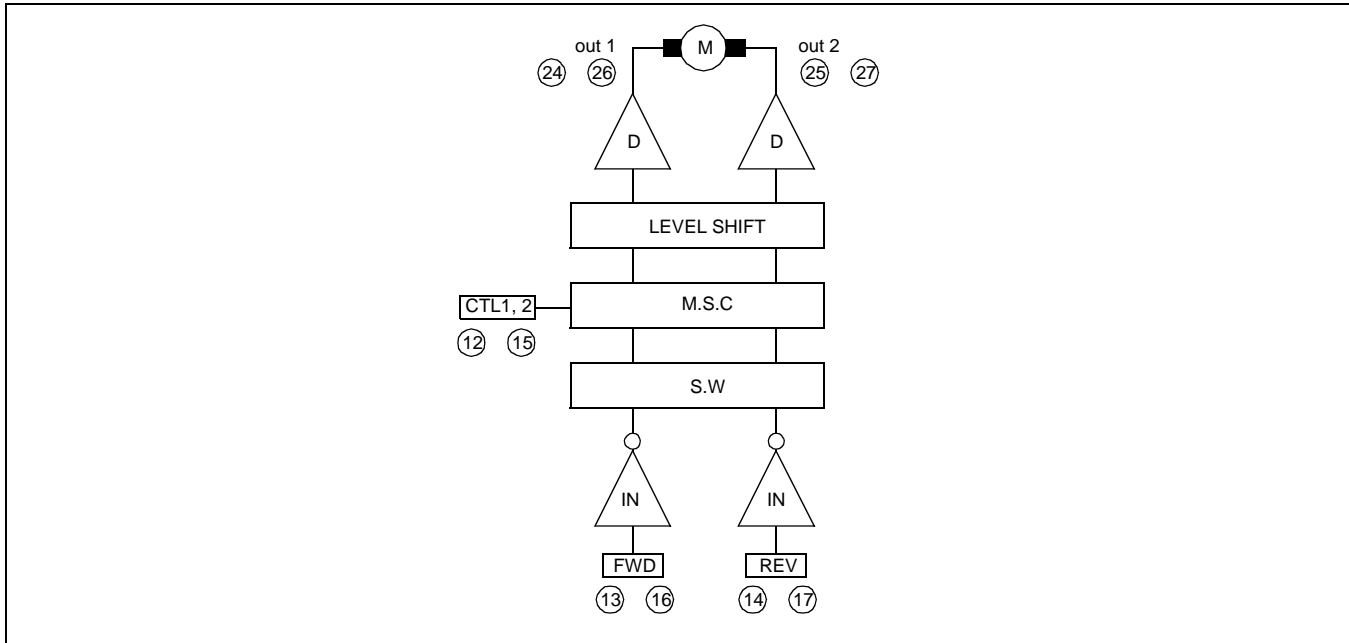
## 5. FOCUS, TRACKING ACTUATOR, SPINDLE, SLED MOTOR DRIVE PART



- The voltage,  $V_{ref}$  is the reference voltage given by the external bias voltage of the pin 45.
- The input signal ( $V_{in}$ ) through pins 3, 6, 9 and 48 is amplified one times ( $R_{ref1} = R_{feed1}$ ) by the AP1 and then fed to the level shift.
- The level shift produces the current due to the difference between the input signal and the arbitrary reference signal. The current produced as  $+\Delta I$  and  $-\Delta I$  are fed into the output amplifier, where output amplifier (AP2, 3) gain is two times (all  $R_{ref2} = R_{feed2}$ ).
- If you desire to change the gain, the input buffer amplifier (BF) can be used.
- The output stage is the balanced transformerless (BTL) driver.
- The bias voltage  $V_r$  is expressed as below;

$$V_r = \frac{V_{CC} - V_{BE}}{2} [V]$$

6. TRAY, CHANGE MOTOR DRIVE PART



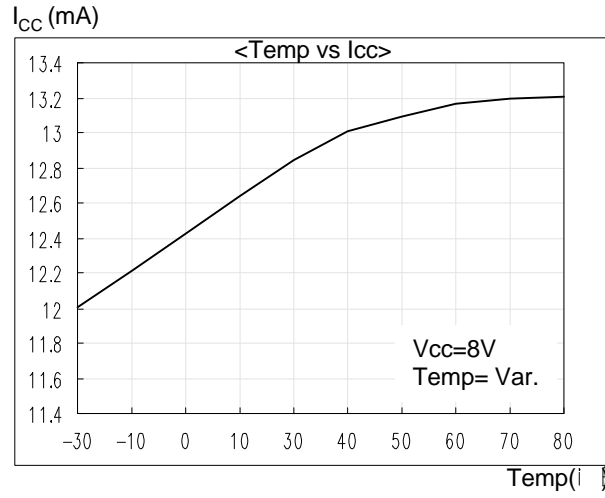
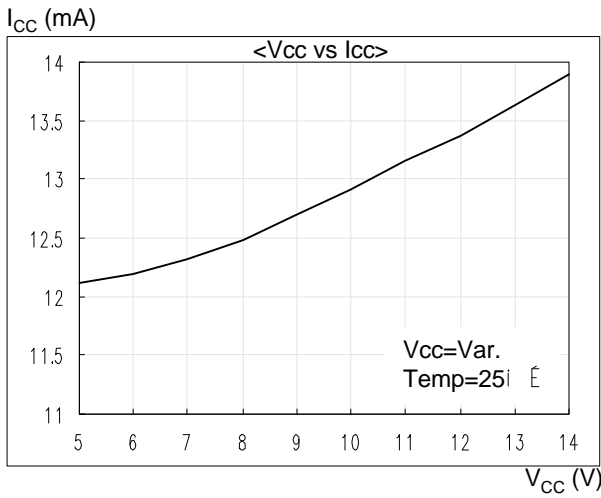
- Rotational direction control  
The forward and reverse rotational direction is controlled by FWD (pin 13, 16) and REV (pin 14, 17) input conditions are as follows.

INPUT		OUTPUT		
FWD	REV	OUT 1	OUT 2	State
H	H	Vr	Vr	Brake
H	L	H	L	Forward
L	H	L	H	Reverse
L	L	Vr	Vr	Brake

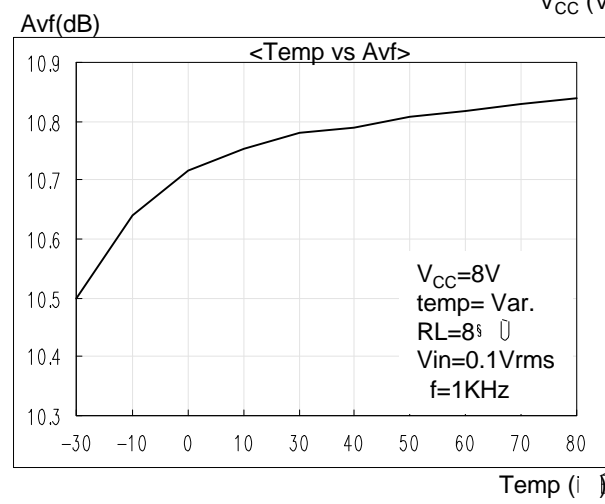
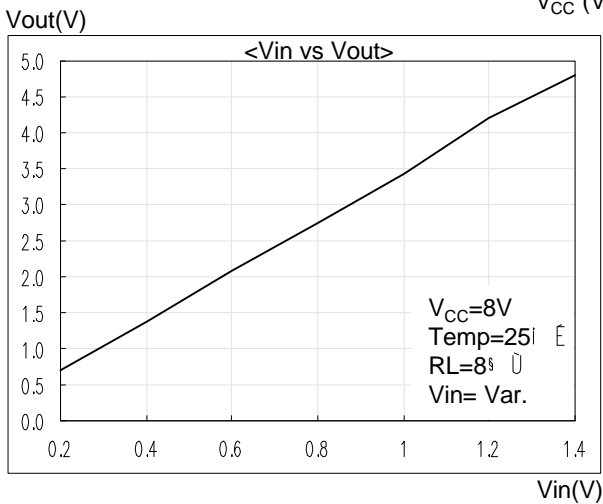
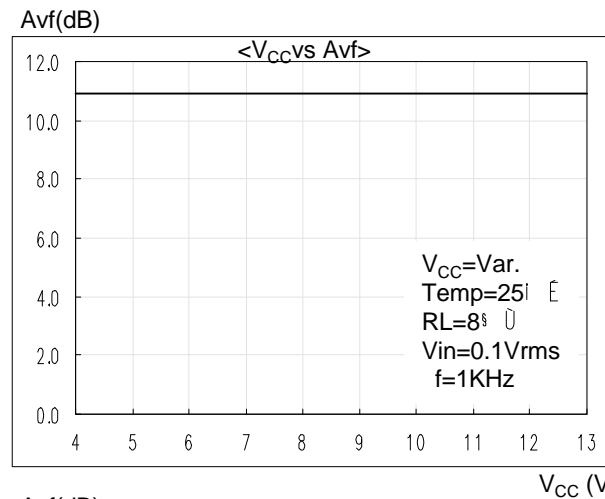
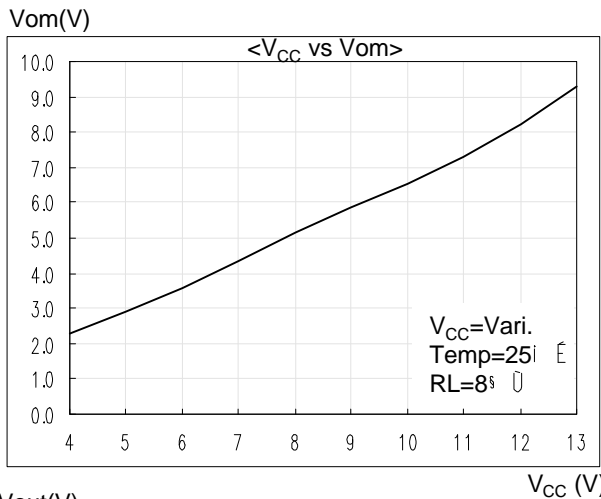
- where Vr is  $(V_{cc} - V_{be}) / 2 = 3.65V$  (at  $V_{cc}=8V$ )
- where Out1 pins are pins 24 and 26, and out2 pins aer pins 25 and 27
- Motor speed control
  - The almost maximum torque is obtained when it is used with the pins 12 and 15 (CTL1, 2) open.
  - If the torque of the motor is too low, then the applied voltage at pins 12 and 15 (CTL1, 2) are 0[V].
  - When motor speed controlled, the applied voltage of the pins 12 and 15 (CTL1, 2) is between 0 and 4V. Also, if the speed control is constant, the applied voltage of the pins 12 and 15 (CTL1, 2) is between 4 and 5V.
  - This IC's applied maximum voltage is 6V when  $V_{CC}$  is 8V.
  - You must not use the applied CTL1, 2 voltage above 5.8V when  $V_{CC}$  is 8V, and 3V when  $V_{CC}$  is 5V.

**ELECTRICAL CHARACTERISTICS CURVES**

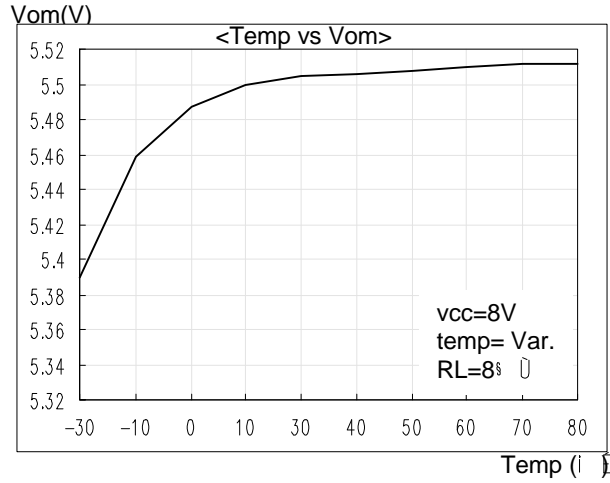
**Total circuit**



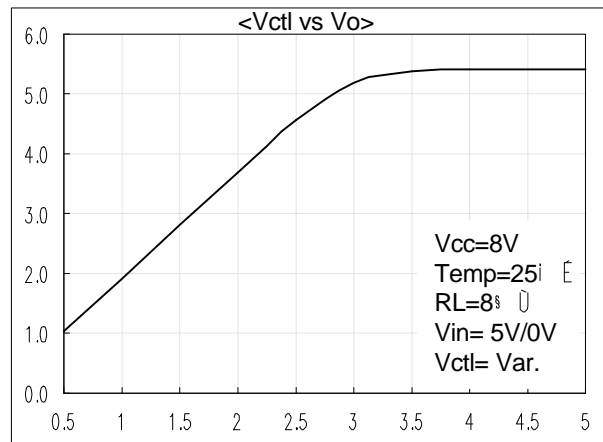
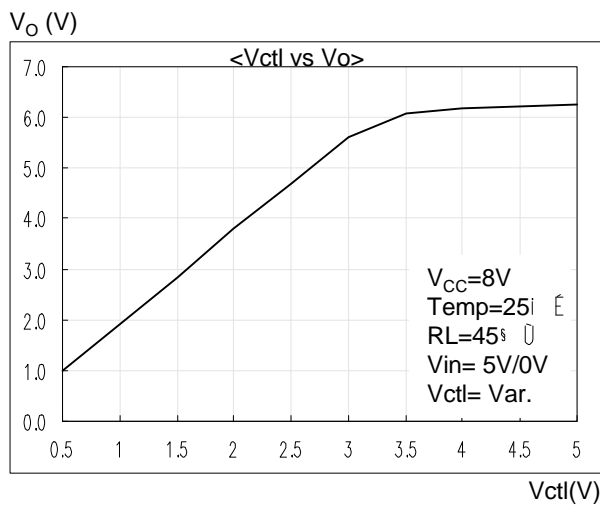
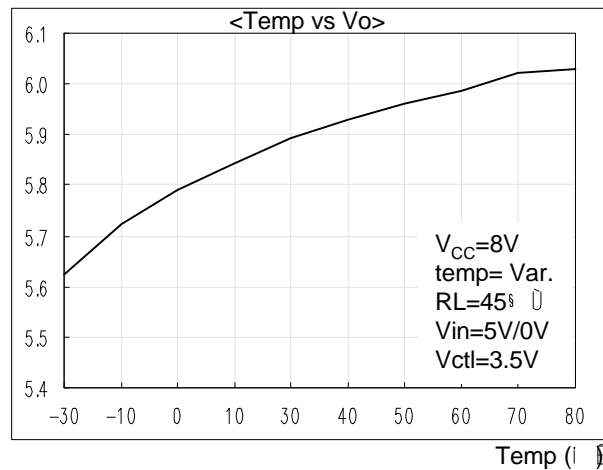
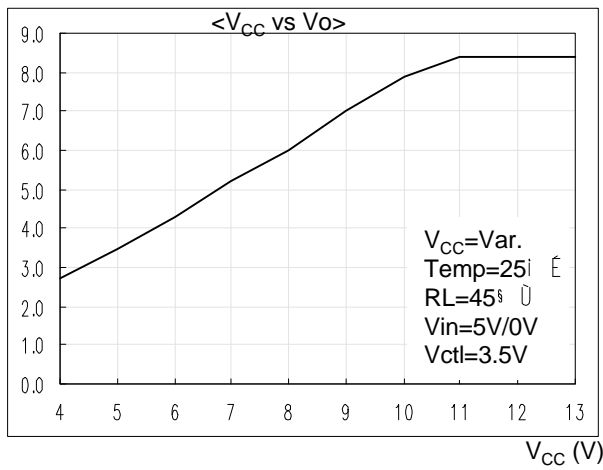
**Focus, Tracking, Spindle, Sled drive part**



ELECTRICAL CHARACTERISTICS CURVES (Continued)

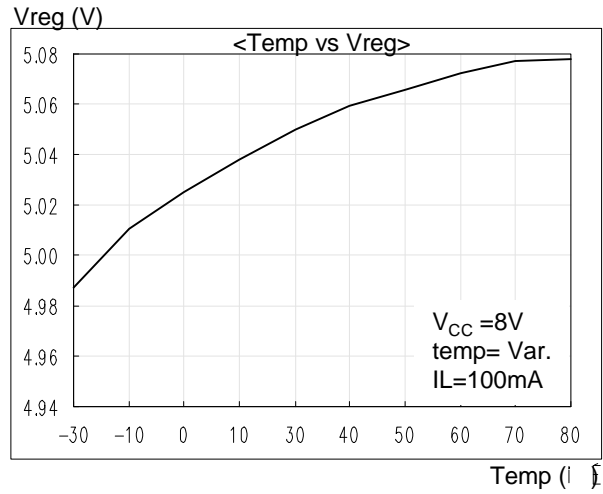
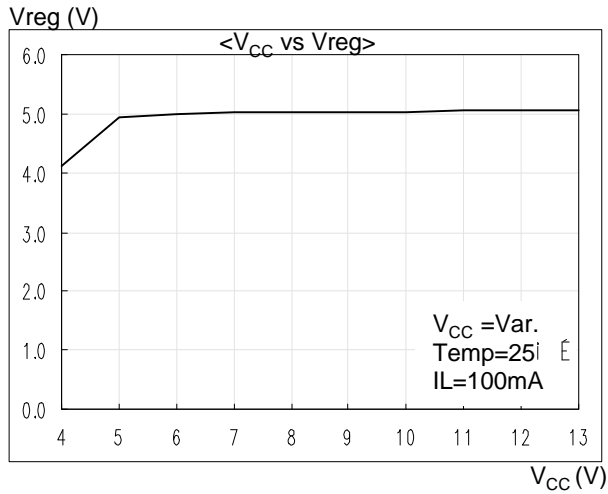


Tray, Change drive part

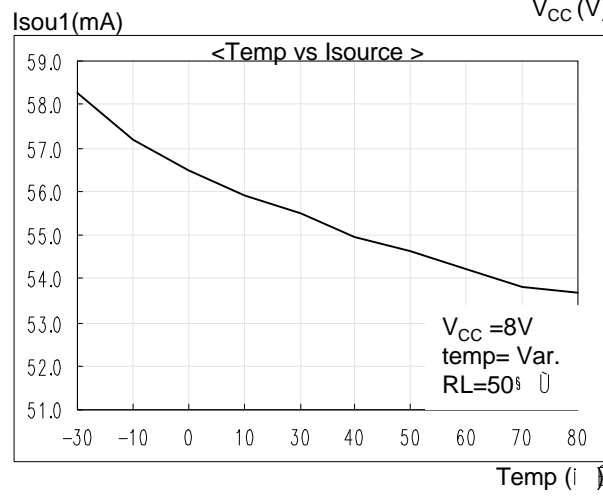
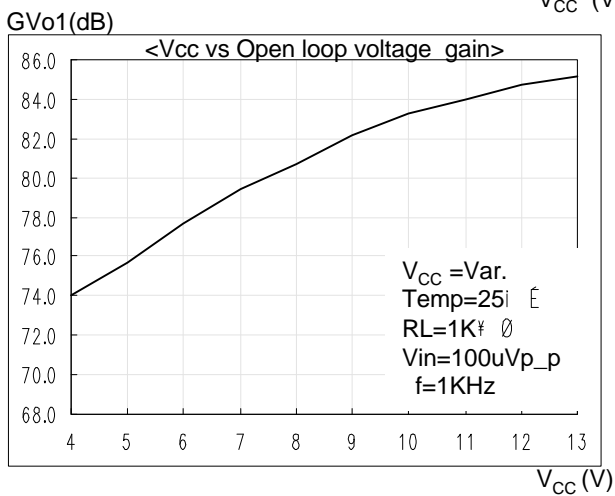
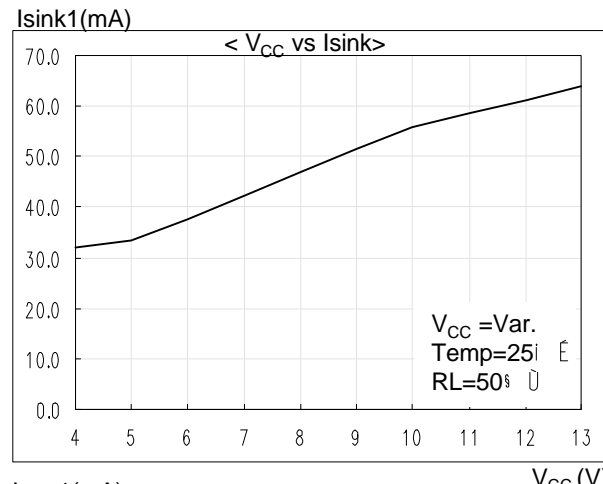
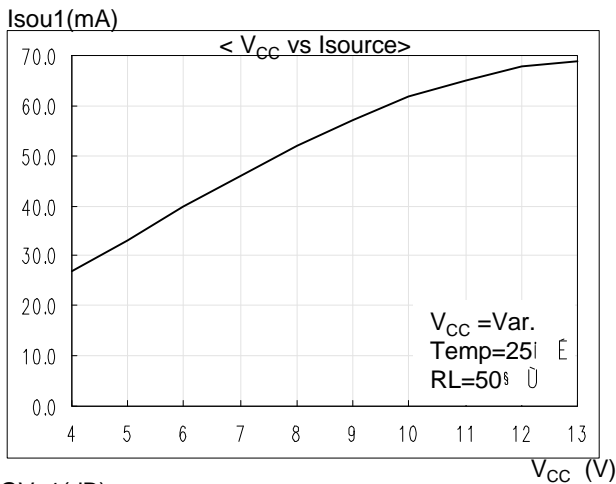


**ELECTRICAL CHARACTERISTICS CURVES (Continued)**

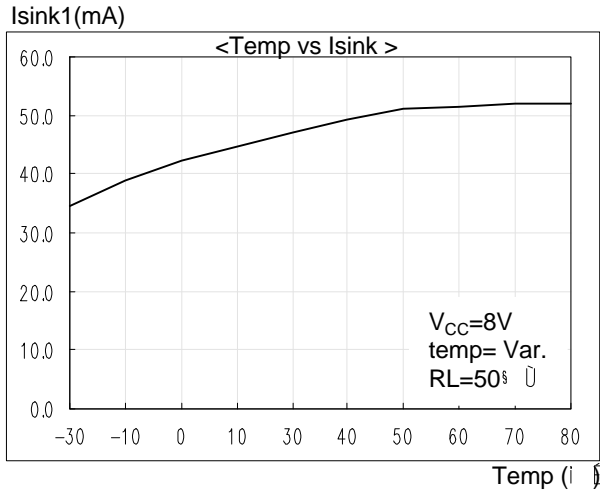
**Regulator part**



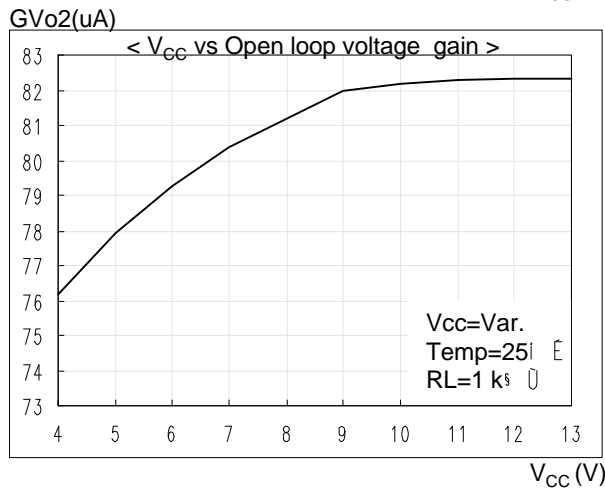
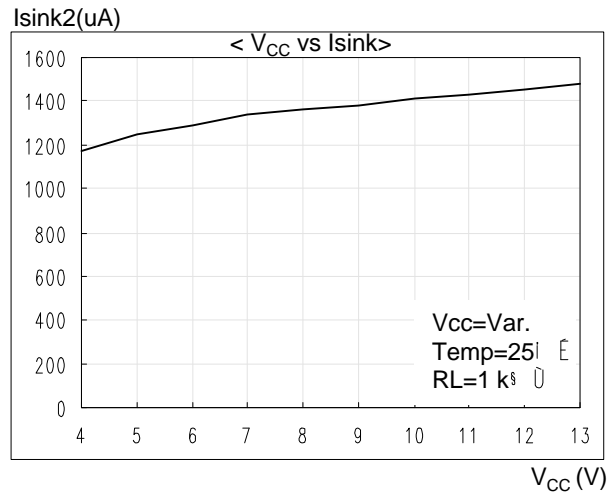
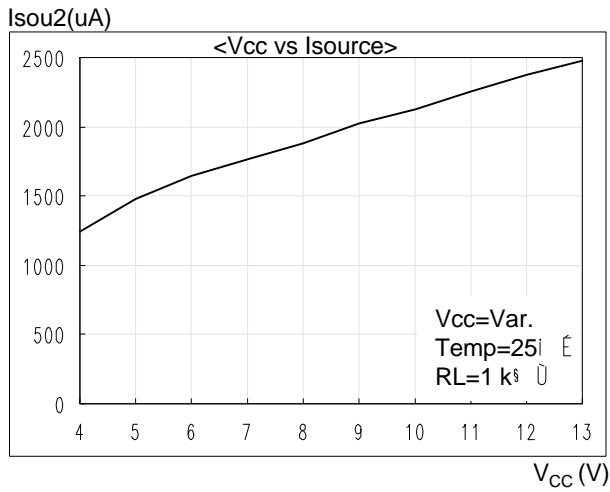
**Normal op amp part**



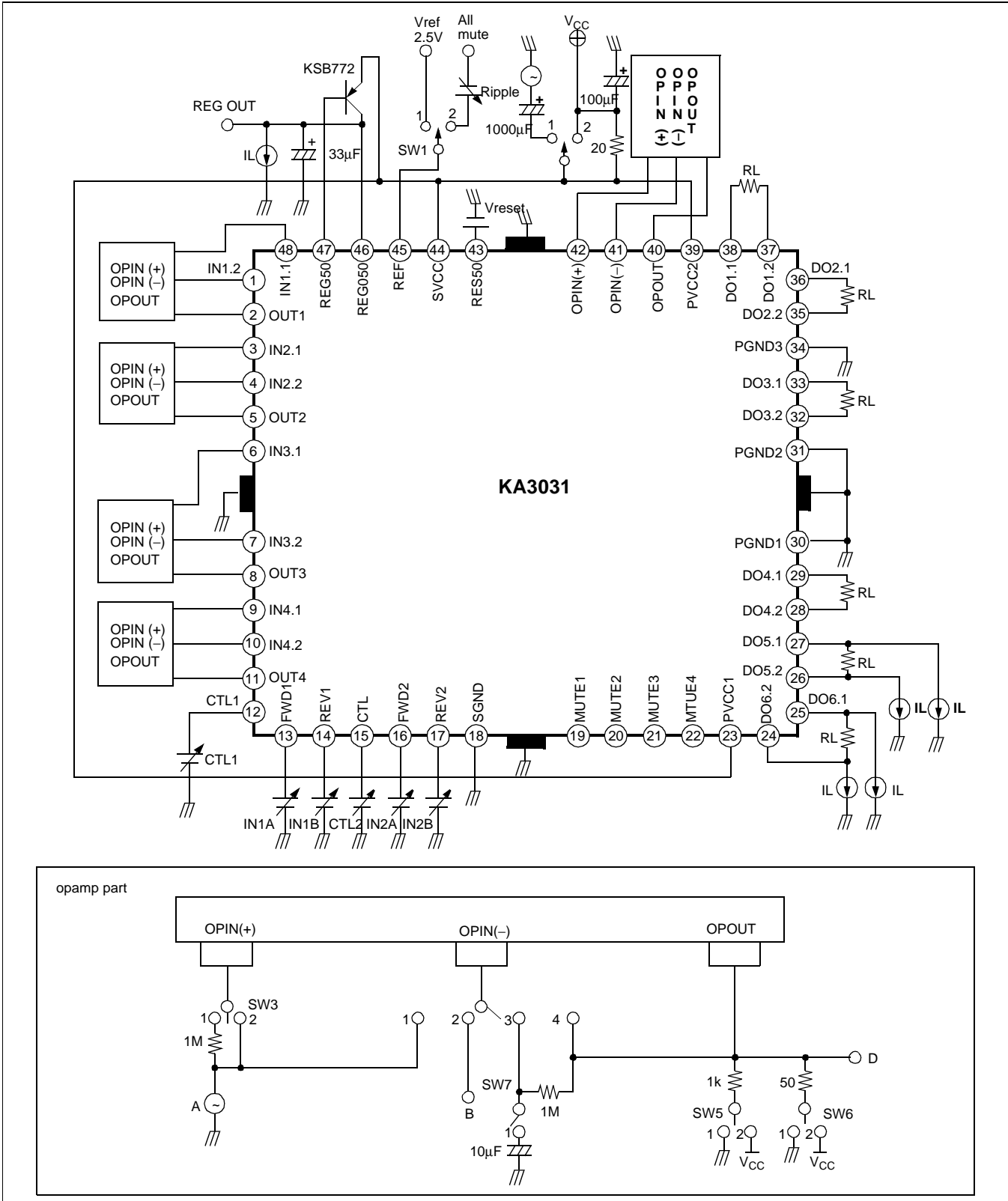
**ELECTRICAL CHARACTERISTICS CURVES (Continued)**



**Input op amp part**

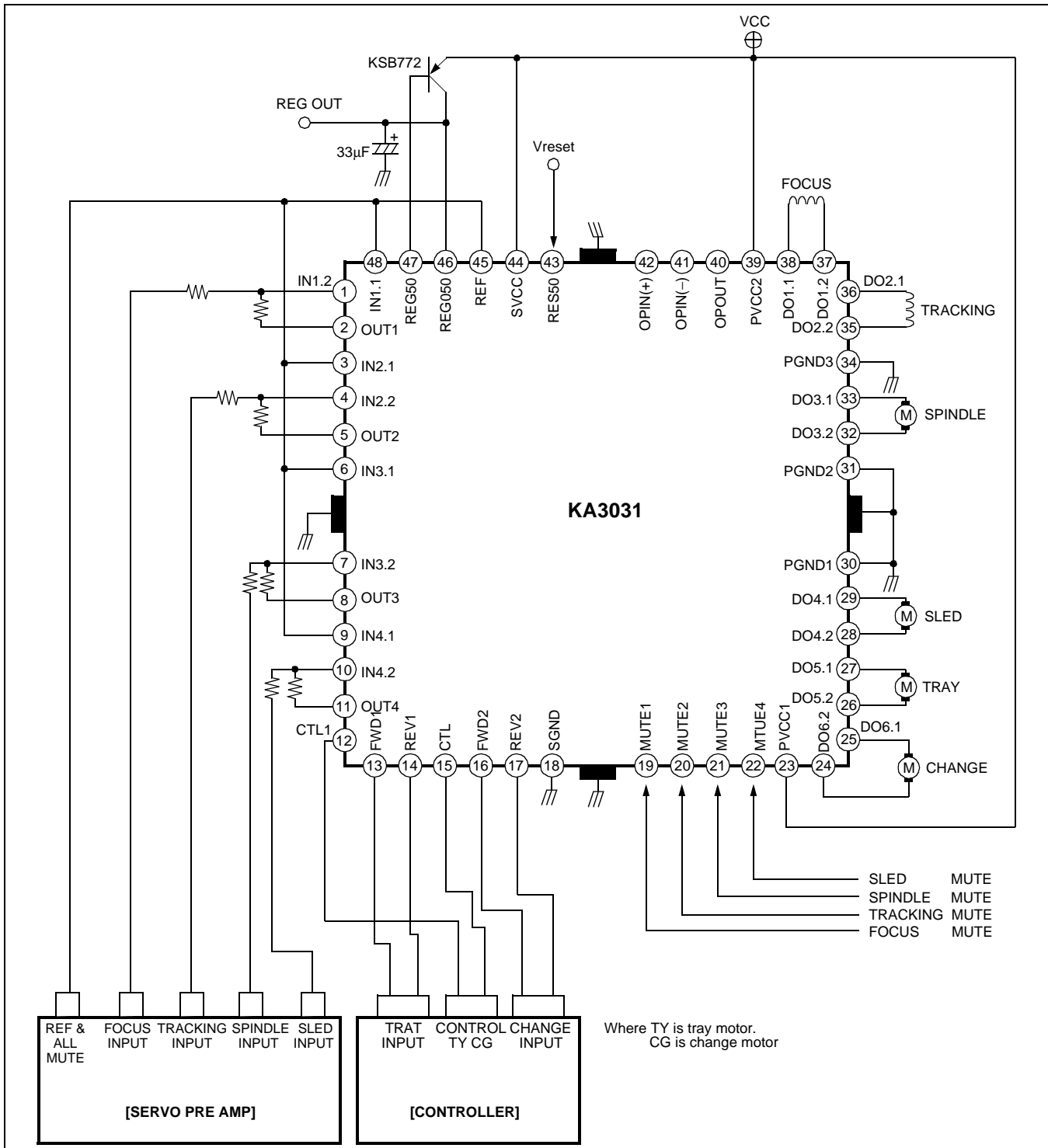


TEST CIRCUIT



APPLICATION CIRCUIT

Voltage Mode Control



**NOTE:** Radiation pin is connected to the internal GND of the package.  
Connect the pin to the external GND.





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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.