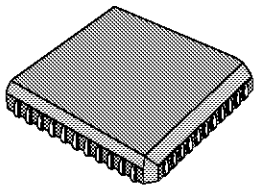
SGS-THOMSON MICROELECTRONICS

L3000N
STLC3040

THIRD GENERATION SUBSCRIBER LINE INTERFACE

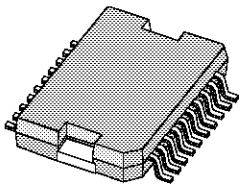
PRODUCT PREVIEW

- TWO CHIP SET + OVERVOLTAGE PROTECTION PROVIDE THE COMPLETE BORSCHT FUNCTIONS.
- PROGRAMMABLE DC FEEDING RESISTANCE AND CURRENT LIMITING 0 TO 70mA (1.1mA STEPS).
- PROGRAMMABLE VOLTAGE DROP ACCORDING TO TTX/ON HOOK TRANSMISSION NEEDS.
- INTEGRATED RING GENERATOR WITH ZERO CROSSING AND PROGRAMMABLE FREQ/LEVEL.
- SUPPORT NORMAL LOOP START LINES, GROUND START PABX LINES, EXTENDED LOOPS AND PAY-PHONES.
- GENERATION, SHAPING AND FILTERING OF 12KHz/16kHz PROGRAMMABLE LEVELS TELETAX METERING SIGNALS.
- REVERSE POLARITY HARD OR SOFT SWITCHING.
- SIGNALLING FUNCTIONS HOOK, GDKEY WITH PROGRAMMABLE PERSISTANCE CHECK.
- ON HOOK TRANSMISSION CAPABILITY.
- CCITT AND LSSGR CODEC/FILTER STD. A/μ LAW.
- 2 WIRE IMPEDANCE SYNTHESIS SOFTWARE PROGRAMMABLE.
- HYBRID FUNCTION SOFTWARE PROGRAMMABLE.
- PROGRAMMABLE GAIN CONTROL AND FREQUENCY RESPONSE CORRECTION.
- SUPERVISION AND TEST OF LINE CONDITIONS, LEAKAGE, CAPACITANCE AND CIRCUIT SIGNALLING TEST FOR TTX AND RINGING.
- TEST TONE GENERATION FOR CIRCUIT TEST, LOOPBACKS POSSIBILITY.
- GCI COMPATIBLE CONTROL INTERFACE.
- SELECTABLE 2/4MHZ BACKPLANE CLOCK.
- MINIMUM EXTERNAL COMPONENTS COUNT.
- ADVANCED 12V BJT-5V CMOS 0.8μmTECHNOLOGY GUARANTEES RELIABILITY AND LOW POWER CONSUMPTION (50MW TOTAL IN ON-HOOK CONDITION).
- INTEGRATED THERMAL PROTECTION WITH THERMAL OVERLOAD INDICATION.



PLCC44

ORDERING NUMBER: STLC3040



PowerSO-20

ORDERING NUMBER: L3000NSO

DESCRIPTION

The subscriber line interface kit (L3000N/STLC3040) is a set of solid state devices designed to integrate all the classical BORSCHT functions (overvoltage protection external) and several additional features needed to interface a telephone line.

The L3000N device is fabricated in B140II (140V Bipolar) technology and is basically an analog front end that drives the line via two output buffers properly amplifying signal applied at its input by the STLC3040. At the same time it provides back to the STLC3040 an accurate image of the loop current.

The STLC3040 device is fabricated in BiCMOS (12V bipolar / 5V CMOS) technology. This device interfaces the L3000N via a dedicated interface and the C.O. backplane via a GCI compatible interface.

The STLC3040 processes the line current image provided by the L3000N generating the transmit signal and the proper voltage signal that will be sent back to the L3000N in order to synthetize the desired AC/DC impedances on the 2-wire side.
At the same time also the received signal on the digital side is transferred into the line.

The signal processing inside the STLC3040 is both analog and digital merging the best available analog and digital processing performances of the BiCMOS technology.

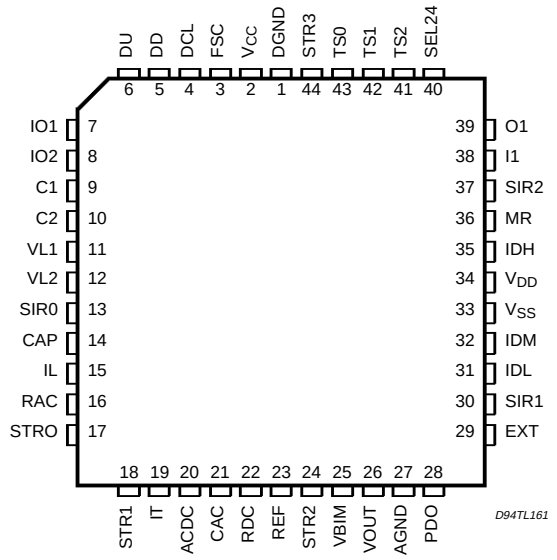
The L3000N/STLC3040 kit is fully programmable and needs only 5 ext. resistors (including the two protection resistors) and 3 capacitors. These components are always the same; all the parameters related to different applications are software programmed. Considering the DC characteristic, by proper programming it is possible to select several limiting currents (from 0 to 70mA with 1.1mA steps, different DC feeding resistance (from 0 to 2 x 400Ω with 100Ω steps) and different drop voltages (on-hook transmission, metering pulse injection).

Considering AC performances all possible 2-wire impedances are software programmable, the same for the two to four wire conversion, where all the possible balance impedances can be software programmed. Both Tx and Rx gain are programmable (12 dB range, 0.1dB step) with proper frequency equalization that will guarantee a complete flat response in the speech band.

Ringing signal is also generated on chip with programmable frequency and amplitude. For this purpose the L3000N device in addition to the negative battery (VB-) requires also a positive one (VB+). VB- can vary between -70V to -24V depending on the application. The VB+ is usually selected in order to have a total battery voltage |VB+|+|VB-| = 120V.
Ring injection and disconnection is always performed in correspondance of zero crossing. In addition when ring trip is detected the ring signal is automatically disconnected again at the first zero crossing. The kit is also able to generate metering pulse signals (12 or 16kHz) with programmable amplitudes up to 5Vrms. Polarity reversal is supported.

Finally several testing features are provided by the kit. This means that the kit is able both to test itself and also the line parameters (leakage, capacitance ..) saving the testing relays and the equipment needed to perform the test.

PIN CONNECTIONS (Top views)



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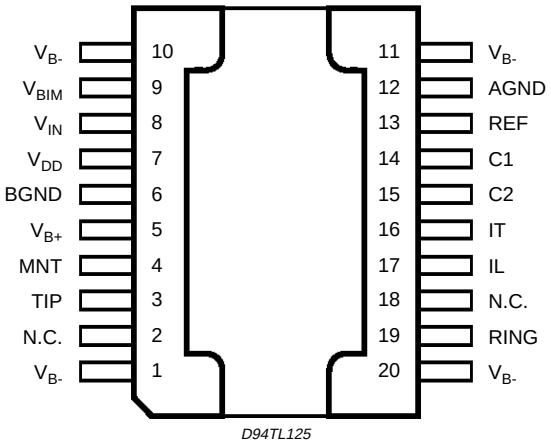


PowerSO-20

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{B-}	Negative Battery Voltage	-80	V
V_{B+}	Positive Battery Voltage	+80	V
$\|V_{B-}\|+\|V_{B+}\|$	Total Battery Voltage	140	V
V_{DD}	Positive Supply Voltage	+5.5	V
V_{SS}	Negative Supply Voltage	-5.5	V
|Vagnd-Vbgnd|	Maximum Voltage Between AGND/BGND	5	V
T_j	Maximum Junction Temperature	150	°C
T_{stg}	Storage Temperature	-55 to +150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
L3000N				
$R_{Th\ j\text{-}case}$	Thermal Resistance Junction to Case	Typ.	2	°C/W
$R_{Th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	Max.	60	°C/W
STLC3040				
$R_{Th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	Max.	80	°C/W

OPERATING RANGE (Refer to the test circuit, unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
T_{oper}	Operating Temperature Range		0		70	°C
V_{B-}	Negative Battery Voltage		-70	-48	-24	V
V_{B+}	Positive Battery Voltage		0	72	75	V
$\|V_{B-}\|+\|V_{B+}\|$	Total Battery Voltage			120	130	V
V_{DD}	Positive Supply Voltage		+4.5		+5.5	V
V_{SS}	Negative Supply Voltage		-5.5		-4.5	V
I_{max}	Total Line Current (IL+IT)				85	mA

PIN DESCRIPTION (L3000N)

PowerSO-20 N°	Name	Description
3	TIP	A line termination output with current capability up to 100mA (I_a is the current sourced from this pin).
4	MNT	Positive Supply Voltage Monitor.
5	V_{B+}	Positive Battery Supply Voltage.
6	BGND	Battery ground relative to the V_{B+} and the V_{B-} supply voltages. It is also the reference ground for TIP and RING signals.
7	V_{DD}	Positive Power Supply +5V.
8	V_{IN}	2 wire unbalanced voltage input.
9	VBIM	Output voltage without current capability, with the following functions: - give an image of the total battery voltage scaled by 40 to the low voltage part. - filter by an external capacitor the noise on V_{B+} and V_{B-}.
1,10,11,20	V_{B-}	Negative Battery Supply Voltage.
12	AGND	Analog Ground. All input signals and the V_{DD} supply voltage must be referred to this pin.
13	REF	Voltage reference output with very low temperature coefficient. The connected resistor sets Internal circuit bias current.
14	C1	Digital signal input (3 levels) that defines device status with pin 12. In thermal overload condition a 240mA typical current is sunk by this pin.
15	C2	Digital signal input (3 levels) that defines device status with pin 11.
16	I_T	High precision scaled transversal line current signal. $I_T = \frac{I_a + I_b}{100}$
17	I_L	Scaled longitudinal line current signal. $I_L = \frac{I_a - I_b}{100}$
19	RING	B line termination output with current capability up to 100mA (I_b is the current sunk into this pin).
2, 18	N.C.	Not connected.

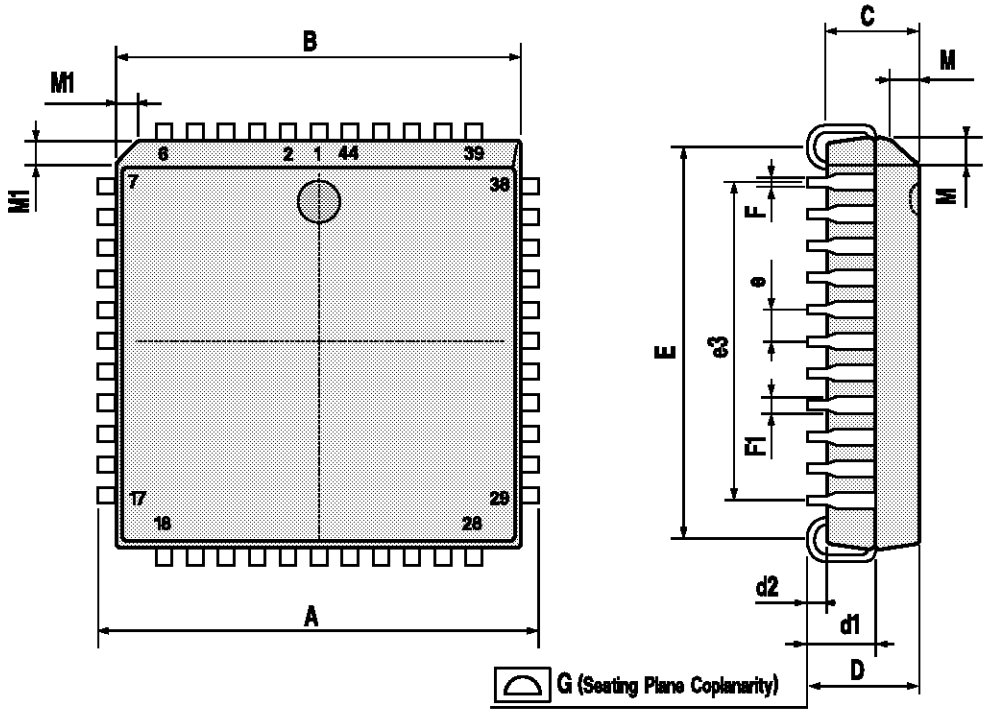
Notes: 1) All information relative to the PowerSO-20 package option should be considered as advanced information on a new product now in developement or undergoing evaluation. Details are subject to change without notice.

PIN DESCRIPTION (STLC3040)

PLCC44 N°	Symbol	Type	Description
1	DGND	ID	Digital Ground.
2	V_{CC}	ID	+5V Digital Supply.
3	FSC	ID	Frame sinc. 8KHz GCI Interface.
4	DCL	ID	Master data Clock GCI Interface.
5	DD	ID	Data Down link GCI Interface
6	DU	OD	Data Up link GCI Interface
7,8	IO1,IO2	I/OD	Programmable I/O GCI controlled
9	C1	OD	State control signal 1. Combination of C1 and C2 define L3000N operating mode.
10	C2	OD	State control signal 2.
11,12	VL1,VL2	IA	Comparator inputs. These are inputs of the comparator that senses the line voltage in Loop Open Mode allowing OFF/Hook detection in this mode.
13	SIR0	I/OD	Dedicated, leave open.
14	CAP	I/OA	Reversal. Proper Capacitor should be connected to this pin when soft battery reversal is needed.
15	IL	IA	Longitudinal Line Current input $I_L = \frac{I_a - I_b}{100}$
16	RAC	I/OA	AC Synthesis Reference Resistor.
17,18	STR0,STR1	I/OD	Dedicated, leave open.
19	IT	IA	Transversal Line Current input $I_T = \frac{I_a + I_b}{100}$
20	ACDC	I/OA	AC/DC Line split. Scaled line current output, DC feedback input.
21	CAC	I/OA	Split Capacitor. AC scaled line current input.
22	RDC	I/OA	DC Synthesis Reference Resistor.
23	REF	I/OA	Reference voltage output. A resistor connected to this pin is setting the internal reference current.
24	STR2	I/OD	Dedicated, leave open
25	VBIM	IA	Battery image monitor.
26	VOUT	OA	Two wire unbalanced output feeding the line voltage signals (DC, AC, RING, TTX) scaled by 40.
27	AGND	IA	Analog Ground.
28	PDO	OA	Power Down output. Proper bias current is provided to L3000N by this pin. When the current is 0 the L3000N goes in Power Down (high impedance).
29	EXT	ID	External Ring Sync. Input.
30	SIR1	I/OD	Dedicated, leave open.
31,32	IDL,IDM	IA	Line-card Identification, least valued bit.
33	V_S	IA	-5V Analog Supply.
34	V_{DD}	IA	+5V Analog Supply.
35	IDH	IA	Line-card Id, serial ID signature input.
36	MR	ID	Master reset Input. When connected to VCC the STLC3040 is forced in power down, all internal registers resetted.
37	SIR2	I/OD	Dedicated, leave open.
38	I1	ID	Digital input read via GCI
39	O1	OD	Digital output written via GCI.
40	SEL24	ID	Select Clock Frequency for GCI Interface 2MHz/4MHz, not affecting the data rate.
41,42,43	TS2,TS1,TS0	ID	GCI Select Time Slot Identifier Pins.
44	STR3	I/OD	Dedicated, leave open.

PLCC44 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045	



PowerSO-20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.60			0.1417
a1	0.10		0.30	0.0039		0.0118
a2			3.30			0.1299
a3	0		0.10	0		0.0039
b	0.40		0.53	0.0157		0.0209
c	0.23		0.32	0.009		0.0126
D (1)	15.80		16.00	0.6220		0.6299
E	13.90		14.50	0.5472		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.90		11.10	0.4291		0.437
E2			2.90			0.1141
G	0		0.10	0		0.0039
h			1.10			0.0433
L	0.80		1.10	0.0314		0.0433
N	10° (max.)					
S	8° (max.)					
T		10.0			0.3937	

(1) "D and E1" do not include mold flash or protrusions
- Mold flash or protrusions shall not exceed 0.15mm (0.006")