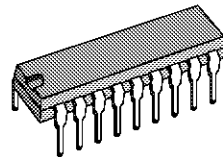


3.5A STEP DOWN SWITCHING REGULATOR

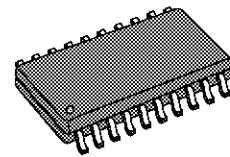
PRODUCT PREVIEW

- 3.5A STEP DOWN CONVERTER
- OPERATING INPUT VOLTAGE FROM 8V TO 55V
- 3.3V AND 5.1V (+/-2%) FIXED OUTPUT VOLTAGES
- OUTPUT VOLTAGE ADJUSTABLE FROM 3.3V TO 40V
- SWITCHING FREQUENCY IN EXCESS OF 200KHZ
- VOLTAGE FEED FORWARD
- ZERO LOAD CURRENT OPERATION
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V (1.5%) REFERENCE VOLTAGE
- INPUT/OUTPUT SYNCHRONIZATION FUNCTION
- INHIBIT FOR ZERO CURRENT CONSUMPTION
- PROTECTION AGAINST FEEDBACK DISCONNECTION
- THERMAL SHUTDOWN

MULTIPOWER BCD TECHNOLOGY



POWERDIP (12+3+3)



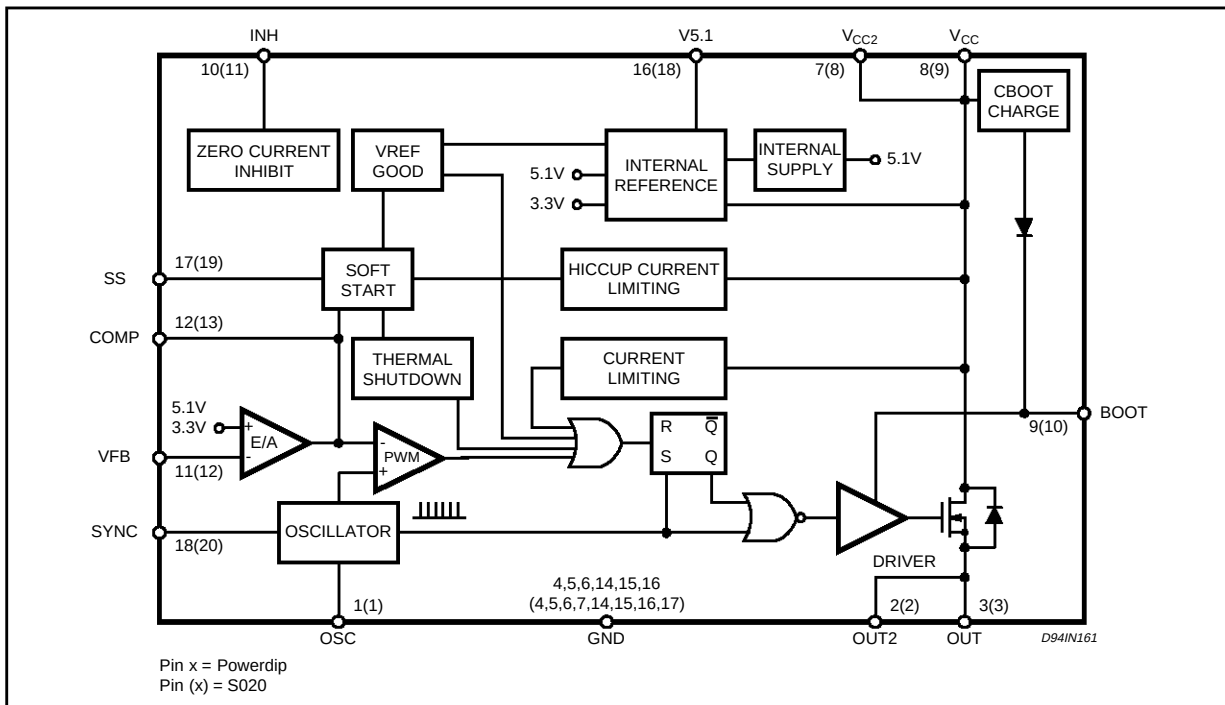
SO20

- SOFT START FUNCTION

DESCRIPTION

The L4973 is a step down monolithic power switching regulator delivering 3.5A at fixed voltages of 3.3V or 5.1V and using a simple external divider output adjustable voltage up to 40V.

BLOCK DIAGRAM



L4973V3 - L4973V5 - L4973D3 - L4973D5

Realized in BCD mixed technology, the device uses an internal power D-MOS transistor (with a typical $R_{ds(on)}$ of 0.15ohm) to obtain very high efficiency and very fast switching times.

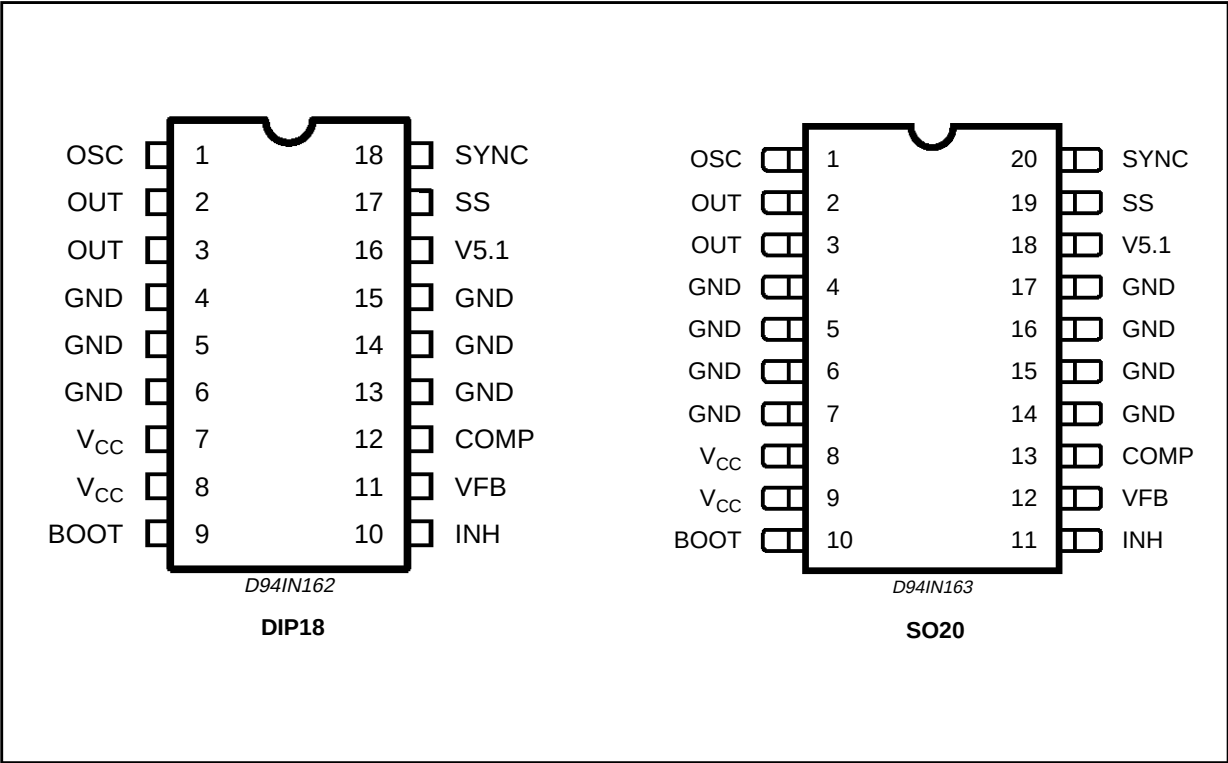
Switching frequency in excess of 200KHz are achievable (the maximum power dissipation of the packages must be observed).

A wide input voltage range between 8V to 55V and output voltages regulated from 3.3V to 40V cover the majority of the today applications.

Features of this new generation of DC-DC converter includes pulse by pulse current limit, hiccup mode for short circuit protection, voltage feed forward regulation, soft start, input/output synchronization, protection against feedback loop disconnection, inhibit for zero current consumption and thermal shutdown.

The proposed packages are in plastic dual in line, DIP-18 (12+3+3) for standard assembly, and SO20 (12+4+4) for SMD assembly.

PIN CONNECTIONS (Top view)



THERMAL DATA

Symbol	Parameter	DIP18	SO20	Unit
$R_{th(j-pin)}$	Thermal Resistance Junction to pin	Max. 12	15	°C/W
$R_{th(j-amb)}$	Thermal Resistance to Ambient	Max. 60 (*)	80 (*)	°C/W

(*) Package mounted on board.

ABSOLUTE MAXIMUM RATINGS

Symbol		Parameter		Value	Unit	
DIP-18	SO-20					
V ₇ ,V ₈	V ₉ ,V ₈	Input voltage		58	V	
V ₂ ,V ₃	V ₂ ,V ₃	Output DC voltage Otput peak voltage at t=0.1us f=200KHz		-1 -5	V V	
I ₂ ,I ₃	I ₂ ,I ₃	Maximum output current		int. limit.		
V ₉ -V ₈	V ₁₀ -V ₈			14	V	
V ₉	V ₁₀	Bootstrap voltage		70	V	
V ₁₁ ,V ₁₇	V ₁₂ ,V ₁₉	Analgos input voltage		14	V	
V ₁	V ₁			-0.3	V	
V ₁₂ ,V ₁₈	V ₁₃ ,V ₂₀			6	V	
				-0.3	V	
V ₁₀	V ₁₁			Vcc	V	
				-0.6	V	
P _{tot}		Power dissipation a Tpins ≤ 90°C		DIP-18	5	W
		(Tamb = 70°C no copper area)			1.3	W
		(Tamb = 70°C 4cm copper area on PCB)			2	W
		Power dissipation a Tpins = 90°C		SO-20L	4	W
T _J ,T _{STG}		Junction and storage temperature		-40 to 150		°C

PIN FUNCTIONS

PIN DIP-18	PIN SO-20	NAME	DESCRIPTION
11	12	COMP	E/A output to be used for frequency compensation
10	11	INH	A logic signal (active low) disables the device (sleep mode operation)
9	10	BOOT	A capacitor connected between this pin and the output allows to drive the internal D-MOS.
18	20	SYNC	Input/Output synchronization.
7,8	8,9	V _{cc}	Not regulated DC input voltage
2,3	2,3	OUT	Stepdown regulator output.
12	13	VFB	Stepdown feedback input. Connecting directly this pin to the output 3.3V and 5.1V are obtained; a voltage divider is requested for higher output voltages.
16	18	V5.1	Reference voltage externally available.
4,5,6 13,14,15	4,5,6,7 14,15,16,17	GND	Signal ground
1	1	OSC	An external resistor connected between the unregulated input voltage and Pin 1 and a capacitor connected from Pin 1 to ground fixes the switching frequency.(Line feed forward is automatically obtained)
17	19	SS	Soft start time constant. A capacitor connected between this terminal and ground determinates the soft start time.

L4973V3 - L4973V5 - L4973D3 - L4973D5

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_J = 25^\circ\text{C}$, $C_{\text{osc}} = 1.2\text{nF}$, $R_{\text{osc}} = 46.4\text{Kohm}$, $V_{\text{CC}} = 24\text{V}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS						
	Input Voltage range (*)	$V_o = 3.3\text{V to } 40\text{V}$ $I_o = 3.5\text{A}$	8		55	V
	Output Voltage	$I_o = 0.5\text{A to } 3.5\text{A}$ $V_{\text{CC}} = 8\text{V to } 55\text{V}$ $V_o = 5.1\text{V}$	5	5.1	5.2	V
		$I_o = 0.5\text{A to } 3.5\text{A}$ $V_{\text{CC}} = 8\text{V to } 55\text{V}$ $V_o = 3.3\text{V}$	3.234	3.3	3.366	V
	Dropout voltage	$V_{\text{CC}} = 8\text{V}$, $I_o = 3.5\text{A}$		0.56	0.77	V
	Maximum limiting current	$V_{\text{CC}} = 8\text{V to } 35\text{V}$ $V_{\text{CC}} = 24\text{V to } 55\text{V}$	4	4.5	5	A
η	efficiency	$V_o = 5.1\text{V}$, $I_o = 3.5\text{A}$		90		%
		$V_o = 3.3\text{V}$, $I_o = 3.5\text{A}$		85		%
	Switching frequency		90	100	110	KHz
	Maximum switching frequency (**)	$R_{\text{osc}} = 27\text{Kohm}$, $V_o = V_{\text{ref}}$, $I_o = 1\text{A}$ $C_{\text{osc}} = 1.2\text{nF}$	200			KHz
	Supply Voltage Ripple Rejection	$V_i = V_{\text{CC}} + 2\text{ VRMS}$ $V_o = V_{\text{ref}}$, $I_o = 1\text{A}$, $f_{\text{ripple}} = 100\text{Hz}$	60			dB
$\Delta f_{\text{sw}}/\Delta V_i$	Voltage stability of switching frequency	$V_{\text{CC}} = 8\text{V to } 55\text{V}$		2	5	%
$\Delta f_{\text{sw}}/\Delta T_j$	Temperat. stability of switching frequency	$T_j = 0^\circ \text{ to } 125^\circ\text{C}$		2		%
REFERENCE SECTION						
	Reference voltage		5.02	5.1	5.18	V
	Line regulation	$V_{\text{CC}} = 8\text{V to } 55\text{V}$ $I_{\text{ref}} = 0\text{ mA}$		5	10	mV
	Load regulation	$I_{\text{ref}} = 0\text{ to } 5\text{mA}$ $I_{\text{ref}} = 0\text{ to } 20\text{mA}$		2 6	10 25	mV mV
	Short circuit current		30	65	100	mA
	Reference voltage stability Vs temperature	$T_j = 0^\circ \text{ to } 125^\circ\text{C}$		0.4		mV/ $^\circ\text{C}$
SOFT START						
	Soft start charge current		30	40	50	μA
	Soft start discharge current		15	20	25	μA
INHIBIT (not compatible with the 3.3V)						
	High level voltage		3.5			V
	Low level voltage				0.9	V
	Isink High level	$3.5\text{V} < V_{\text{INH}} < 12\text{V}$		1		μA
		$V_{\text{INH}} < 0.9\text{V}$		1		μA
DC CHARACTERISTICS						
	Total operating quiescent current			4	8	mA
	Quiescent current	duty cycle = 0		2	3.5	mA
	Total stand by quiescent current	$V_{\text{CC}} = 24\text{V}$ $V_{\text{CC}} = 55\text{V}$, $V_{\text{INH}} < 0.9$		100 150	200 300	μA μA

(*) Pulse testing with a low duty cycle.

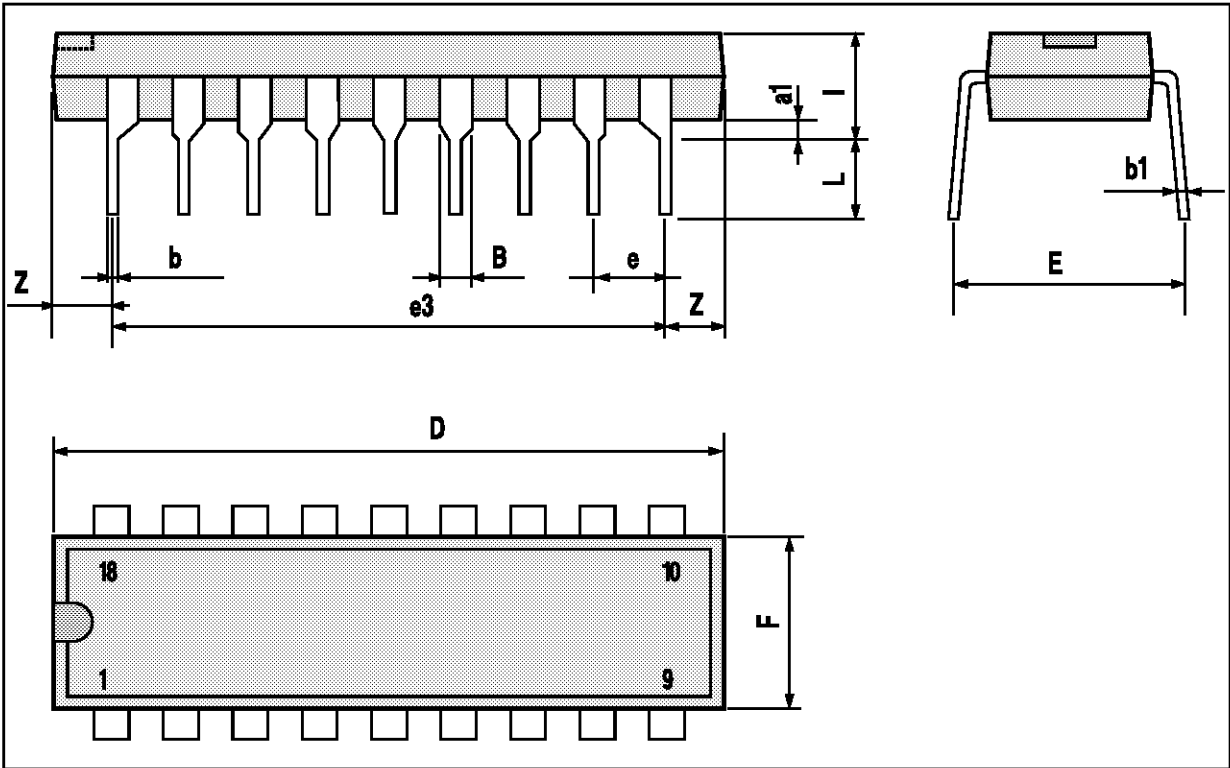
(**) The maximum power dissipation of the packages must be observed.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ERROR AMPLIFIER						
	High level output voltage		11.5			V
	Low level output Voltage				0.65	V
	Source output current		200	300		μ A
	Sink output current		200	300		μ A
	Supply voltage ripple rejection	$V_{COMP} = V_{FB}$ $V_{CC} = 8V$ to 55V	60	80		dB
	DC open loop gain		60			dB
OSCILLATOR SECTION						
	Ramp valley		0.78	0.85	0.92	V
	Ramp peak	$V_{CC} = 8V$	2.1	2.3	2.5	V
		$V_{CC} = 55V$	10	10.6	11.2	V
	Maximum duty cycle		95	97		%
SYNC FUNCTION						
	High input voltage	$V_{CC} = 8V$ to 55V	3.5			V
	Low input voltage	$V_{CC} = 8V$ to 55V			0.9	V
	Slave sink current			0.3	0.5	mA
	Master output amplitude	$I_{source} = 5mA$	4	4.5		V
	Output pulse width	no load, $V_{sync} = 3.5V$	0.15	0.25		μ s

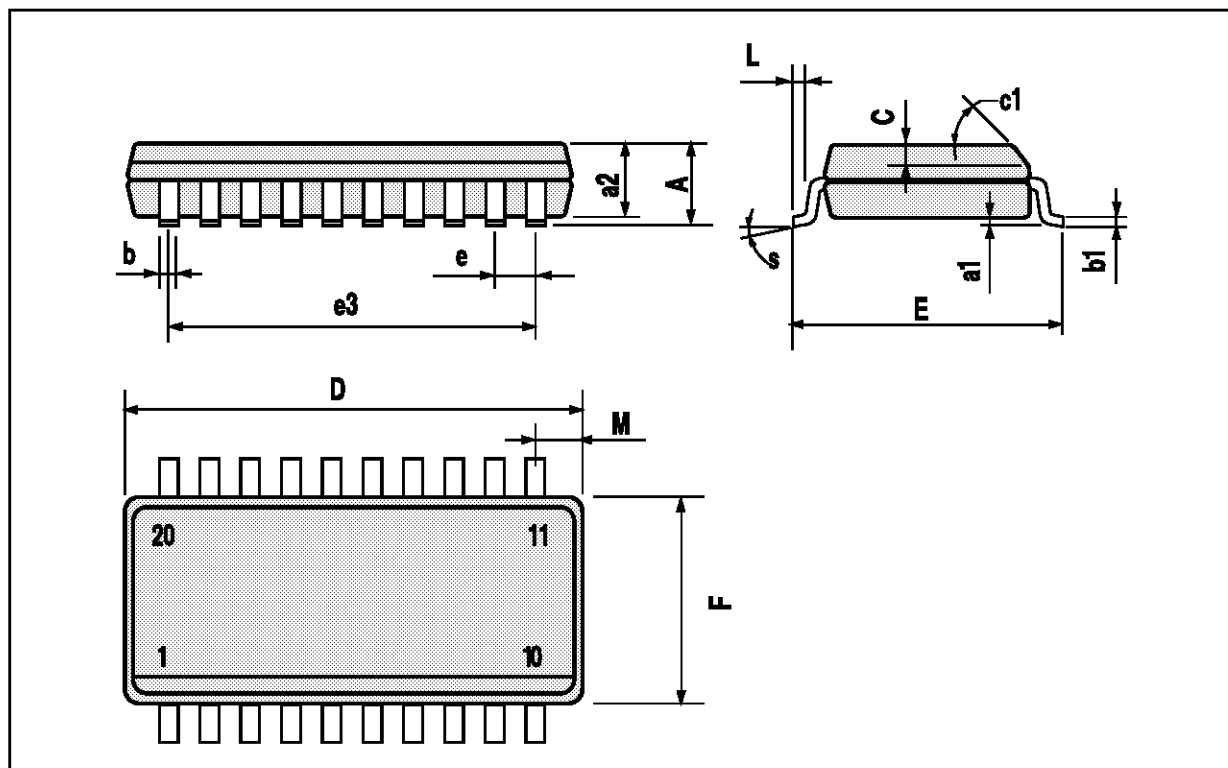
POWERDIP 18 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			24.80			0.976
E		8.80			0.346	
e		2.54			0.100	
e3		20.32			0.800	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			2.54			0.100



SO20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45 (typ.)					
D	12.6		13.0	0.496		0.512
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8 (max.)					



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