SGS-THOMSON MICROELECTRONICS

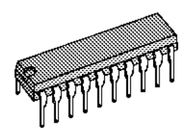
L4985

HIGH EFFICIENCY SWITCHING REGULATOR

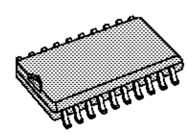
PRODUCT PREVIEW

- OPERATING INPUT VOLTAGE: FROM 4.5V TO 21V
- HIGH EFFICIENCY 3A STEP DOWN CONVERTER
  - 3A @ 3.3V OUTPUT VOLTAGE FROM 4.5V INPUT VOLTAGE
  - ADJUSTABLE OUTPUT VOLTAGE FROM 1.28V
  - GATE DRIVER FOR SYNCHRONOUS RECTIFICATION
  - 100% MAXIMUM DUTY CYCLE
  - INTERNAL CURRENT LIMIT
  - SOFT START, RESET SIGNAL, THERMAL SHUTDOWN
- AUXILIARY CONVERTER WITH 40V OPEN DRAIN SWITCH DELIVERING 5W @ V_{IN} = 12V
  - 1.7A PEAK CURRENT INTERNALLY LIMITED (TYP)
- POWER MANAGEMENT

MULTIPOWER BCD TECHNOLOGY



POWERDIP 16+2+2



SO20

ORDERING NUMBERS: L4985 (Powerdip)
L4985D (SO20)

DESCRIPTION

This high efficiency DC-DC converter is a monolithic device developed to generate all the voltages required in multioutputs DC-DC converters, in particular when the supply voltage is a battery, and isolation is not needed.

Designed to start to operate at an input voltage as low as 4.5V up to 21V, the device takes the advantages offered by our proprietary BCD Multipower technology to deliver 3A to the load on the stepdown section, and to manage 1.5A peak current on the open drain section.

The packages proposed are in plastic dual in line, Powerdip 20 (16+2+2) for standard assembly, and SO20L for SMD assembly.

This device is constitueed by two major sections: one section is a stepdown regulator, and the other one is a flexible regulator with open drain output DMOS transistor, source grounded, for flyback/forward topologies for multioutputs, or step-up topology when a single voltage higher than the supply one is requested.

Step Down Converter Section

The stepdown section, delivering to the load up to 3A current, at an output voltage adjustable from 1.28V up to 16V, works in voltage mode, fixed frequency, with no limitation on the max duty cycle.

This section has been designed to maximise the efficiency minimising the conduction losses and the quiescent current.

An internal step-up converter using a small chip inductor and a filter capacitor provides voltage and energy the gate driver of the internal N-channel DMOS transistor of 0.1Ω typ of R_{dson}, and the driver of an external DMOS transistor that should require no more than 30nC of gate charge, at 100KHz.

The gate driver pin can be left open if the use of a Schottky diode is preferred.

An internal pulse by pulse current limiting protects the device it self and the load from overload and short circuit conditions.

A reset block, monitoring the feedback voltage, with an programmable reset delay time, generates a reset signal for the microprocessor.
The reset output is an open drain.

Moreover, the DIS1 pin, active low, will inhibit the whole device, reducing to leakage only the current consumption from the battery.

Open Drain Converter Section

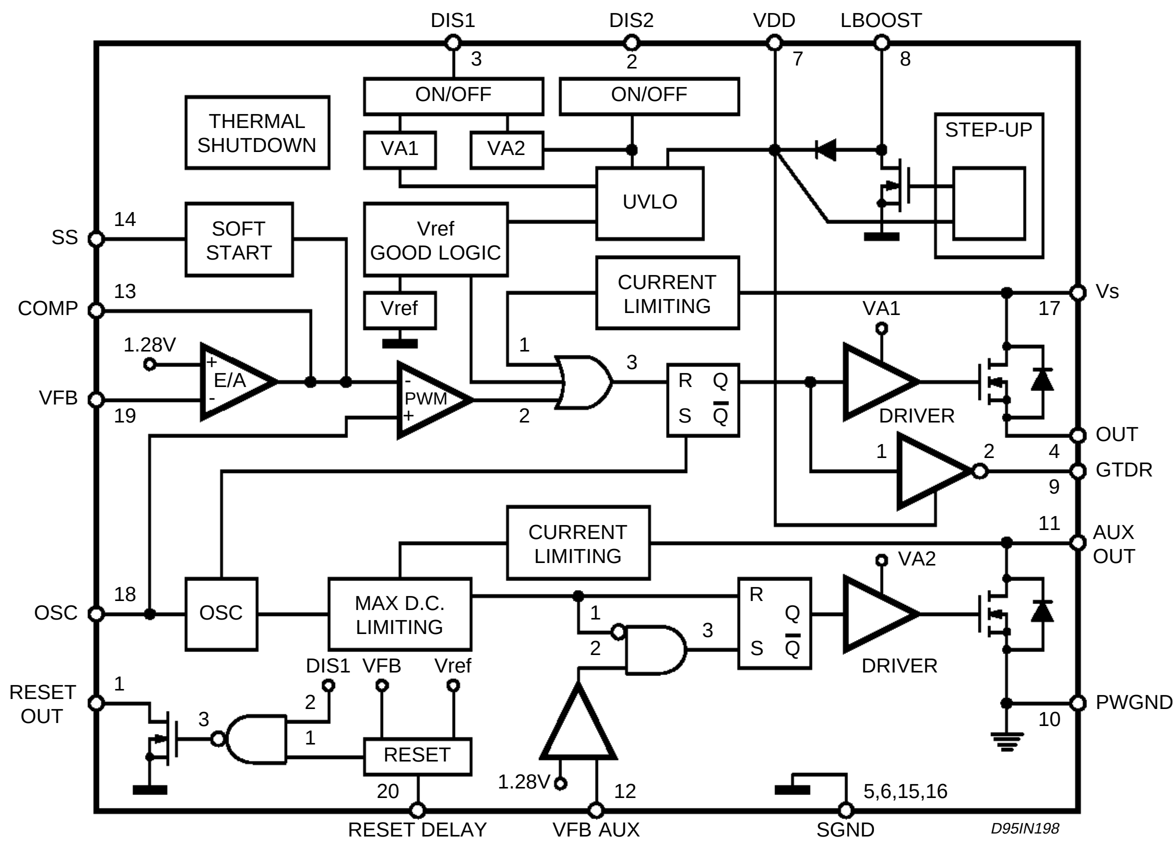
It's a low power converter, capable to deliver a global output power in excess of 5W @ V_{IN} = 12V.The max power delivered is depending on the supply voltage and on the topology used.

The open drain DMOS R_{dson} is 1Ω typ and a max voltage breakdown is 40V.

This section required few components just a voltage dueder to fix the output voltage.

DIS2 pin, when low, inhibits this section, reducing to zero the quiescent current consumption of this section.

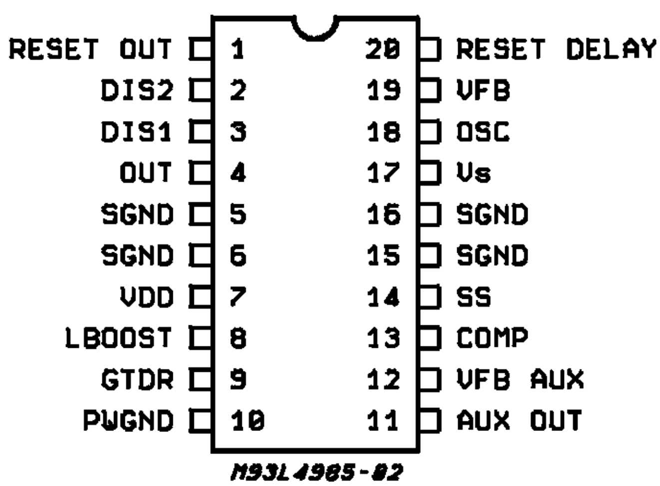
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Pins	Parameter	Value	Unit
V_S	17	Input Voltage	25	V
		Input Operating Voltage	20	V
$V_{AUX\ OUT}$	11	Auxiliary Drain Voltage	40	V
I_{OUT}	4	Maximum Output Current	internally limited	
$I_{AUX\ OUT}$	11	Maximum Auxiliary Output Current	internally limited	
DIS 1	3	Disable 1 Voltage	25	V
DIS 2	2	Disable 2 Voltage	25	V
R_{OUT}	1	Reset Output Voltage	25	V
	12,13,14,19	Analog Inputs	3.5	V
COMP	13	Sink Current	5	mA
SS	14	Soft start Sink Current	5	mA
OUT	4	Output Peak Voltage at 0.1µs f_{sw} = 100KHz	-2	V
GTDR	9	Output Gate Charge at f_{sw} = 100KHz	30	nC
V_{DD}	7	Step-up Output Voltage	V_{CC} +14V	V
LBOOST	8	Step-up Input Voltage	V_{CC} +14V	V
P_{TOT}		Power Dissipation at T_{amb} < 70°C (PDIP 20)	1.3	W
		Power Dissipation at T_{amb} < 70°C (SO 20L)	1	W
T_j ,T_{stg}		Junction and Storage Temperature	-40 to 150	°C

PIN CONNECTION



THERMAL DATA

Symbol	Parameter		PDIP 20	SO 20	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction Ambient	max	60	80	°C/W

PIN FUNCTIONS

N.	Name	Function
1	RESET OUT	Open drain reset output. The output is high when the stepdown output voltage is nominal
2	DIS 2	A signal (active low) disables only the auxiliary DC-DC converter.
3	DIS 1	A signal (active low) disables the device (sleep mode operation)
4	OUT	Stepdown regulator output
5, 6, 15, 16	SGND	Signal Ground
7	V_{DD}	Regulated step-up output. This output can deliver also 1mA for external function.
8	LBOOST	Step-up open drain, to be connected to the chip inductor.
9	GTDR	Synchronous gate driver for external power MOS
10	PWGND	Power ground
11	AUX OUT	Auxiliary output, open drain converter for boost or flyback / forward topologies
12	VFB AUX	Feedback of the auxiliary DC-DC converter
13	COMP	E/A output to be used for frequency compensation
14	SS	Soft start time constant. A capacitor connected between this pin and ground determinates the soft start time.
17	V_S	Input supply voltage
18	OSC	An external capacitor connected between this pin and ground fixes the switching frequency.
19	VFB	Stepdown feedback input . It is directly connected to the output for 1.28V; a voltage divider is requested for higher output voltages.
20	RESET DELAY	Connecting a capacitor between this terminal and ground,a delay time reset is fixed.

ELECTRICAL CHARACTERISTICS (V_{17} = 12V; T_j = 25°C; C_{osc} = 560pF;unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS						
V_I	Input Voltage Range	I_O = 3A; V_O = V_{REF}	4.5		20	V
V_O	Output Voltage Range	I_O = 3A; V_S = 18V	V_{REF}		16	V
f_{SW}	Switching Frequency		73	83	93	KHz
V_{19}	Feedback Voltage	I_O = 0.5A	1.254	1.28	1.306	V
V_L	Line and Load Regulation on Feedback Voltage	V_{17} = 5 to 18V; I_O = 0.5 to 3A; V_O = V_{REF}	1.242	1.28	1.318	V
V_{17} - V_4	Dropout Voltage	I_O = 3A		0.3	0.4	V
		I_O = 3A 0 < T_j < 125°C		0.45	0.6	V
n	Efficiency	V_O = 5V; I_O = 3A DIS 2 = LOW; DIS 1 = HIGH		85		%
I_4	Max Limiting Current	V_{17} = 8 to 18V; V_O = 5V	3.75	4.25	4.75	A
$\delta f_{SW} / \delta V_S$	Voltage Stability of Switching Frequency	V_{17} = 5 to 18V		1	2	%
$\delta f_{SW} / \delta T_j$	Temperature Stability of Switching Frequency	T_j = 0 to 70°C		4	6	%
GTDR GATE DRIVER OUTPUT						
V_9	Output Low Level	I_{SINK} = 10mA		0.26	0.5	V
		I_{SINK} = 30mA		1	2	V
V_9	Output High Level	I_{SOURCE} = 3mA	8.3	10		V
		I_{SOURCE} = 10mA	8.3	9.5		V
t_r	Rise Time	C_L = 1nF		70	100	ns
t_f	Fall Ttime	C_L = 1nF		70	100	ns

ELECTRICAL CHARACTERISTICS (V_{17} = 12V; T_j = 25°C; C_{osc} = 560pF;unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
AUXILIARY OUTPUT SECTION						
V_{11} - V_{10}	Dropout Voltage	I_{O2} = 0.5A		0.5	0.8	V
		I_{O2} = 0.5A; 0 ≤ T_j ≤ 125°C		0.8	1.3	V
I_{11}	Maximum Limiting Current		1.2	1.7	2.2	A
V_{12}	Internal Reference Voltage	V_{O2} = 24V; I_{O2} = 50mA	1.244	1.28	1.316	V
RESET FUNCTION						
V_1	Output Saturation Voltage	I_1 = 10mA			0.4	V
I_{20}	Delay Source Current		6	9	12	µA
V_{dH}	Delay High Level Threshold Vol.			2.5		V
V_{dL}	Delay Low Level Threshold Vol.			0.4		V
V_{tr}	Rising Threshold Voltage			V_{REF} -70mV		V
V_{tf}	Falling Threshold Voltage			V_{REF} -210mV		V
I_1	Leakage Current				50	µA
SOFT START						
I_{14}	Soft Start Source Current		45	55	65	µA
V_{14}	Output Saturation Voltage	I_{SINK} = 3mA		0.5		V
DISABLE (1&2) FUNCTION						
V_{HL}	High Level Voltage		3			V
V_{LL}	Low Level Voltage				0.9	V
$I_{SINK\ H}$	I_{SINK} High Level			10	90	µA
$I_{SINK\ L}$	I_{SINK} Low Level			1		µA
DC CHARACTERISTICS						
I_{17}	Total Quiescent Current	V_{19} = 1.5V V_{17} = 20V DIS1 = DIS2 = HIGH		3.5	7	mA
I_4	Output Leakage Current	V_{17} = 20V; DIS 1 = LOW; DIS2		10	80	µA
I_{11}	Auxiliary Output Leakage Current	V_{11} = 40V; DIS 2 = LOW		20	100	µA
I_{17}	Quiescent Current	V_{17} = 20V; V_{19} = 1.5V DIS 2 = LOW DIS1 = HIGH DIS 1 = LOW DIS2		 3 70	 5 150	 mA µA
ERROR AMPLIFIER						
V_{OH}	High Level Output Voltage	I_{13} = 0.5mA; V_{19} = 1.2V	2.4	2.8		V
V_{OL}	Low Level Output Voltage	I_{13} = 1mA; V_{19} = 1.35V		0.15	0.3	V
G_v	Unit Gain Bandwith			1.5		MHz
I_b	Input Bias Current			0.5	2	µA
G_{DC}	DC Open Loop Gain			80		dB
OSCILLATOR SECTION						
V_{18}	Ramp Valley		0.5	0.63	0.76	V
V_{18}	Ramp Peak		1.9	2	2.1	V
I_{sink}	Sink Current			3.2		mA
I_{SOURCE}	Source Current			60		µA

Figure 1: Dropout voltage between Pin 17 and Pin 4 vs. output current (step down converter.

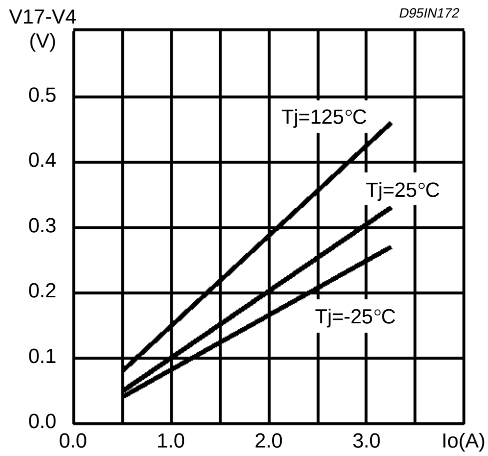


Figure 2: Dropout voltage between Pin 17 and Pin 4 vs. Junction Temperature

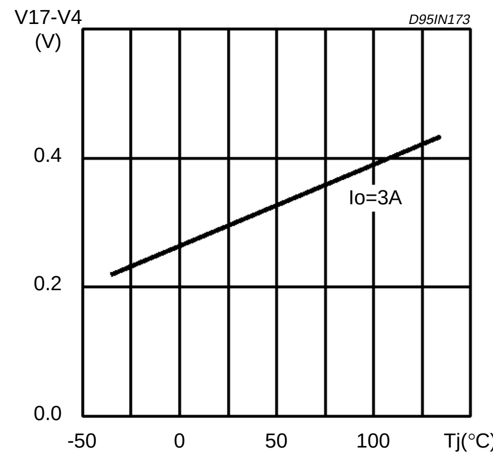


Figure 3: Dropout voltage between Pin 11 and Pin 10 vs. switch output current (auxiliary converter)

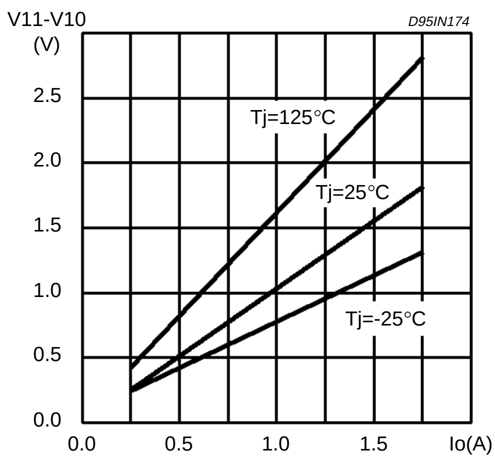


Figure 4: Dropout voltage between Pin 11 and Pin 10 vs. Junction Temperature

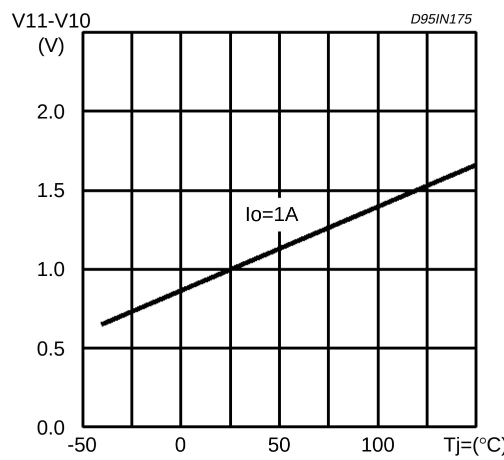


Figure 5: Power dissipation (device only) vs. supply voltage (refer to test circuit of fig.29 with D1 = SB540, Pin 9 = open)

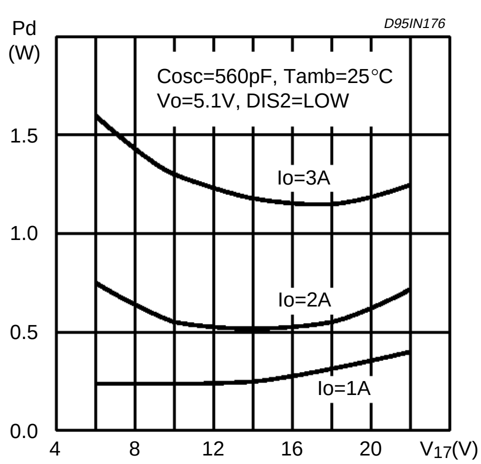


Figure 6: Power dissipation (device only) vs. supply voltage (see test circuit fig. 28, with D1 = SB540, pin 9 open

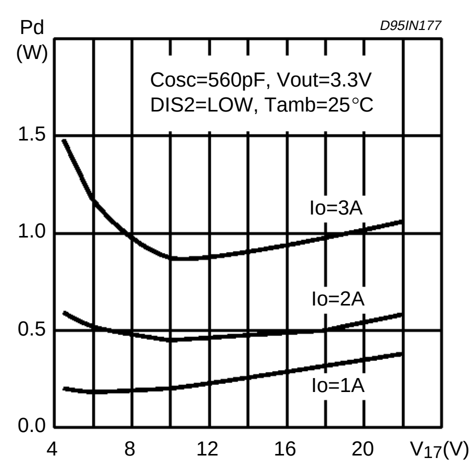


Figure 7: Power dissipation (device only) vs. output current (see test circuit fig. 28/29 with D1 = SB540, pin 9 open).

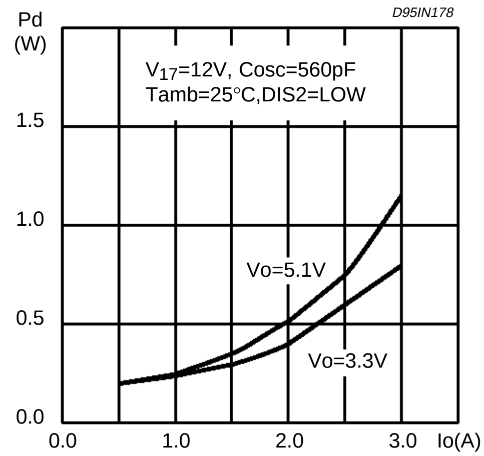


Figure 8: Current consumpion vs. junction temperature.

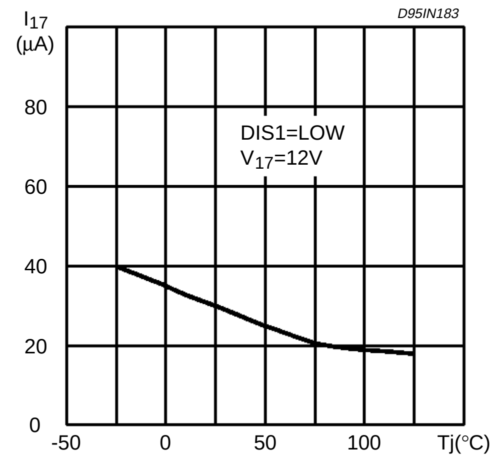


Figure 9: Quiescent current vs. supply voltage.

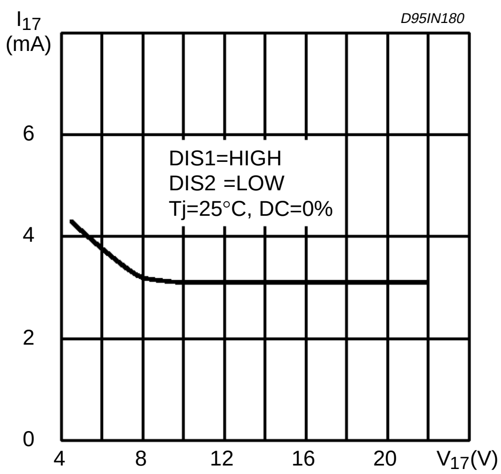


Figure 10: Quiescent current vs. supply voltage.

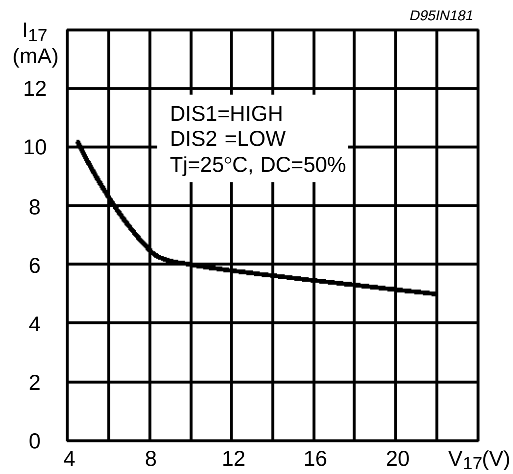


Figure 11: Quiescent current vs. junction temperature

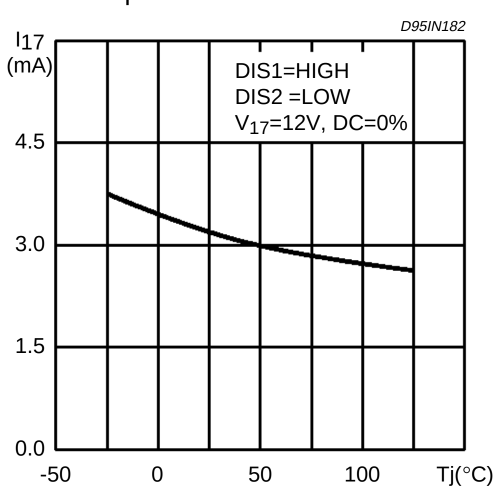


Figure 12: Current consumption vs. supply voltage

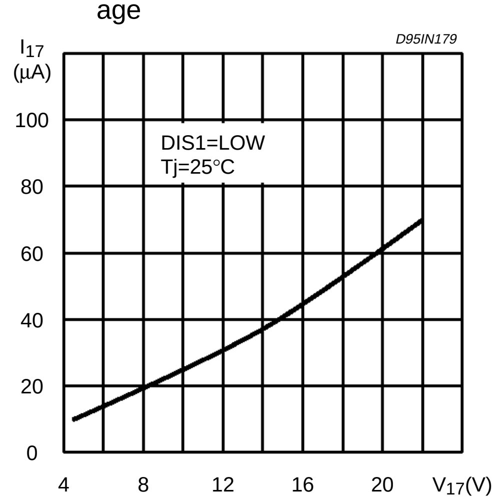


Figure 13: Oscillator frequency vs. supply voltage

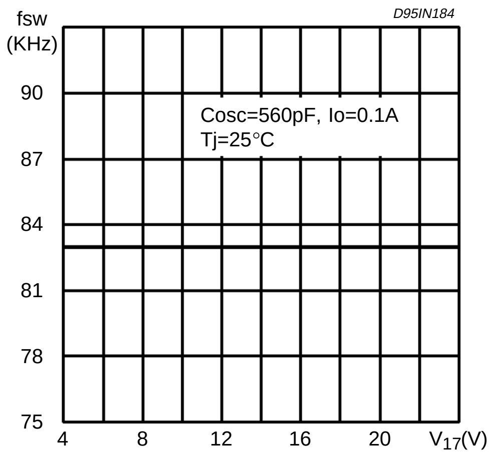


Figure 14: Oscillator frequency vs. temperature

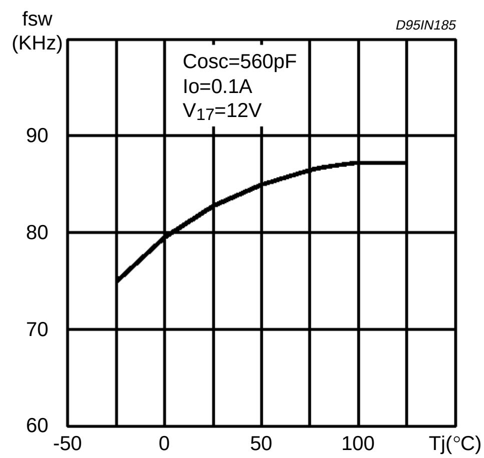


Figure 15: Reference voltage (pin 19) line regulation

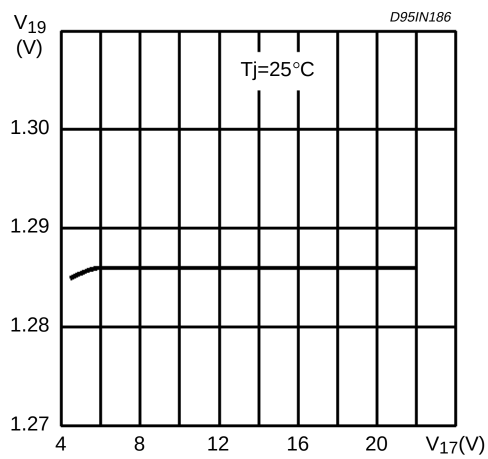


Figure 16: Reference voltage (pin 19) vs junction temperature

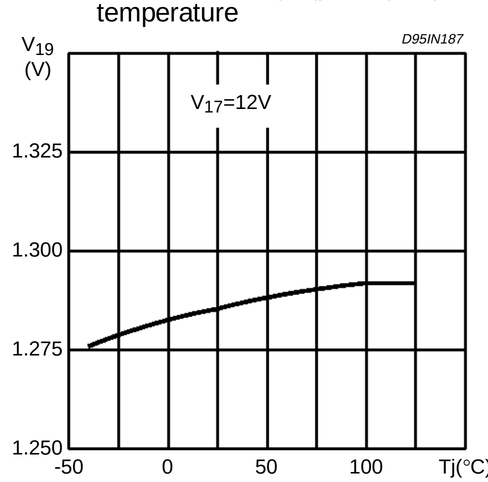


Figure 17: Open loop frequency and phase response of error amplifier

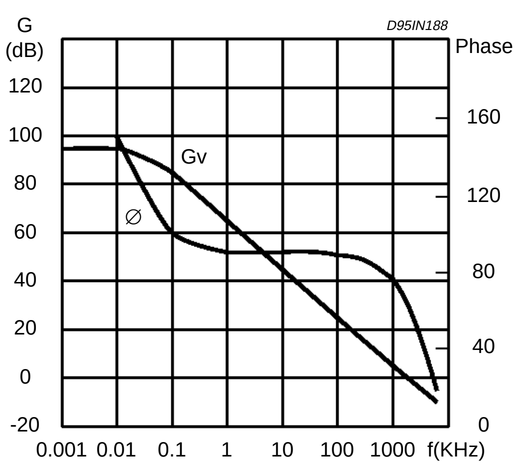


Figure 18: Supply voltage ripple rejection vs. frequency (from input to output voltage, test circuit of fig. 28 with D1 = SB540, pin 9 = Open)

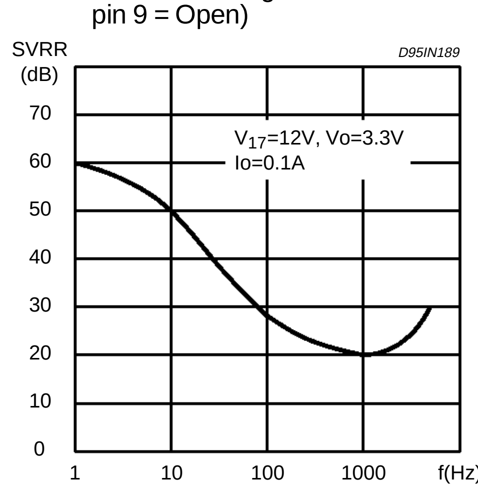


Figure 19: Switching frequency vs. Cosc

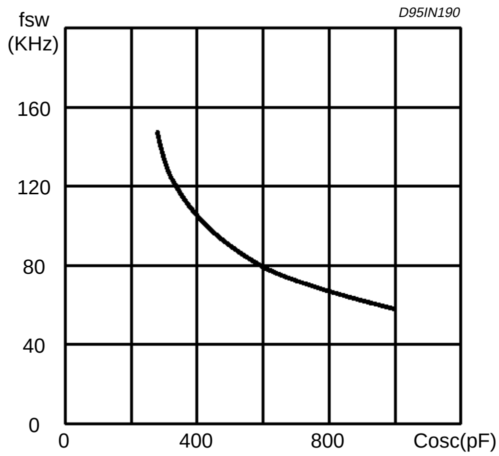


Figure 20: Evaluation board efficiency of (Ref fig. 29) with synchronous rectifier

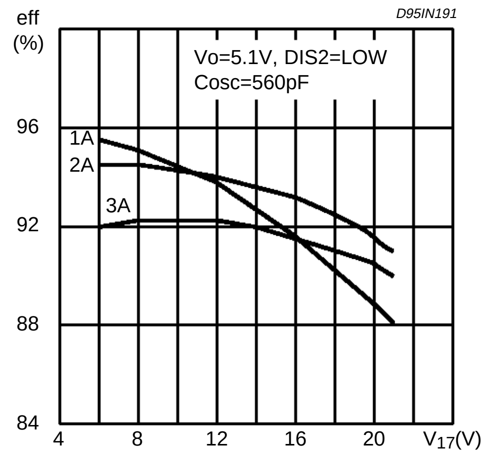


Figure 21: Evaluation board efficiency (Ref. fig. 25) with synchronous rectifier [V_{01} = 5V, V_{02} = 24V]

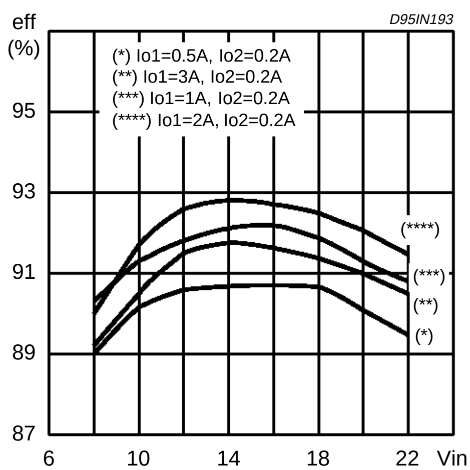


Figure 22: Evaluation board efficiency (Ref. fig. 28) with synchronous rectifier

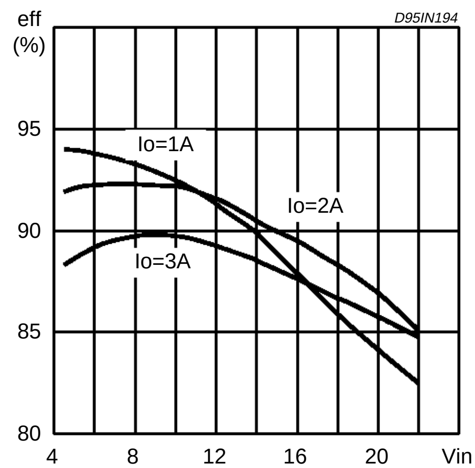


Figure 23: Evaluation board efficiency (Ref fig.28) with D1 = SB540 and pin9 open.

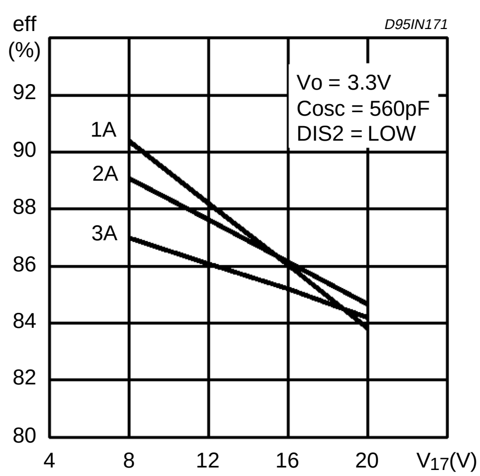
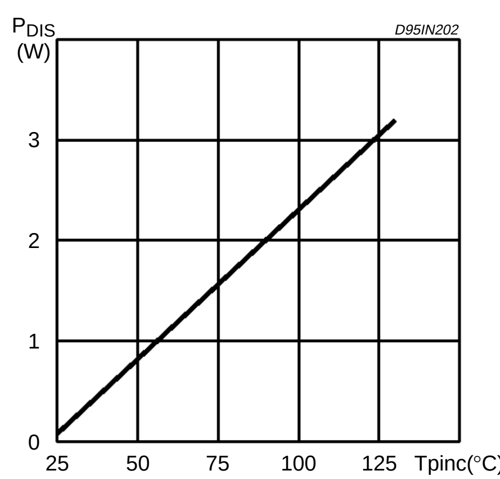
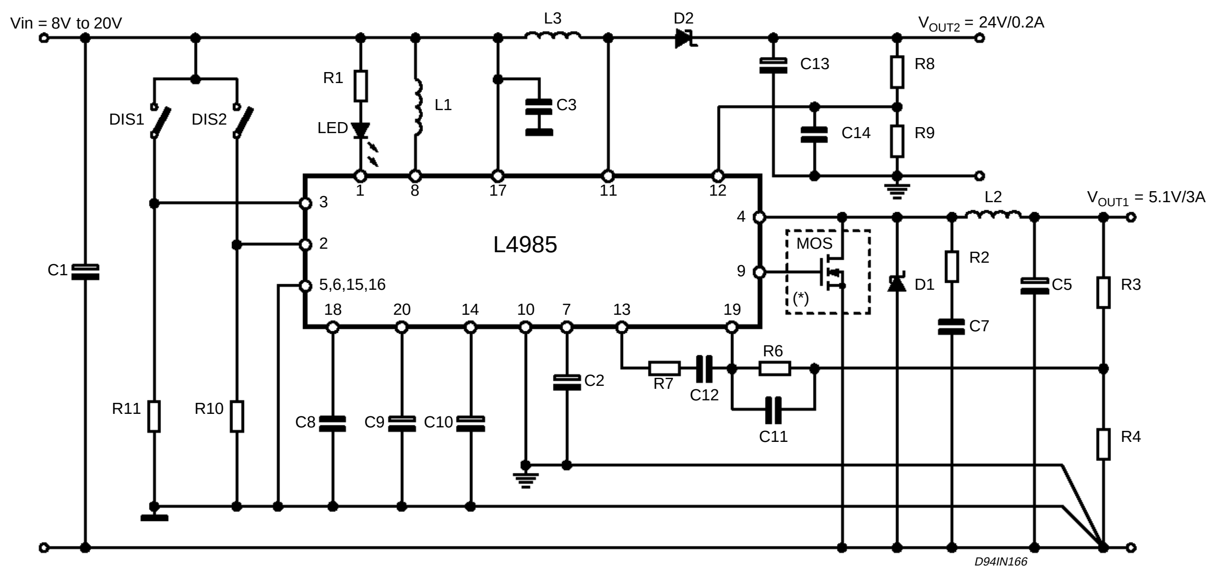


Figure 24: PCB thermal characteristic



APPLICATION INFORMATION

Figure 25: Dual converter evaluation board circuit (Fig.: 26-27)



C1 = 560µF / 25V NCC LXF
C2 = 10µF / 50V
C3 = 330nF film
C5 = 220µF / 10V SANYO OS CON
C7 = 2.2nF film
C8 = 560pF multilayer
C9 = C10 = 2.2µF / 10V
C11 = 3.9nF
C12 = 5.6nF
C13 = 330µF / 35V NCC LXF
C14 = 22nF

R1 = 3.3kΩ
R2 = 4.7Ω
R3 = 8.2kΩ
R4 = 2.7kΩ
R6 = 56kΩ
R7 = 39kΩ
R8 = 47kΩ
R9 = 2.7kΩ
R10 = 10kΩ
R11 = 10kΩ

L1 = 180µH axial
L2 = 50µH (Core Magnetics 58120, 27 turns, 0.8mm)
L3 = 50µH (Core Magnetics 58050, 27 turns, 0.6mm)

D2 = ST BYV 10 - 40
D1 = SB540
PIN 9 = OPEN
(*) OPTIONAL:
D1 = STBYV 10-40 AND
MOS = DY9410 SILICONIX

Table 1: Evaluation board test circuit results (using synchronous rectifier).

Symbol	Parameter	Test Condition	Value	Unit
η	Efficiency	V_{in} = 14V; DIS 2 = HIGH; I_{out1} = 1A; I_{out2} = 0.2A;	92.0	%
		V_{in} = 14V; DIS 2 = HIGH; I_{out1} = 3A; I_{out2} = 0.2A;	91.8	%
ΔV_{out1}	Line Regulation	V_{in} = 8 to 21V; DIS 2 = HIGH I_{out1} = 0.5A; I_{out2} = 20mA;	4	mV
ΔV_{out1}	Load Regulation	V_{in} = 8 to 21V; DIS 2 = HIGH I_{out1} = 0.5 to 3A ; I_{out2} = 0.2A	10	mV
ΔV_{out2}	Line Regulation	V_{in} = 8 to 21V; DIS 2 = HIGH I_{out1} = 0.5A; I_{out2} = 20mA;	50	mV
ΔV_{out2}	Load Regulation	V_{in} = 8 to 21V; DIS 2 = HIGH I_{out1} = 0.5 to 3A ; I_{out2} = 0.2A	300	mV

Figure 26: PC Board (Component Side) and Components Layout of fig. 25 (scale 1:1)

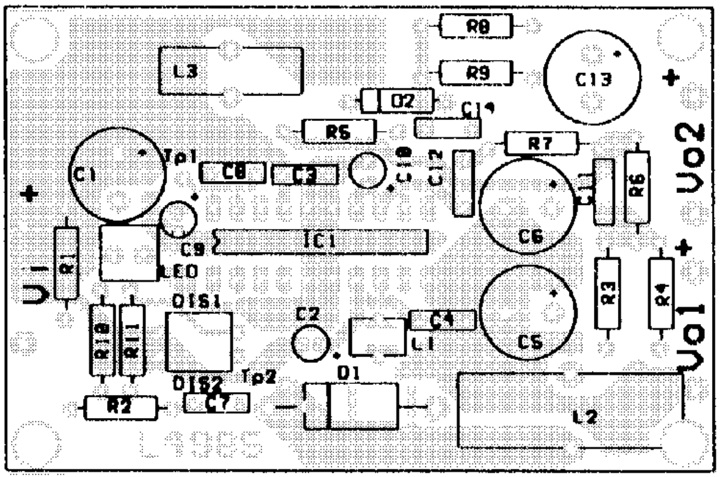


Figure 27: PC Board (Back Side) and Components Layout of fig. 25 (scale 1:1)

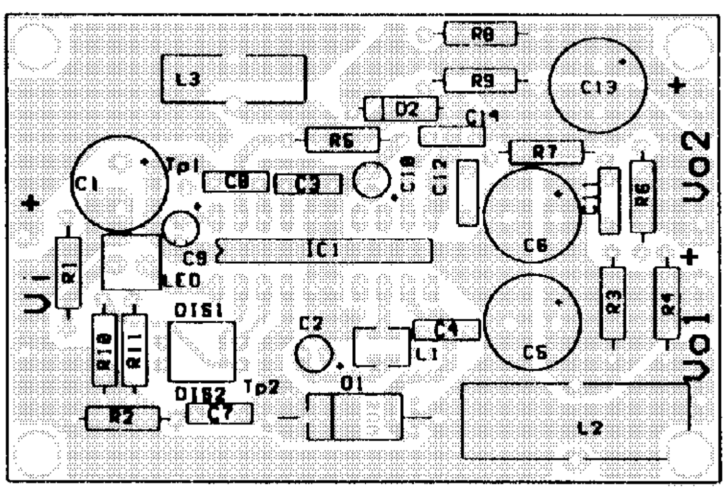


Figure 28: L4985 single output: evaluation board circuit.

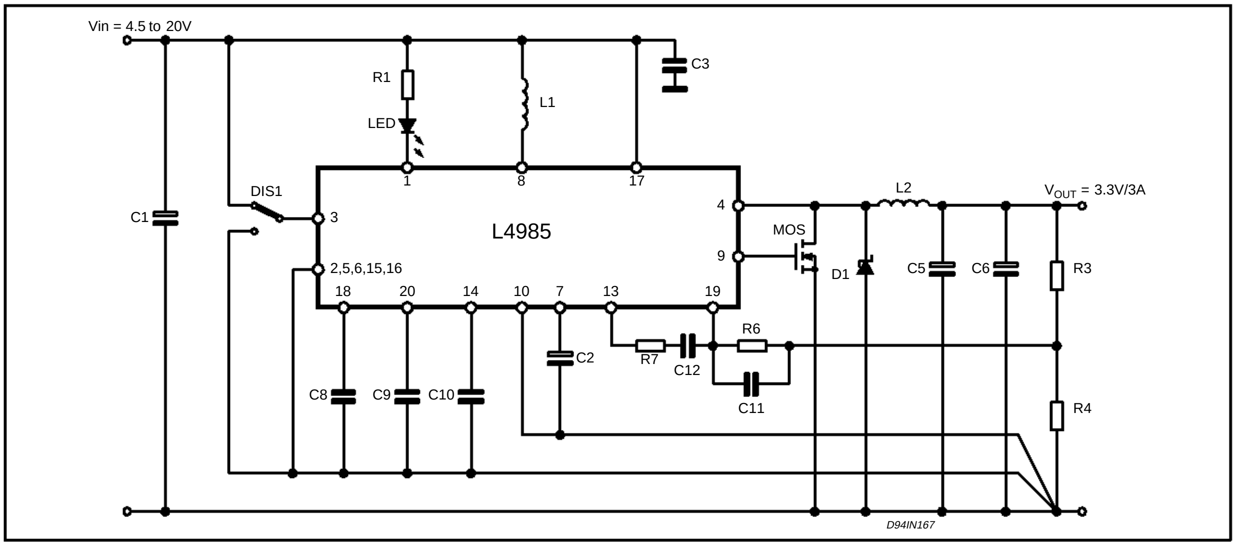
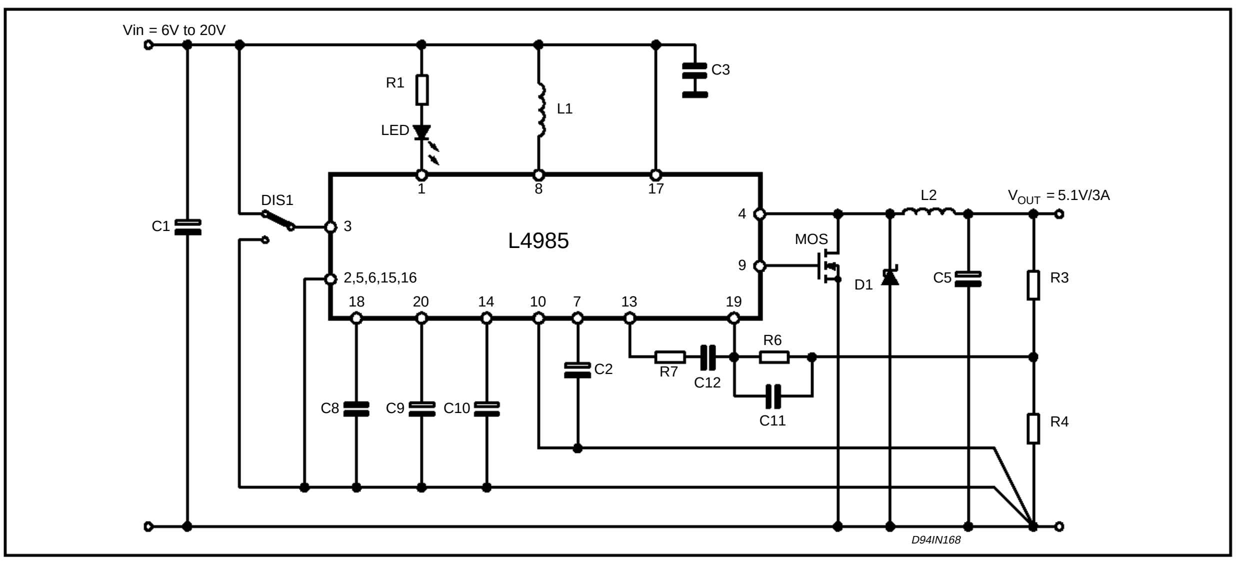


Figure 29: L4985 single output: evaluation board circuit (**).



C1 = 470µF / 25V NCC LXF
C2 = 10µF / 50V
C3 = 330nF film
C5 = C6 = 220µF / 10V SANYO OS-CON
C8 = 560pF multilayer
C9 = C10 = 2.2µF / 10V
C11 = 4.7nF (3.9nF **)
C12 = 8.2nF (5.6nF **)

R1 = 3.3kΩ
R3 = 3.9kΩ (8.2kΩ **)
R4 = 2.4kΩ (27kΩ **)
R6 = 56kΩ
R7 = 33kΩ (39kΩ **)

L1 = 180µH axial
L2 = 45µH (Core Magnetics 58120, 24 turns, 0.9mm PCB copper thickness 70mm)
[L2 = 50µH (Core Magnetics - 27 turns, 0.8mm) PCB copper thickness 70mm **]
D1 = SB540 (pin 9 open)
(*) OPTIONAL: D1 = ST BYV 10 - 40
MOS = DY9410 SILICONIX

Table 2: Step down converter using synchronous rectifier evaluation results.

Symbol	Parameter	Test Condition	Value	Unit
η	Efficiency	V_{in} = 5V; I_{out} = 1A ; V_{out} = 3.3V	94.0	%
		V_{in} = 5V; I_{out} = 3A ; V_{out} = 3.3V	89.1	%
ΔV_{out}	Line Regulation	V_{in} = 4.5 to 21V; I_{out} = 0.5A	2.0	mV
ΔV_{out}	Load Regulation	V_{in} = 4.5 to 21V; I_{out} = 0.5 to 3A	5.0	mV

Figure 30: PC Board (Component Side) and Components Layout of Fig. 28 (scale 1:1)

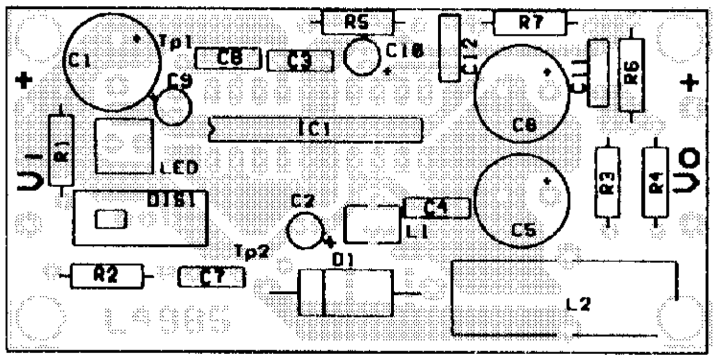


Figure 31: PC Board (Back Side) and Components Layout of Fig. 28 (scale 1:1)

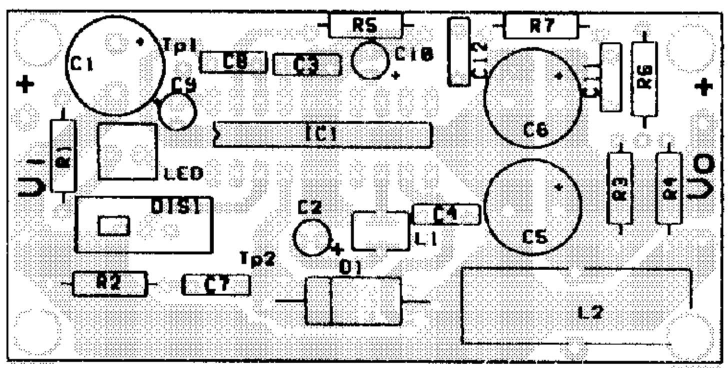


Figure 32: L4985 single output: Minimum external component count.

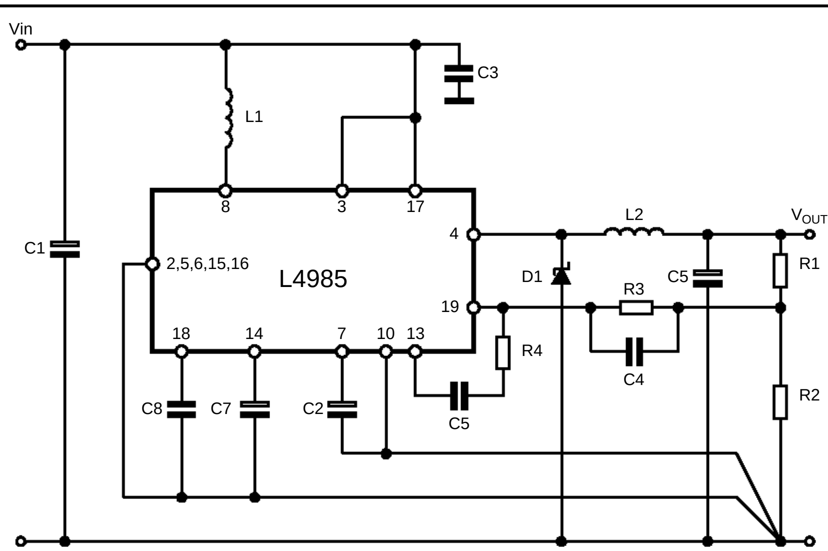
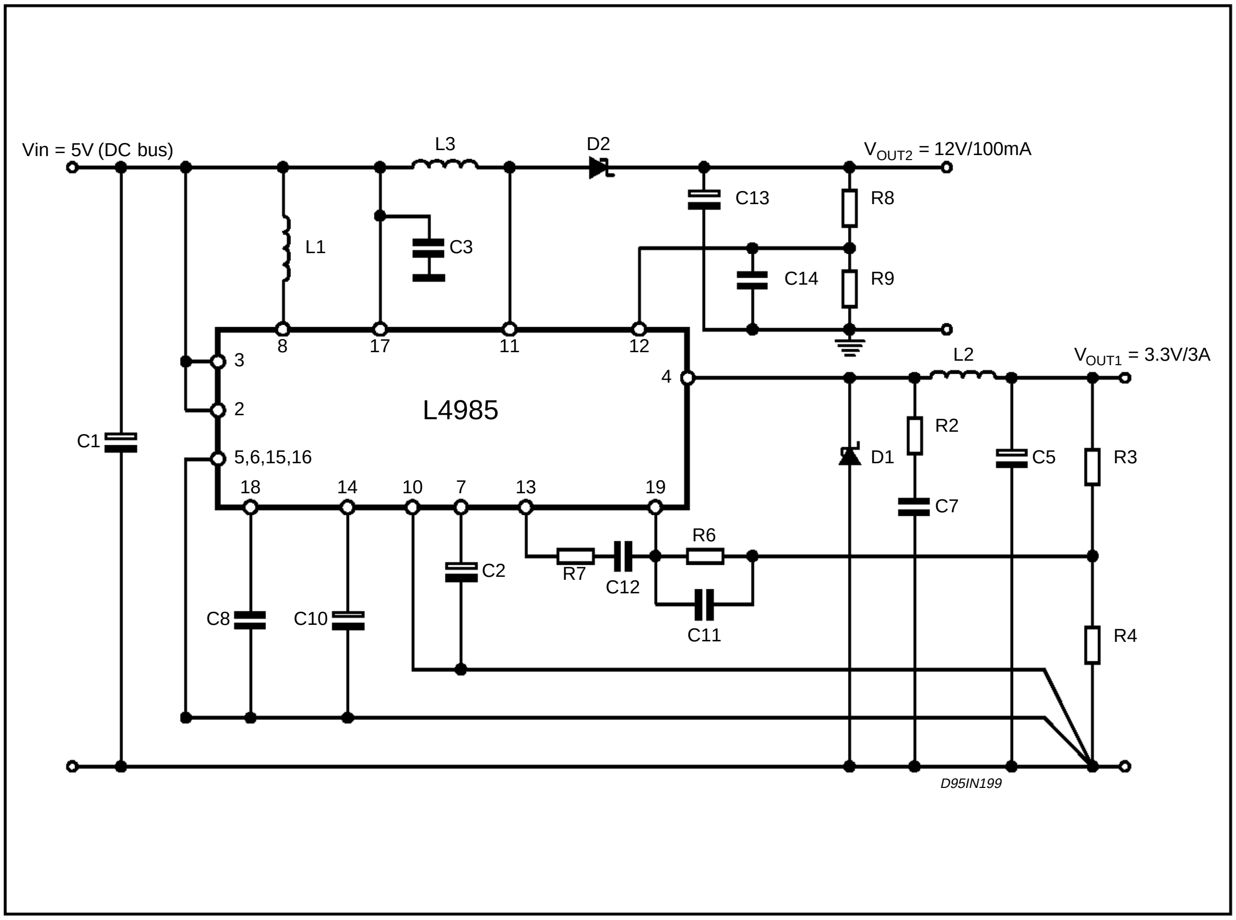
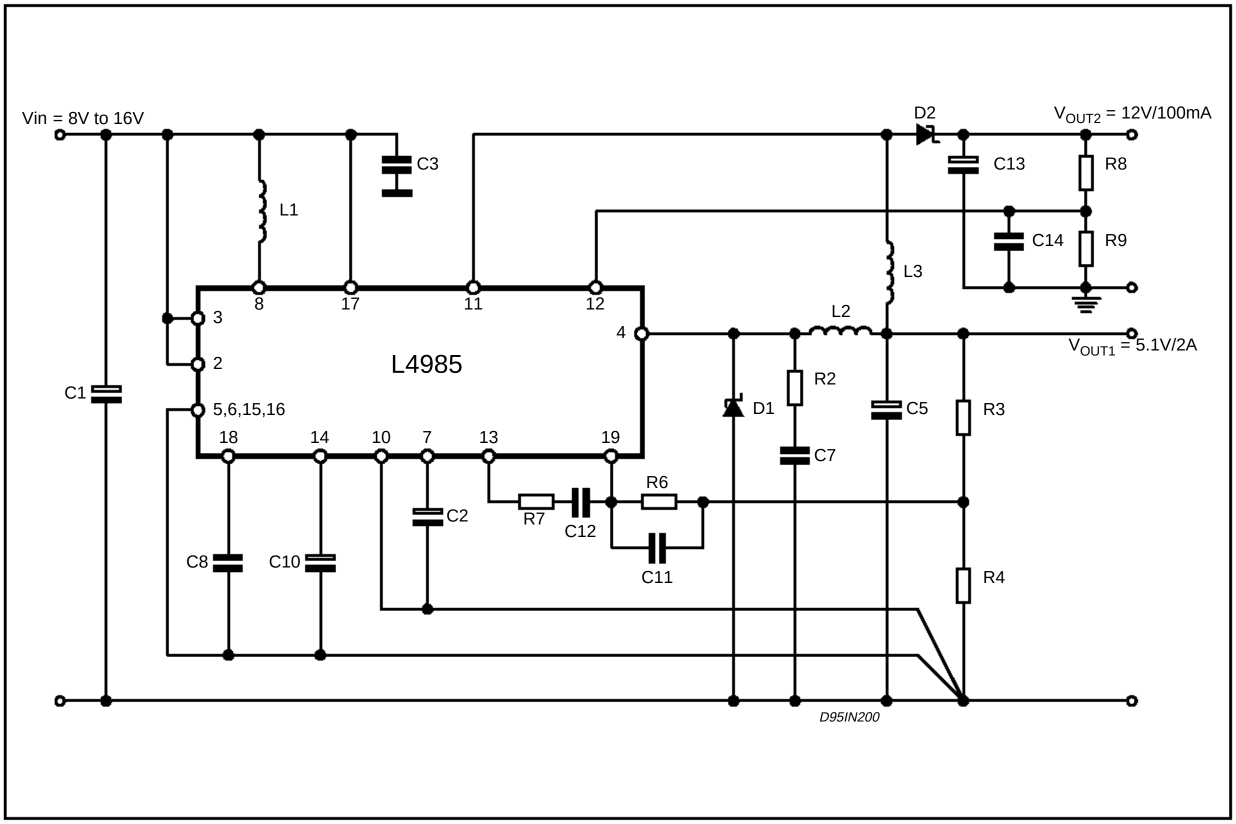


Figure 33 : Single chip converter generates 3.3V/3A for logic and 12V/100mA (flash eprom) from 5V bus



C1 = 560µF / 25V NCC LXF	R1 = 3.3kΩ	L1 = 180µH axial
C2 = 10µF / 50V	R2 = 4.7Ω	L2 = 20µH (Core Magnetics 55050, 19 turns, 0.8mm)
C3 = 330nF film	R3 = 3.9kΩ	
C5 = 220µF / 10V SANYO OS CON (2x220µF)	R4 = 2.4kΩ	L3 = 15µH (Core Magnetics 58080, 16 turns, 0.6mm)
C7 = 2.2nF film	R6 = 56kΩ	
C8 = 560pF multilayer	R7 = 33kΩ	
C9 = C10 = 2.2µF / 10V	R8 = 27kΩ	D2 = ST BYV 10 - 40
C11 = 4.7nF	R9 = 2.7kΩ	D1 = SB540
C12 = 8.2nF	R10 = 10kΩ	PIN 9 = OPEN
C13 = 330µF / 25V NCC LXF	R11 = 10kΩ	
C14 = 22nF		

Figure 34 : Single chip converter generates 5V/2A for logic and 12V /100mA for flash eprom

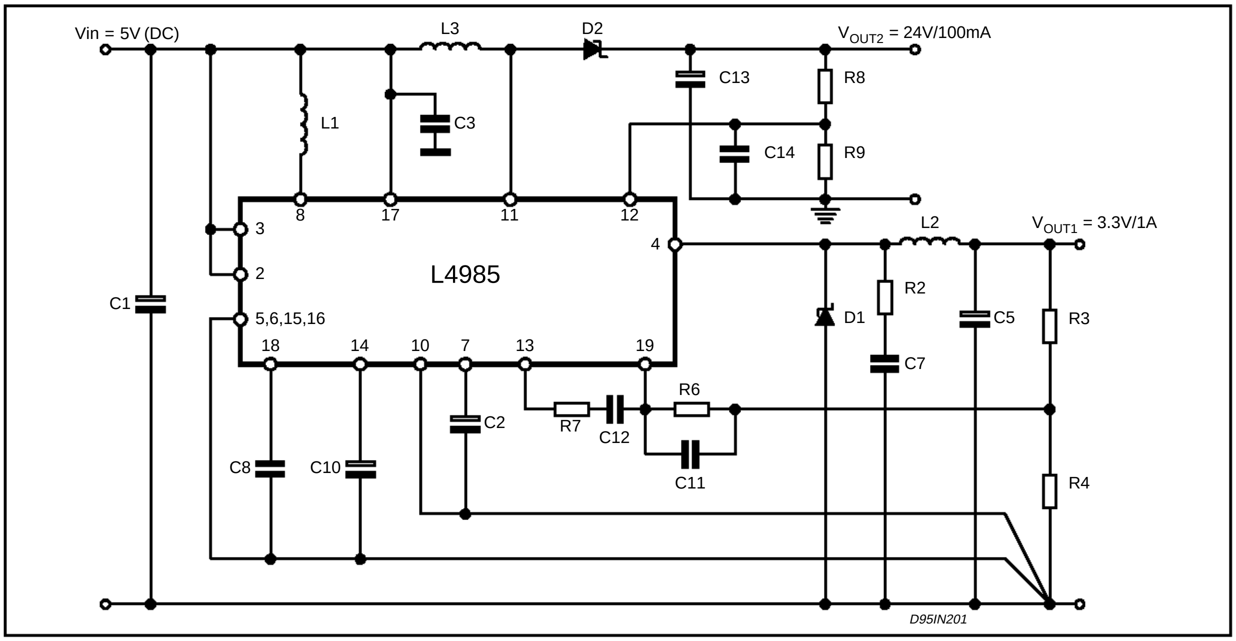


C1 = 560µF / 25V NCC LXF
C2 = 10µF / 50V
C3 = 330nF film
C5 = 220µF / 10V SANYO OS CON (2x220µF)
C7 = 2.2nF film
C8 = 560pF multilayer
C9 = C10 = 2.2µF / 10V
C11 = 3.9nF
C12 = 5.6nF
C13 = 330µF / 25V NCC LXF
C14 = 22nF

R1 = 3.3kΩ
R2 = 4.7Ω
R3 = 8.2kΩ
R4 = 2.7kΩ
R6 = 56kΩ
R7 = 39kΩ
R8 = 27kΩ
R9 = 2.7kΩ
R10 = 10kΩ
R11 = 10kΩ

L1 = 180µH axial
L2 = 20µH (Core Magnetics 58120, 27 turns, 0.8mm)
L3 = 15µH (Core Magnetics 58050, 16 turns, 0.6mm)
D2 = ST BYV 10 - 40
D1 = SB540
PIN 9 = OPEN

Figure 35: Extremely compact one chip solution for inkjet printer.



C1 = 100µF / 16V NCC LXF
C2 = 10µF / 50V
C3 = 330nF film
C5 = 100µF / 16V (ESR = 0.045mΩ)
C7 = 2.2nF film
C8 = 560pF multilayer
C10 = 2.2µF / 10V
C11 = 3.9nF
C12 = 5.6nF
C13 = 220µF / 35V
C14 = 22nF

R2 = 4.7Ω
R3 = 3.9kΩ
R4 = 2.4kΩ
R6 = 56kΩ
R7 = 39kΩ
R8 = 47kΩ
R9 = 2.7kΩ
'

L1 = 180µH axial (R_S = 2 to 5Ω)
L2 = 68µH (Core Magnetics 55050, 34 turns, 0.8mm)
L3 = 68µH (Core Magnetics 55050, 34 turns, 0.8mm)

D1 = D2 = ST BYV 10 - 40
PIN 9 = OPEN

TYPICAL EFFICIENCY OF FIGURE 35

V_{IN}	I_{OUT2} = 100mA			Unit
	I_{OUT1} = 0.5A	I_{OUT1} = 1A	I_{OUT1} = 1.5A	
5V	87.5	89	88.5	%
7.3V	85.5	88	85	%

Figure 36: Multioutputs idea in auxiliary converter only

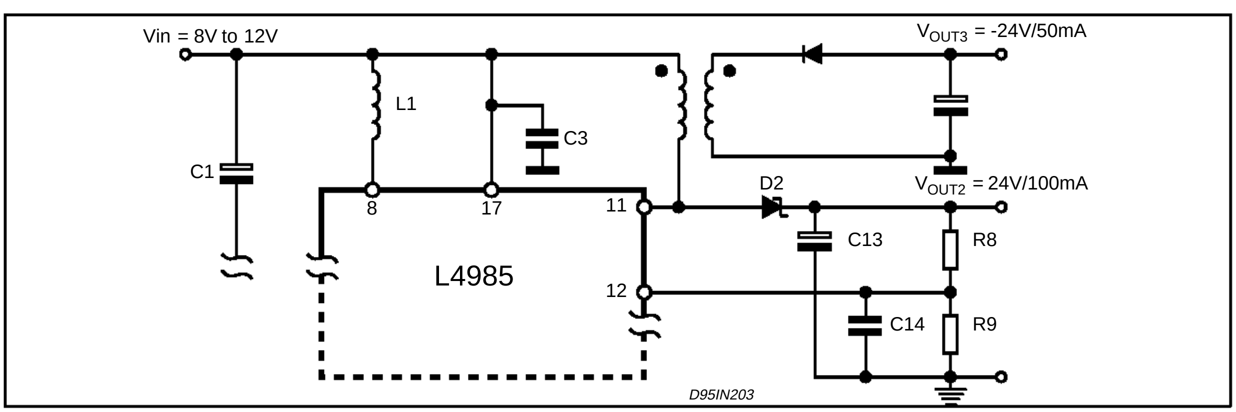
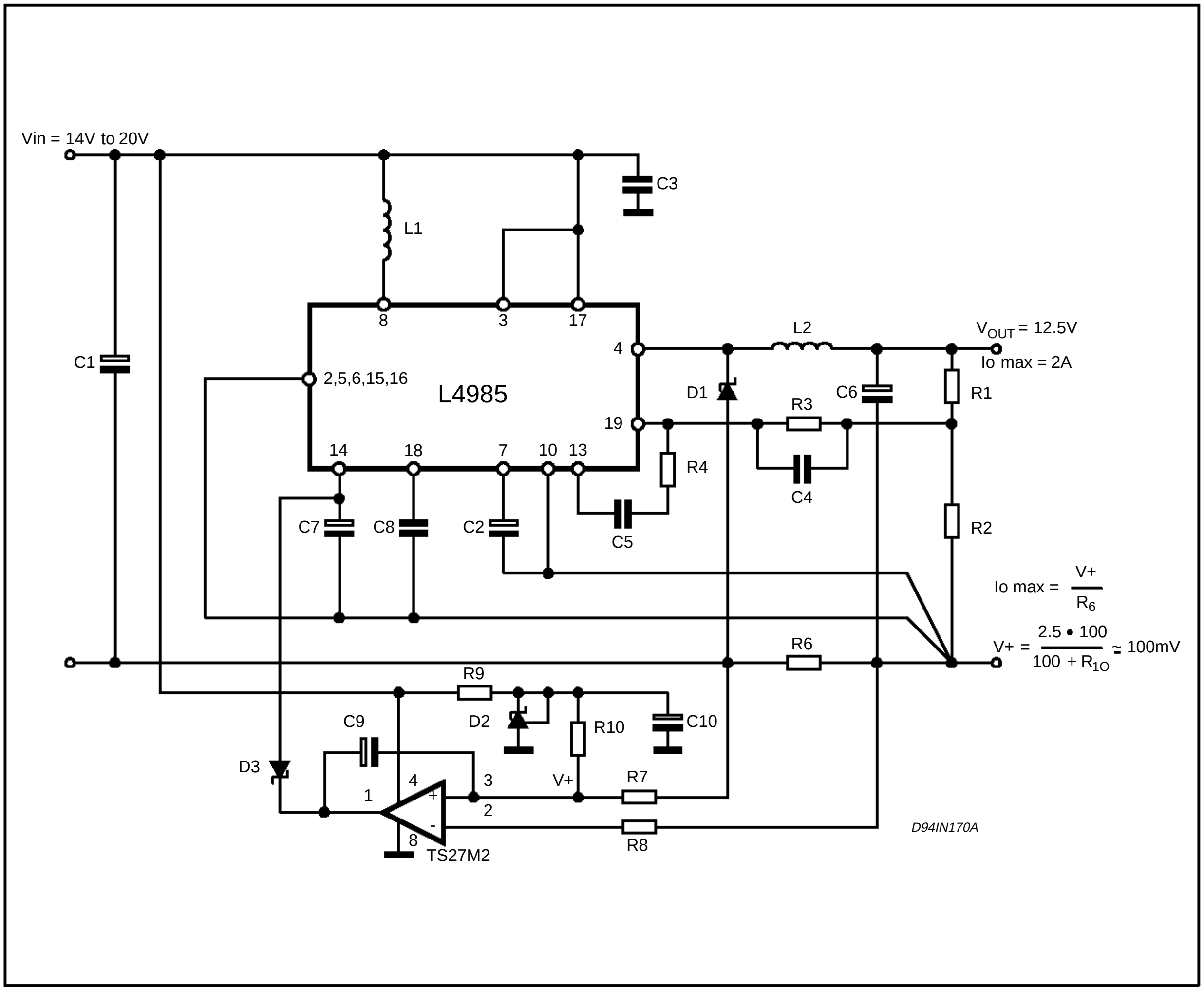
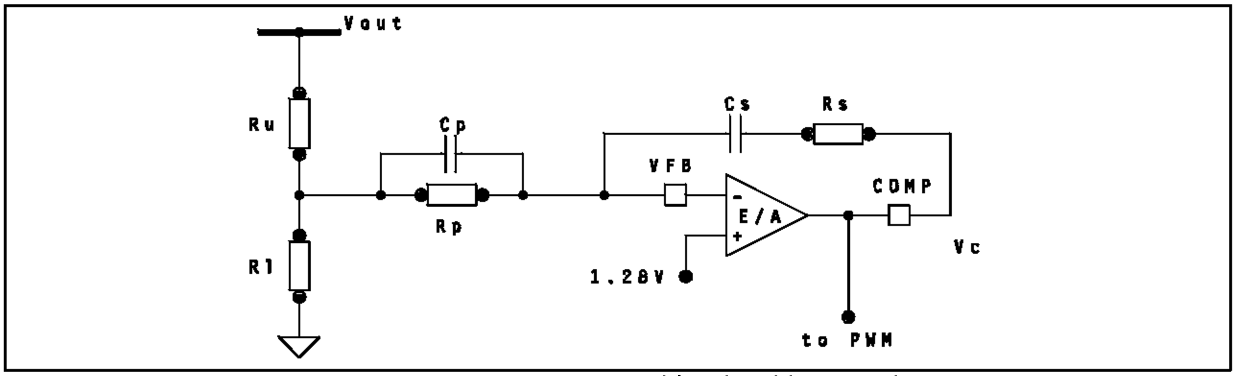


Figure 37: Battery charger application circuit.



C1 = 470µF / 25V NCC LXF	R1 = 22kΩ	L1 = 180µH axial
C2 = 10µF / 50V	R2 = 2.4kΩ	L2 = 50µH (Core Magnetics 58120, 27 turns, 0.8mm)
C3 = 330nF /63V film	R3 = R4 = 56kΩ	
C4 = 3.9nF	R6 = 55mΩ	
C5 = 2.7nF	R7 = R8 = 100Ω	D1 = SB540
C6 = 220µF	R9 = 4.7kΩ	D2 = TL431
C7 = 1µF	R10 = 2.4kΩ	D3 = BYT1040
C8 = 560pF		
C9 = 100nF		
C10 = 1µF		

Figure 38: E/A Compensation Network



APPLICATION HINTS

Oscillator (pin 18)

An external capacitor, Cosc, connected between pin 18 and SGND fixes the oscillator frequency fsw. In the range from 25 kHz to 350 kHz, fsw is given by:

fsw = 31 - 8 · Cosc + 32/Cosc,

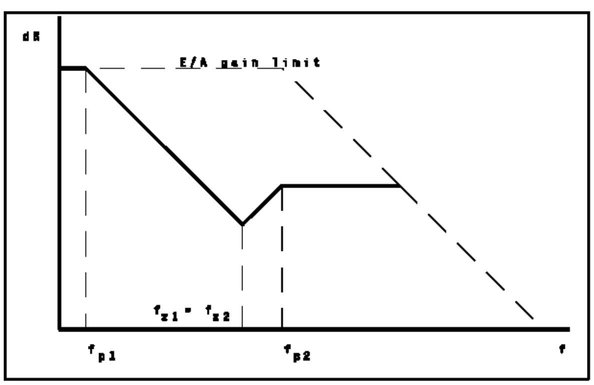
[fsw]=kHz, [Cosc]=nF

A value of 85 kHz (Cosc = 560 pF) is suggested as optimum trade-off between high efficiency and output filter size reduction.

Comp (pin 13)

An E/A compensation networks providing two pole-zero pairs is suggested for stabilizing the control loop of the L4985. In fig. 38, an example of such a kind of network is shown. In fig. 39 the bode plot of its gain is drawn.

Figure 39: E/A Compensation Network Gain.



Power Management (pins 2 & 3)

Pin 3 (DIS1), controls the enabling/disabling of the whole chip. A low level (below 0.9V) disables it, reducing the current absorbed from the supply to few A (sleep mode). A voltage above 3V enables the chip operation.

Pin 2 (DIS2) works just like DIS1 but controls the auxiliary converter only, leaving the main converter still operating.

Internal Boost (pins 7 & 8)

This low power converter is used to generate a DC bus, delivering 10 V above the supply voltage, needed for driving the internal NDMOS switches. This solution does not put any limitation both to maximum duty cycle and to minimum load current.

The internal boost uses, as external components, a small chip or axial inductor (connected to the V_S) and a capacitor (connected to PWGND).

The inductance should be in the range 100 to 200 µH, with few ohms of series resistance to limit the peak current.

The capacitor will be an electrolytic one (10 uF is OK) without any particular requirement.

Gate Driver (pin 9)

This output can drive an external PowerMOS acting as a synchronous rectifier for achieving maximum efficiency at high load current.

The driver can deliver up to 30 nC per cycle with a 10 V voltage, and that must be taken into account when selecting the external PowerMOS, because of its gate charge.

A small Schottky diode in parallel to the external PowerMOS is still used in order to avoid power losses due to the turn-on of the PowerMOS inherent diode.

Reset Function (pins 1 & 20)

The RESET signal, delivered at pin 1 with an open drain output (compatible to V_S), indicates with a low level either that the chip is disabled or that an output voltage drop has occurred.

The high level appears, after a programmable delay, as the chip is enabled or the ouptut voltage has recovered its correct value.

Figure 40: Auxiliary converter internal schematic.

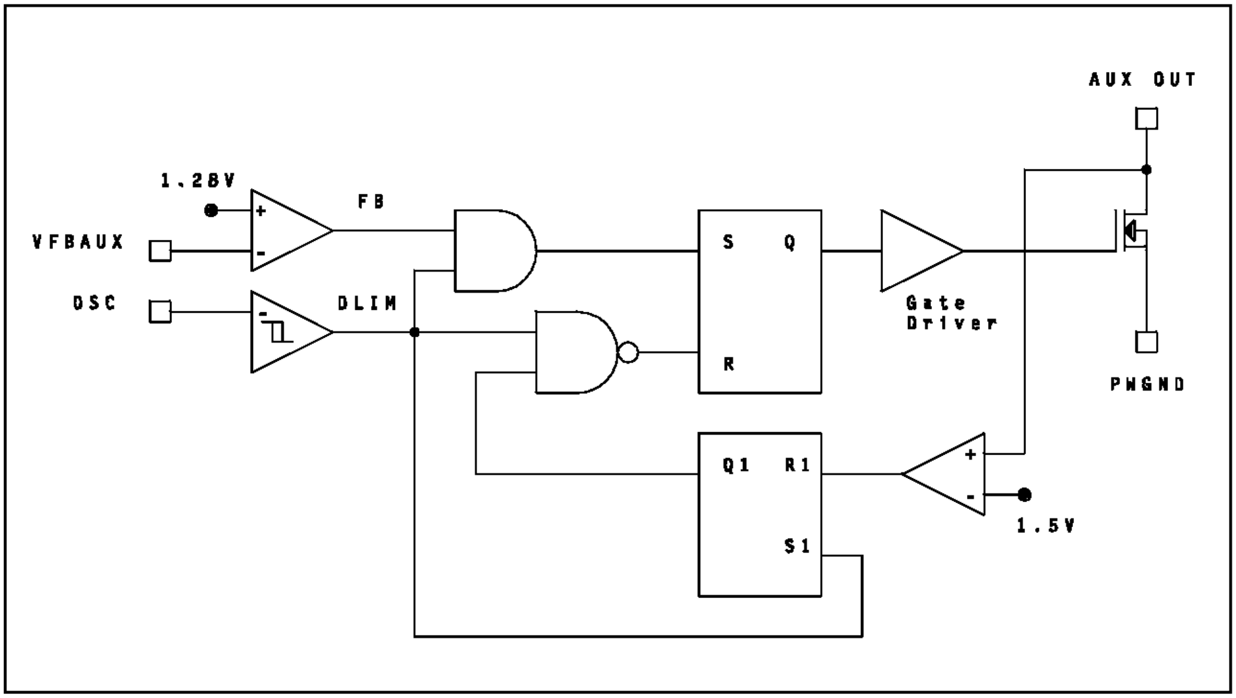
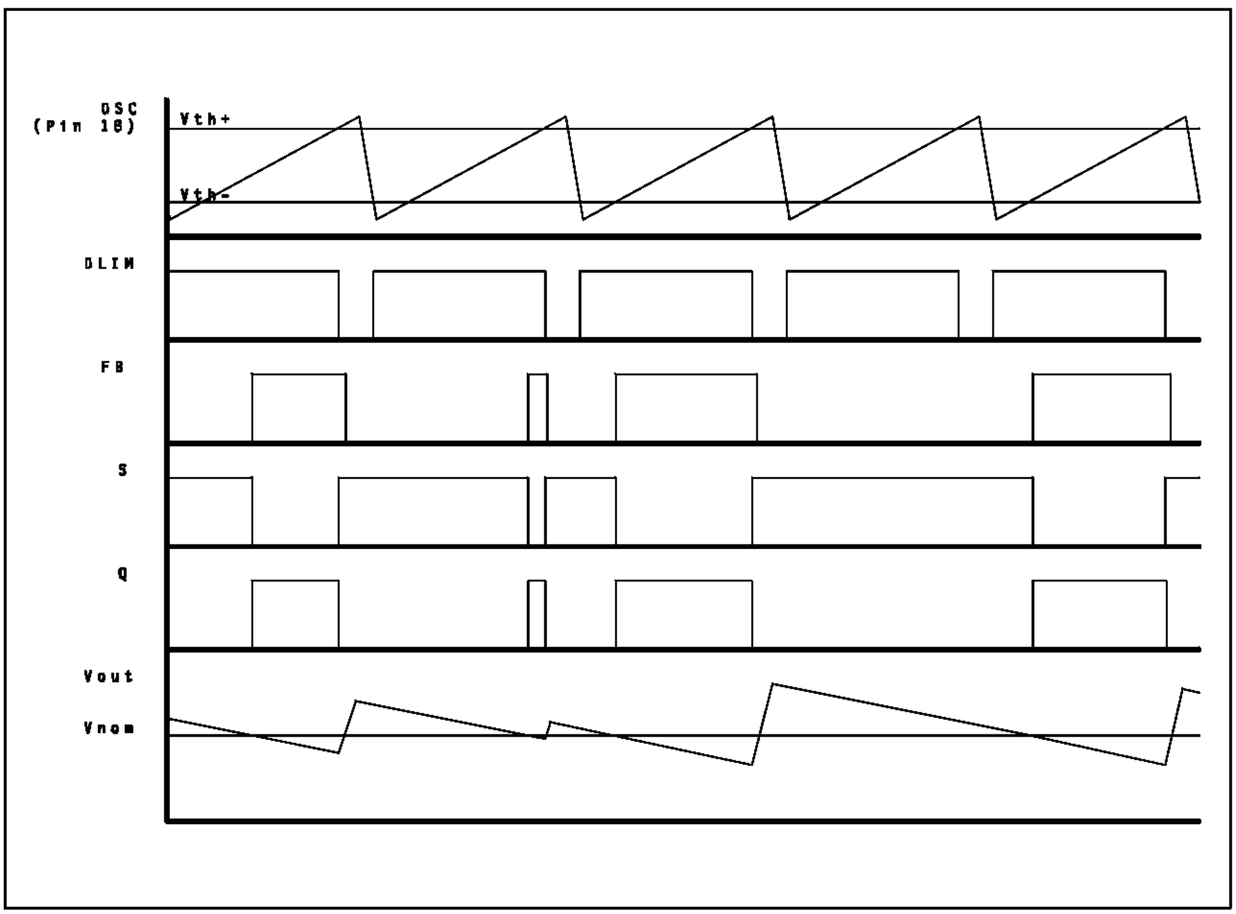


Figure 41: Auxiliary converter: Principal waveforms



The delay (Trd) is programmed by an external capacitor connected to pin 20 and SGND according to the approximate rate:

$$Trd = 250\ ms/\mu F$$

Soft Start (pin 14)

Soft-start, essential to assure a correct and safe start-up of converters, is performed by means of an external capacitor, Css. The soft-start time is related to Css by the approximate rate:

$$Tss = 30\ Vout / Vin\ \ [ms/\mu F]\ .$$

Auxiliary Converter (pins 11 & 12)

The auxiliary section includes, as a power switch, an NDMOS with grounded source and open drain, thus allowing the implementation of either boost or transformer coupled converters. That requires, besides the magnetics and the output stage, only a resistor divider to fix the output voltage. No frequency compensation is needed.

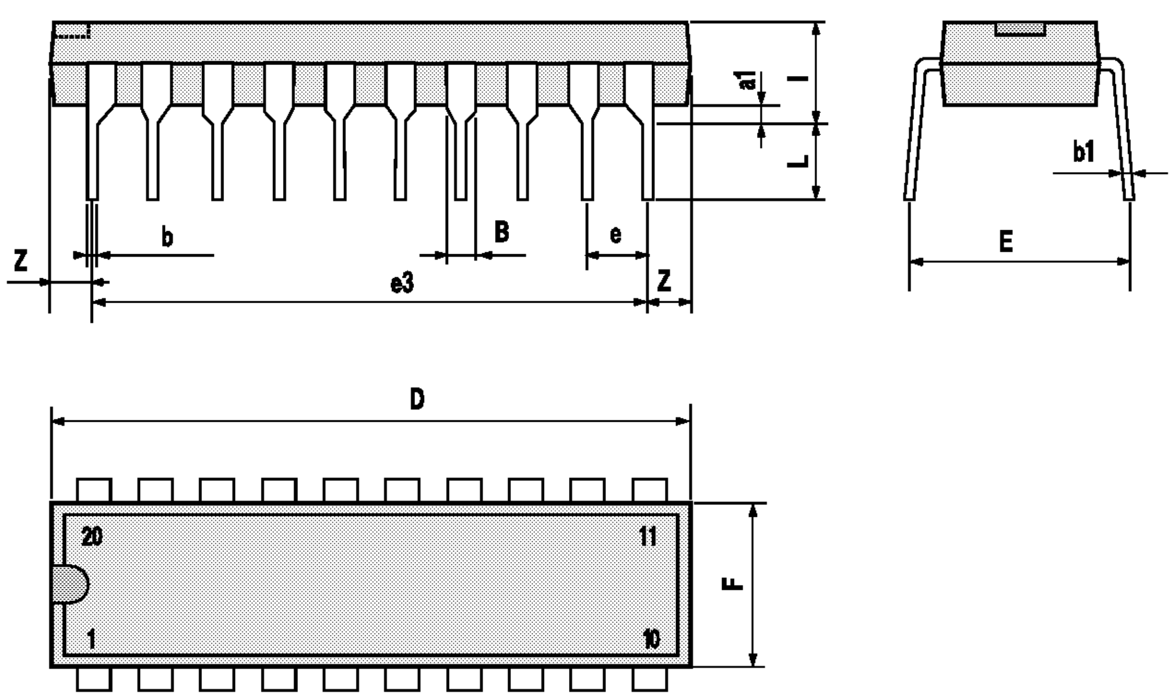
BOARD LAYOUT CONSIDERATIONS.

To prevent degraded performances or, worse, instabilities and oscillations, a careful board layout is mandatory. With this aim, the following points should be considered.

1) Separate ground paths of signals and load currents of the main converter. The two paths should have their common point in the (-) plate of the output capacitor.
2) Separate the ground path of the auxiliary converter from that of the main converter. The former runs from the (-) plate of its output capacitor to PWGND. The (-) plates of the two output capacitors should be connected.
3) Make separate supply paths for the IC (pin 17), the internal step-up and the auxiliary converter, all leading to the (+) plate of the input capacitor.
4) The anode of the Schottky diode (the drain of the synchronous rectifier, when used) should be placed as close as possible to pin 4 in order to reduce stray inductance which causes ringing spikes at MOS turn-off.
5) Place the input capacitor as close as possible to the IC so to reduce the effect of the pulsed current absorbed.
6) Make copper tracks carrying high currents (either pulsed or DC) as large as possible, in order not to impair efficiency and load regulation. Concerning this, it is important to use copper layers as thick as possible. Some of these tracks could be doubled on the other side of the board.
7) Make copper tracks carrying small signals run far from points with quickly swinging voltages.
8) Widen as much as possible the copper area to which the four central ground pins are connected, in order to make easier heat dissipation. Also ground paths could be widened to form ground planes.

POWERDIP 16+2+2 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			24.80			0.976
E		8.80			0.346	
e		2.54			0.100	
e3		22.86			0.900	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050



SO-20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45 (typ.)					
D	12.6		13.0	0.496		0.512
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8 (max.)