SGS-THOMSON MICROELECTRONICS

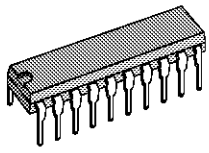
L9824

OCTAL PARALLEL LOW SIDE DRIVER

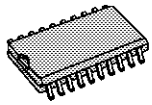
ADVANCE DATA

- OPERATING DC SUPPLY VOLTAGE RANGE 5V TO 25V
- SUPPLY OVERVOLTAGE PULSE UP TO 40V
- VERY LOW STANDBY QUIESCENT CURRENT 100µA
- EIGHT BIT PARALLEL STRUCTURE WITH MEMORY FEATURE
- BIDIRECTIONAL INPUTS-OUTPUTS
- µC COMPATIBLE INPUT LEVELS WITH THRESHOLD HYSTERESIS
- INTERNAL 4.5V REFERENCE DEFINING THE OUTPUT HIGH LEVELS
- EIGHT HIGH CURRENT OUTPUTS FOR DC CURRENTS UP TO 350mA WITH ON RESISTANCE LESS THAN 3Ω (typ. 1,5Ω)
- OUTPUT SHORT CIRCUIT PROTECTION WITH TIME DELAY CHARACTERISTICS FOR DRIVING LAMPS
- THERMAL OVERLOAD PROTECTION

MULTIPOWER BCD TECHNOLOGY



DIP20



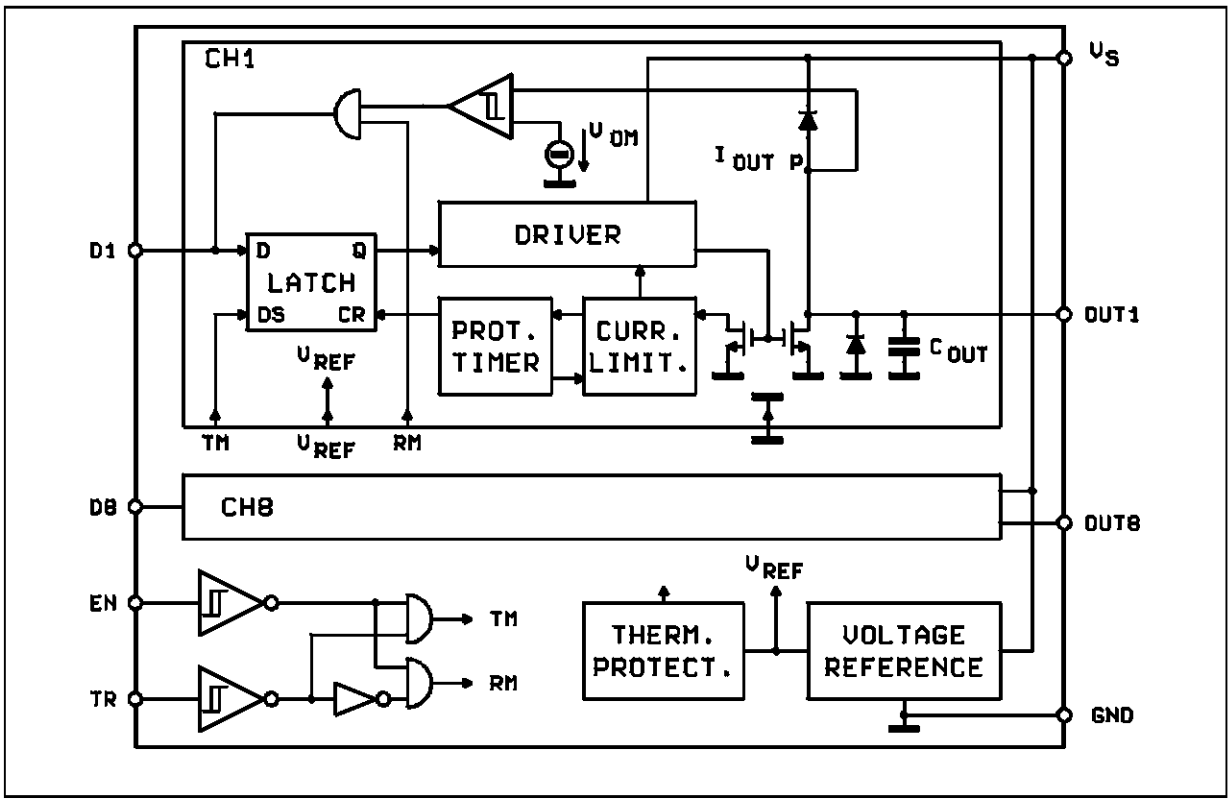
SO20

ORDERING NUMBERS : L9824 (DIP20)
L9824D (SO20)

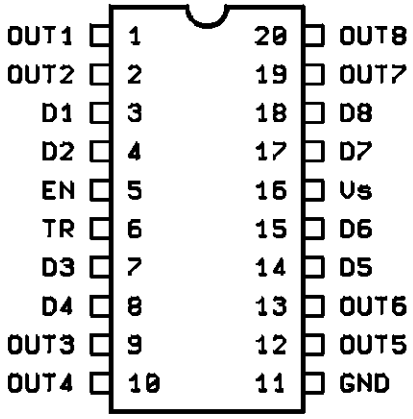
DESCRIPTION

The L9824 is an octal parallel input power interface circuit in the Multipower BCD technology with bidirectional inputs and outputs and the output status monitoring.

BLOCK DIAGRAM



PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_S	Supply Voltage		40	V
V_{OUT}	Output Voltage		Int. Clamped to Vs	
dV_{OUT}/dt	Output Voltage Transient		100	V/µs
$I_{OUT\ DC}$	DC Output Current		±350	mA
$I_{OUT\ P}$ (*)	Peak Output Current ($T/t_p \geq 100$, t_p = 4ms)		±2	A
I_S	DC Current at V_S		– 1.5	A
$V_{D\ IN}$	Input Voltage		– 0.3 to 7 (**)	V
V_{EN}	Enable Input Voltage		– 0.3 to 7 (**)	V
V_{TR}	Transfer Input Voltage		– 0.3 to 7 (**)	V
T_j	Operating Junction Temperature		– 40 to 150	°C
T_{stg}	Storage Temperature		– 65 to 150	°C
P_{max}	Power Dissipation (T_{amb} = 80°C)	DIP20 SO20	875 420	mW mW

(*) Schaffner pulses type 1 and 2
(**) For V_S < 6.7V the device can be supplied through the internal ESD diodes from inputs to V_S.

THERMAL DATA

Symbol	Parameter		DIP20	SO20
Rth j-amb	Thermal Resistance Junction-ambient	Max.	80°C/W	165°C/W
$T_{j\ MAX}$	Maximum Junction Temperature		150°C/W	150°C/W

ELECTRICAL CHARACTERISTICS ($5V \le V_S \le 25V$ (40V @ $t < 400ms$), $-40°C \le T_j \le 125°C$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DINL} V_{DINH}	Input Voltage LOW Input Voltage HIGH	V_E = L, V_{TR} = L (input-mode) 1) V_E = L, V_{TR} = H (output-mode) 1)	0 3.0		1.0 7.0	V V
V_{DOUTL} V_{DOUTH}	Output Voltage LOW Output Voltage HIGH	V_E = L, V_{TR} = H (output-mode) 1)	 4.0		0.4 5.0	V V
I_{DIN}	Input Current	V_E = L, V_{TR} = L (input-mode) 1)	– 10		10	µA
V_{ENL}	Enable Voltage LOW		0		1.0	V
V_{ENH}	Enable Voltage HIGH		3.0		7.0	V
V_{TRL}	Transfer Voltage LOW		0		1.0	V
V_{TRH}	Transfer Voltage HIGH		3.0		7.0	V
$I_{EN.TR}$	Enable, Transfer Input Current	$0 < V_{E.TR} < 5V$	– 1		1	µA
V_{EHY}	Enable Threshold Hysteresis		200			mV
V_{THY}	Transfer Threshold Hysteresis		200			mV
R_{OUT}	Output Resistance R_{OUT}-characteristic See fig. 2	Out = L $0 < I_{OUT} \le 350mA$ $V_S \ge 8V$ V_S = 6.5V V_S = 5.0V		1.5	 3.0 25 1	 Ω Ω KΩ
I_{SC}	Output Short Current I_{OUTSC}-characteristic (See fig. 3)	$8V \le V_S = V_{out} \le 25V$ T_{SCL} = 20ms	 0.36	 0.5	 1.2	 A
V_{OUT}	Output Voltage	Out = H I_{OUT} = 0.35A (DC) I_{OUT} = 1A (pulsed)	 V_S + 0.5 V_S + 2.0		 V_S + 2 V_S + 4	 V V
ΣI_{OUTL1}	Output Leakage Current per Channel	Out = H, $-40 \le T_j \le 85°C$ V_{OUT} = 16V			100	µA
C_{OUT}	Output Capacitance	Out = H, V_{OUT} = 5V V_{OUT} = 15V	 60 30	 90 60	 120 90	 pF pF
I_Q	Quiescent Current STANDBY MODE TRANSFER-, HOLD MODE READ MODE	$5V \le V_S \le 16V$; I_{DOUT} = 0 $-40 \le T_j \le 85°C$ V_E = H, V_{TR} = H V_{TR} = L V_E = L, V_{TR} = H			 100 200 400	 µA µA µA
I_Q	Quiescent Current	V_S = 25V V_S = 40V @ $t \le 400ms$		 20	2 35	mA mA
I_{SCOP}	Additional Short Circuit Operating Current Per Channel	V_{EN} = L, V_{DIN} = L V_{TR} = L, $I_{OUT} = I_{SC}$			 I_O +500	 µA
V_{OM}	Output Monitor Threshold		2.5		3.5	V
T_{SCL} (2)	Duration of Low Short Current Limiting	$I_{OUT} = I_{SCL}$	20	40	60	ms

Note : 1. $V_{D...}$ are bidirectional data inputs or outputs depending on the V_E, V_{TR} status.

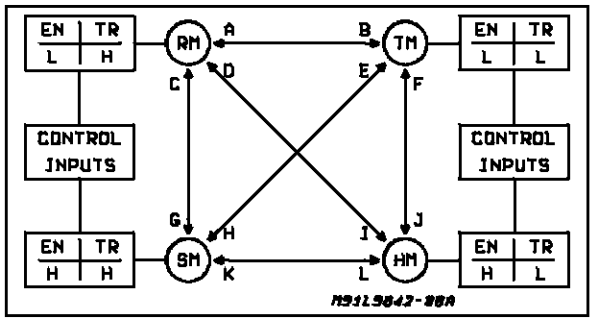
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_n ON	ON-delay Time (5)	See fig. 1 R_L = 1KΩ			10	ms
t_n OFF (3)	OFF-delay Time (5)				10	µs
t_s ON	ON-delay Time (6)			20	100	µs
t_s OFF (3)	OFF-delay Time (6)			20	40	µs
t_D ON	Data ON - Delay Time (7)			2	10	µs
t_D OFF (3)	Data OFF - Delay Time (7)			2	10	µs
t_{ON}-t_{OFF}	Delay Time Difference	Except STANDBY MODE			4	µs
t_f	Filter Time (8)		0.7	2	4	µs

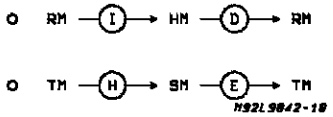
Notes : 2. If the output current exceeds the high short current threshold I_{SC} an internal timer is started. If after the time period of T_{TSC} the current limiting is still active the overload condition is recognized and this output is switched off. To restart the output the TRANSFER MODE has to be chosen and the corresponding input voltage V_{DIN} must become HIGH to reset the internal overload latch.

3. Because the output capacitance is the drain-source capacitance of the power switch the risetime of the outputs depends of the used supply voltage V_S, the load resistor R_L and the output capacitance C_{OUT} and can be calculated with the following equation :
$T_d = \tau$ In 10 (reaching 90% of V_S) $\tau = R_L \times C_{OUT} \times K$ (4) K = 1.5
This additional delay time T_d must be added to t_{OFF}.
4. Because the drain source capacitance of the output transistor is voltage dependent, it is necessary to multiply C_{OUT} (specified at the maximum V_{OUT}) with a correction factor K to obtain the average output capacitance C_{OUT}.
5. Delay time between all modes except STANDBY MODE.
6. Delay time between STANDBY MODE and any other mode and vice versa.
7. Data delay time when TRANSFER MODE is chosen.
8. Explanation see page 6.

MODE CHANGE DIAGRAM

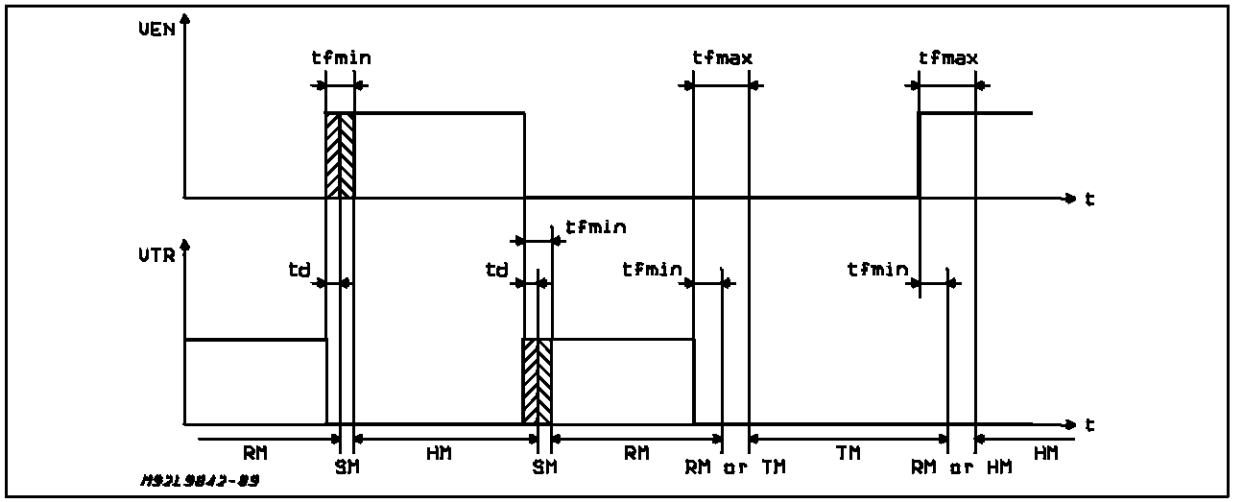


- Critical mode variations occur when both mode inputs change their state simultaneously. This is represented by the diagonal arrows in the mode change diagram.



- To avoid that a filter is implemented in the TM signal path. A suitable filter time t_f is chosen to be well beyond the mode comparator delays.

FILTERING TIMING



- As a consequence of the filter function the following features are given respectively has to be considered (refer to timing above):
- For a delay between RM and HM up to t_d < tmin the parasitic TM will be supressed.
- To obtain the transfer function surely both mode inputs be "Low" for at least t_{TM} t_{fmax}.
- Therefore the change from TM to any other mode causes an additional delay t_f that is the internal filter time.
- The parasitic SM time is too short to influence the outputs and is hence negligible.

TRUTH TABLE FOR THE CONTROL INPUTS

Enable V_E	Transfer V_{TR}	Mode Symbol	Function Mode
L	H	RM	READ MODE (output monitoring)
L	L	TM	TRANSFER MODE (input data transferred to output)
H	L	HM	HOLD MODE (output corresponds to the data latch)
H	H	SM	STANDBY MODE (all outputs open)

Figure 1 : Timing Diagram with Function Modes.

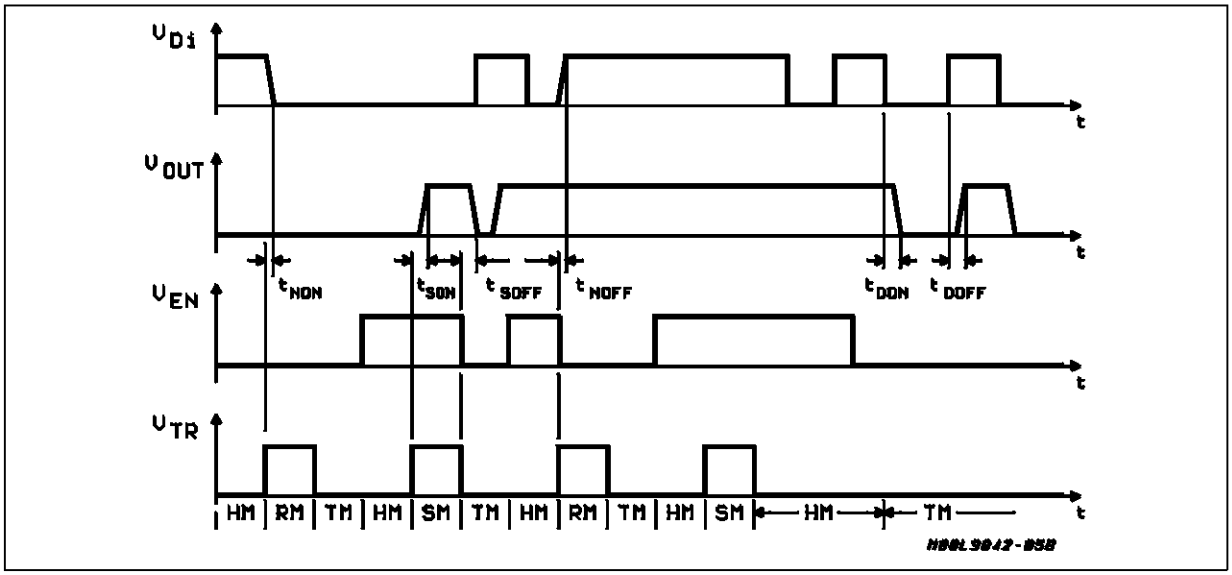


Figure 2 : Maximum R_{OUT} - Characteristics.

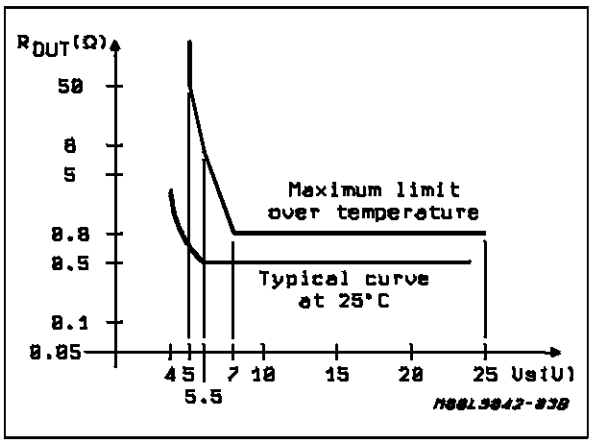
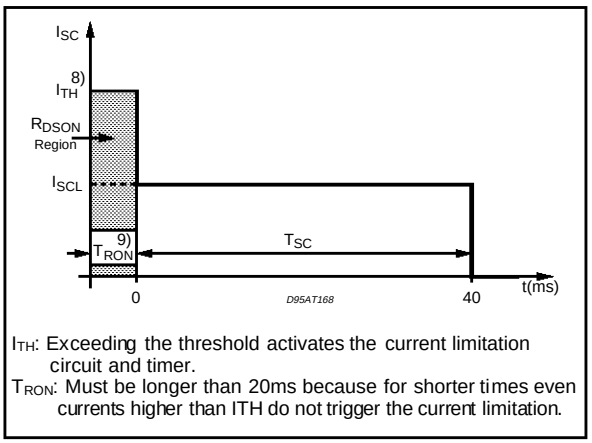
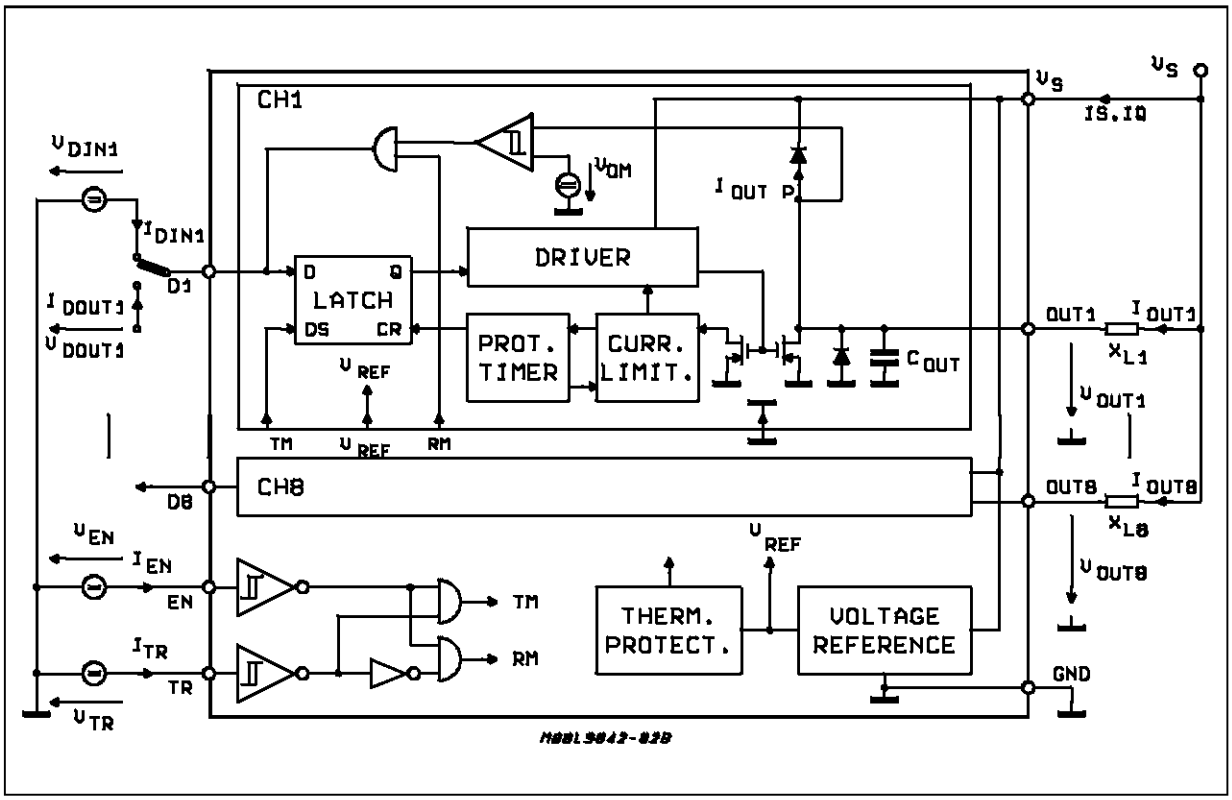


Figure 3 : Typical Short Current Characteristics.



I_{TH}: Exceeding the threshold activates the current limitation circuit and timer.
T_{RON}: Must be longer than 20ms because for shorter times even currents higher than ITH do not trigger the current limitation.

Figure 4 : Test Circuit.



FUNCTIONAL DESCRIPTIONS

This device was developed specially for automotive applications to drive different loads like relais, lamps, data buses or actuators with very low current consumption.

The L9824 contains eight identical channels each with a separate DATA input/output and the power output. In each channel the memory function, the output short circuit function and the diagnostic function is realized.

The common part determines the function modes through ENABLE and TRANSFER inputs whereas the reference part biases all current sources and generates the threshold voltages and the stabilized supply voltage for the whole CMOS-logic.

A special thermal protection, ESD-protected inputs/DATA pins and a particular output short circuit characteristic prevent a damage or the destruction of the device.

Referring to the block diagram it can be seen that each channel works independent and contains all necessary functions described in the following points.

OUTPUT BLOCK

TRANSFER FROM DATA INPUT TO POWER OUTPUT.

The DATA pins are used bidirectionally. The main path is the non inverting transfer of a digital signal from the DATA pin to the power output (TRANSFER MODE). The data pass the input latch that works also as a memory in the HOLD MODE. They remain stored until the TRANSFER MODE is selected to write in new data.

This means that in all other modes the memory content will not be changed except the output short circuit protection was active more than the check time of 42.5ms. In this case in all modes the storage flip-flop will be set to hold the output for protection into the Off-state. By activating the READ MODE in this position it is possible to detect short-circuit load.

To switch on the output again, the external control processor has to select the TRANSFER MODE and to change the input signal at the corresponding data terminal to HIGH to set the storage flip-flop and then to write in LOW. An additional reading of this channel output (selecting the READ MODE after the mentioned check time) shows whether the short-circuit is still present.

TRANSFER FROM POWER OUTPUT TO DATA OUTPUT.

The opposite signal path (READING MODE) from the output to the DATA terminals is used for the diagnostic function to monitor the output status. Output voltages greater than 3.5V lead to "HIGH" state at the DATA terminals. The HIGH level is typical 4.5V and internally stabilized. For "LOW" level the saturation voltage of N-Channel MOS transistor is relevant.

SHORT-CIRCUIT PROTECTION.

For the use of lamps a particular short-current characteristic is implemented and it is drawn in fig. 3. Because of the low resistance of lamps during the ON-phase the current limit is for typical 2.5ms about the double as for the second current limiting phase. Detecting a short circuit condition means that the channel output remains low in any condition for the check time $T_{CH} = T_{TSCH} + T_{SCL}$ independent of the status of the inputs.

These time periods are generated from two frequencies 400Hz/6.4kHz coming from the common oscillator part. If the current limiting is active after the check period an overload is recognized and the regarding channel is switched off and the DATA flip-flop is also reset as explained earlier.

In order to save supply current a special short-circuit protection is used that needs no quiescent current during the ON-state as long as no overload is present at the output. Because of this special circuit configuration the output current must exceed a given threshold to activate the current regulation loop.

This current threshold I_{TH} is determined by the ON-resistance R_{DSON} of the output DMOS and the minimum operating supply voltage V_{Smin} of the limiting circuit and can be easily calculated in the following way :

$I_{TH} = V_{Smin}/R_{DSON} = 4V/1.5\Omega = \underline{2.7A}$ (typical value at $T_j = 25°C$)

When the output is shorted for instance to V_S a maximum peak current will occur for a short duration up to the limiting circuit is switched on and the settling time is over. Under worst case conditions ($T_j = -40°C$), $V_S = 16V$, where R_{DSON} is lowest) the peak current can reach 7A with a duration of 1µs at V_{out} = 15V and 4A with a duration of 20µs at V_{out} = 5V.

COMMON PARTS

MODE CONTROL.

By the "TRANSFER" and "ENABLE" input, working modes can be selected as shown in the truthtable in the upper part of fig. 1. The control signals coming from both input comparators which determine the logic threshold and hysteresis drive the mode logic that distributes the right data to all output blocks.

TRANSFER, HOLD and READ MODE are explained before. The remaining STANDBY MODE switches the clock oscillator and all outputs off and reduce the quiescent current below 100µA. This means that only the both mode comparators and the bandgap regulator are active. The input data stored before will be not changed.

OSCILLATOR PART.

The clock oscillator contains an on-chip capacitor and requires therefore no external components. The oscillation frequency is approximately in the range of 50kHz. This oscillator signal is devided by a 7 bit-counter which creates the two frequencies for the timing of all short current control circuits in each output block.

VOLTAGE REFERENCE.

The main reference cell is a bandgap controlled very low drop voltage regulator. All threshold voltages for the input comparators, the diagnostic comparators and the thermal overload comparators as well as the reference voltage for the CMOS supply buffers are derived from one resistor devider.

Because of the low current capability of the regulator two buffers are used to supply the CMOS logic for every four channels. These voltage followers work like a current multiplier at a very low quiescent current. A clamping circuit prevents that the CMOS breakdown voltage will be reached.

CURRENT REFERENCE + POWER–ON RESET.
The two temperature compensated current lines are generated directly from the bandgap voltage and are switched off by the mode logic to save supply current. A third unswitched current line biases the input comparators and CMOS buffers.

During supply voltage rise, power-on reset circuit provides a defined status of all latches in the CMOS logic. From a supply voltage of about 4V on it enables the whole logic and the device can work. Below 4V all latches are set to hold the outputs into the OFF state.

PROTECTION CIRCUITS

ESD–PROTECTION.

Both input comparators (ENABLE, TRANSFER) are ESD protected and include zener diodes that clamp the gates of the internal MOSFETs to minimal 15V. Second diodes clamp these inputs to V_S if the supply voltage is lower than 0.6V below the zener voltage.

The eight "DATA" terminals has the same ESD protection structure as the comparator inputs.

SHORT CURRENT LIMITING.

The detailed function explanation is given in a former section where the output block is described. Generally it can be supplementary said that this kind of protection determines the limits within the safe operating area of the used DMOS structure.

The big chip area and the heat capacity of silicon allow for short durations peak currents up to five times the maximum DC current that occur under certain conditions as expounded above.

THERMAL SHUTDOWN.

Because of the symmetry and the big size of chip two thermal overload protection circuits were placed on each side of the chip where the output structures are concentrated to ensure minimum thermal gradients to the thermal sensors.

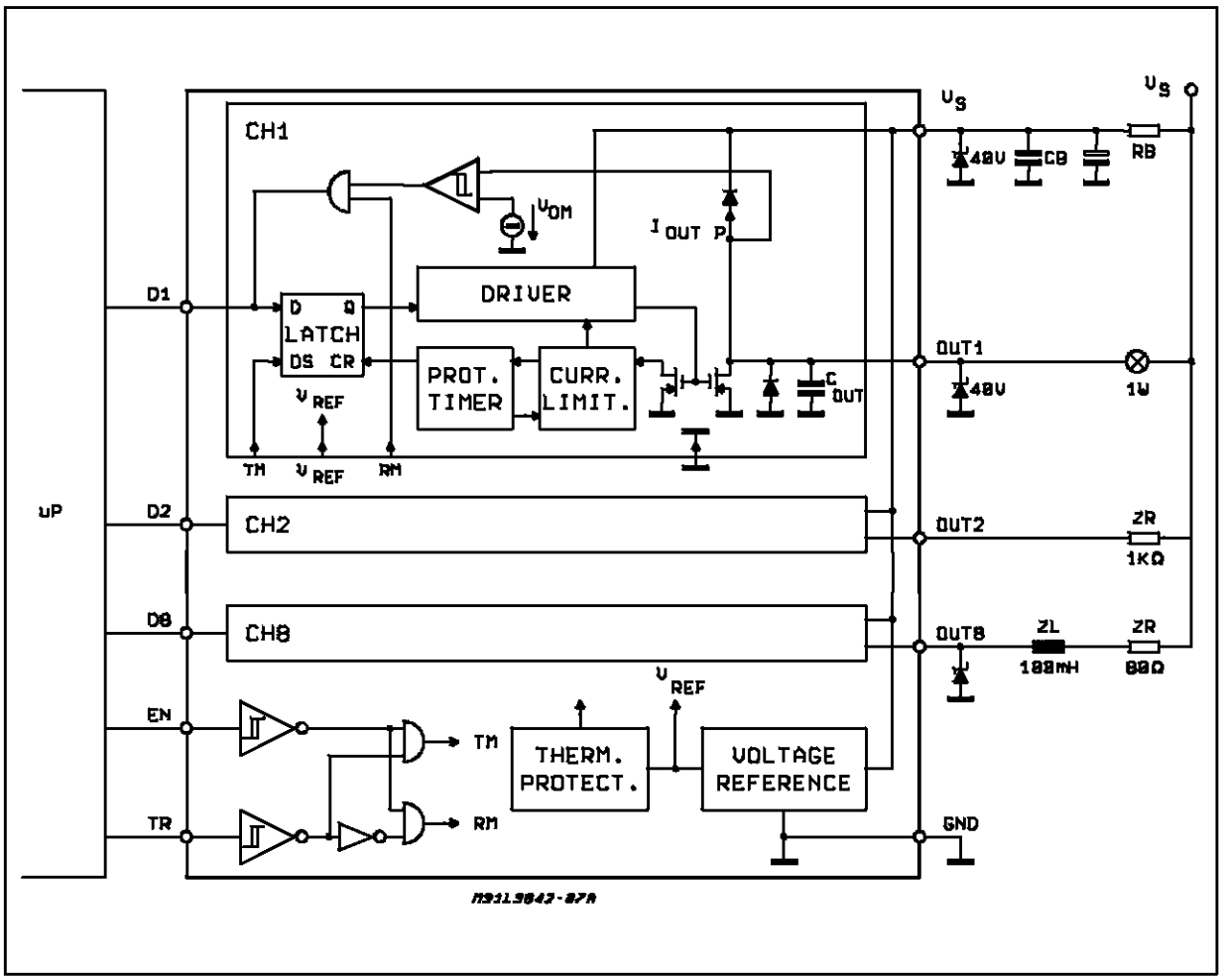
At a chip temperature of about 160°C the device is switched OFF. This state is similar to the STANDBY MODE. After the temperature remains under approximately 135°C the element is switched ON. Thermal shut-down does not influence any logic because it switches only the gates of all output DMOS-transistors directly to ground.

APPLICATION HINTS

– Precausions by external components must be provided to avoid damage of the device (it's in any case not allowed to exceed the maximum ratings given on page 2).

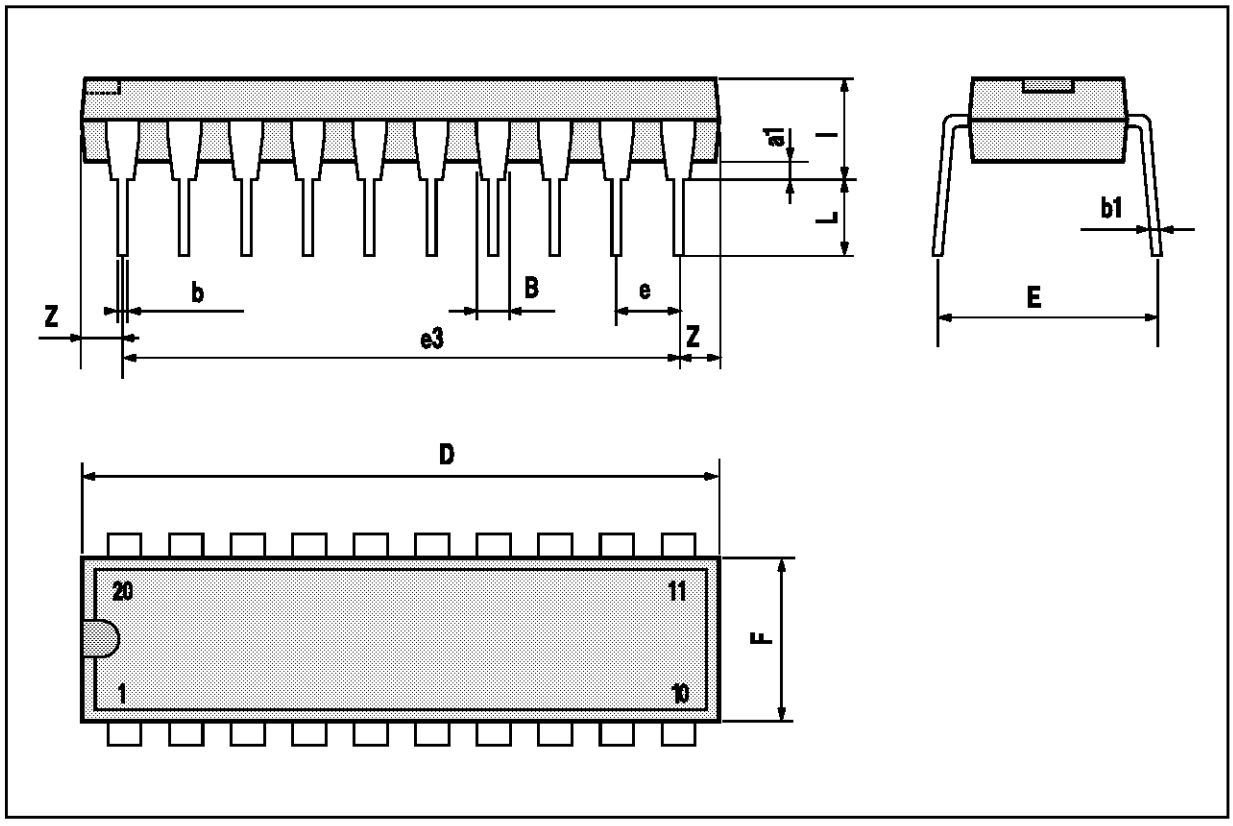
– For open load detection it is recommended to use external components to fix the desired status (depending on the temperature the internal open load status can vary from "H" to "L" caused by leakage currents)

Figure 5: Application Diagram



DIP20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



SO20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45 (typ.)					
D	12.6		13.0	0.496		0.512
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8 (max.)