Ordering number:EN4033A

Monolithic Linear IC

LA4536M

5V CD Headphone-stereo Power Amplifier

The LA4536M is a low noise, low distortion headphone-stereo power IC designed for use on a portable CD.

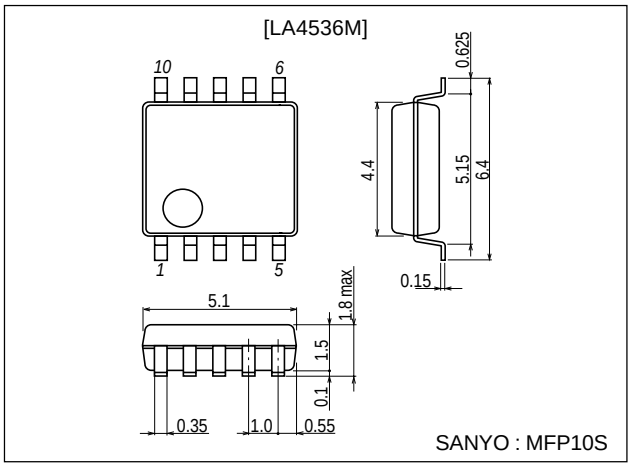
Features

- Less current drain.
- Accept 16Ω load drive.
- Excellent voltage reduction characteristic.
- Excellent ripple rejection.
- Power switch function and built-in muting circuit.
- Low noise (7μV), low gain (11dB).

Package Dimensions

unit:mm

3086A-MFP10S



Specifications

Absolute Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max	No signal	6.0	V
Allowable power dissipation	Pd max		300	mW
Operating temperature	Topr		–20 to +75	˚C
Storage temperature	Tstg		–40 to +125	˚C

Operating Conditions at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		5.0	V
Operating supply voltage range	V_{CC} op		4.0 to 6.0	V
Recommended load impedance	R_L		16 to 32	Ω

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquaters

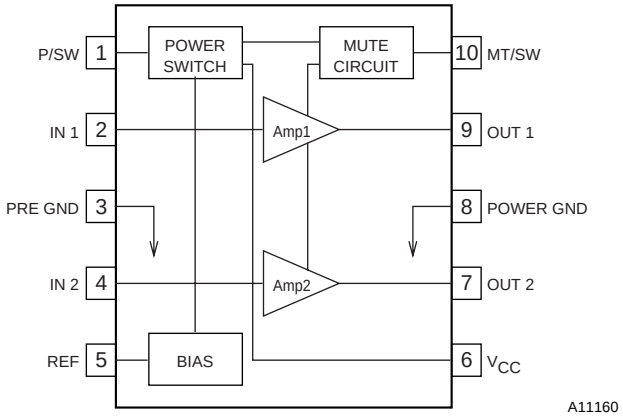
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Operating Characteristics at Ta = 25˚C, R_L=16Ω, Rg=600Ω

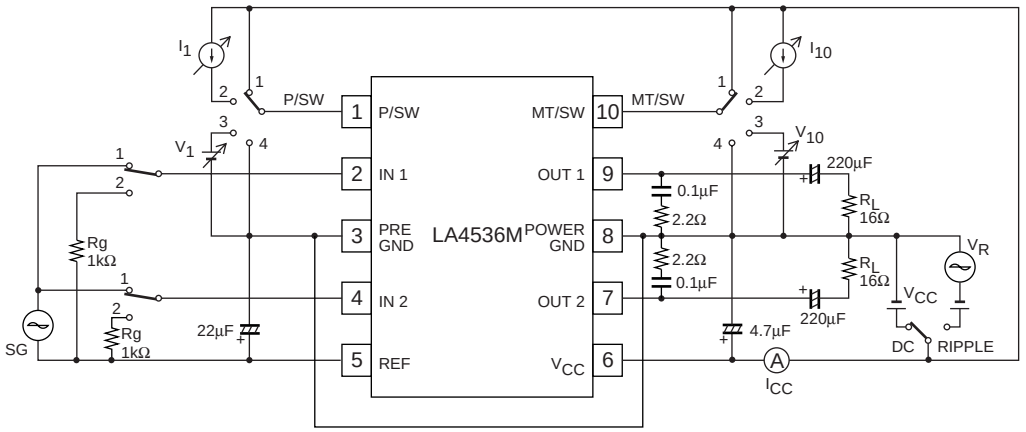
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current	$I_{CCO}1$	V_{CC}=5.0V, no signal		10	20	mA
	$I_{CCO}2$	V_{CC}=6.0V, pin 10, GND		1.1	4.0	mA
	$I_{CCO}3$	V_{CC}=6.0V, pin 1, GND			1.0	µA
Voltage gain	VG	V_{CC}=5.0V, f=1kHz, V_O=– 10dBm	9	11	13	dB
Voltage gain variations	ΔVG1	V_{CC}=5.0V, f=1kHz, V_O=– 10dBm			1.0	dB
	ΔVG2	V_{CC}=4.0V, f=1kHz, V_O=– 20dBm			1.0	dB
Total harmonic distortion	THD	V_{CC}=5.0V, f=1kHz, P_O=– 1mW		0.02	0.24	%
Output power	P_O	V_{CC}=5.0V, f=1kHz, THD=10%	40	100		mW
Crosstalk	CT	V_{CC}=5.0V, f=1kHz, Rg=1kΩ, V_O=– 10dBm	40	60		dB
Ripple rejection	SVRR	V_{CC}=4.0V, f=100Hz, Rg=1kΩ, V_O=– 20dBm, BPF=100Hz	45	65		dB
Output noise voltage	V_{NO}	V_{CC}=6.0V, Rg=1kΩ, BPF=20Hz to 20kHz		7	20	µV
Power off effect	$V_{O(off)}$	V_{CC}=4.0V, f=100Hz, Pin 1 to GND, V_{IN}=– 10dBm			– 80	dBm
Mute effect	$V_{O(MT)}$	V_{CC}=4.0V, f=100Hz, Pin 1 to GND, V_{IN}=– 10dBm			– 80	dBm
Power on current sensitivity	$I1_{(on)}$	V_{CC}=5.0V, V5>0.85V		0.05	2.0	µA
Power off voltage sensitivity	V1(off)	V_{CC}=5.0V, V5>0.1V	0.5	0.6		V
Mute off current sensitivity	I10(off)	V_{CC}=5.0V, V5>0.85V		0.2	2.0	µA
Mute on voltage sensitivity	V10(on)	V_{CC}=5.0V, V5>0.1V	0.5	0.65		V

Note : Quiescent current is the current flowing into pin 6. The current flowing into pin 1 and pin 10 is at the maximum value and calculated from the equation (V pin–0.5V)/16[V/kΩ], increasing total current.

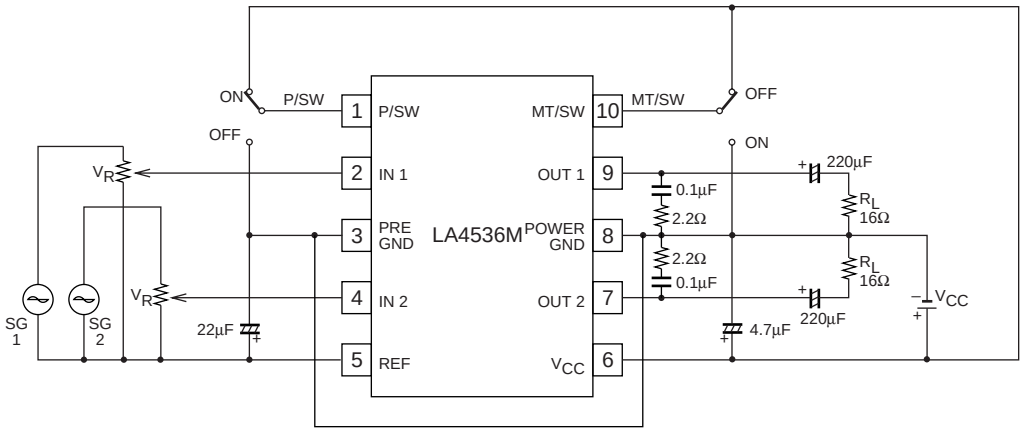
Equivalent Circuit Block Diagram



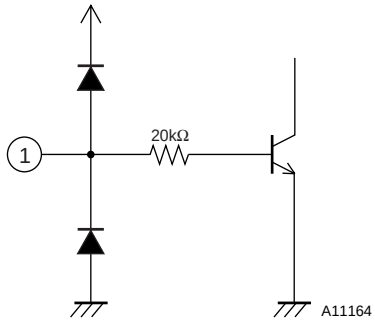
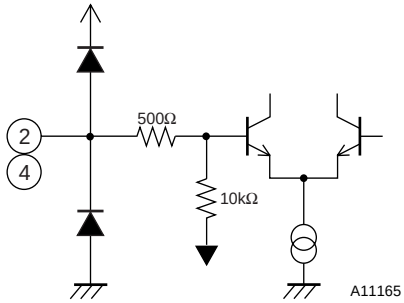
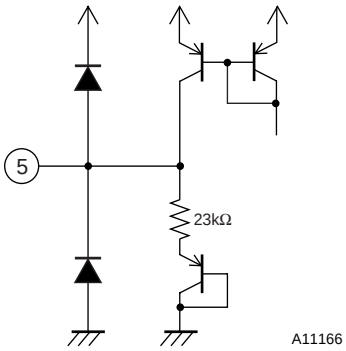
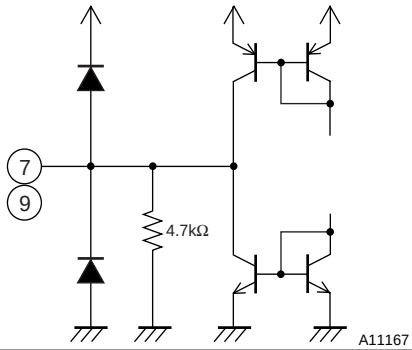
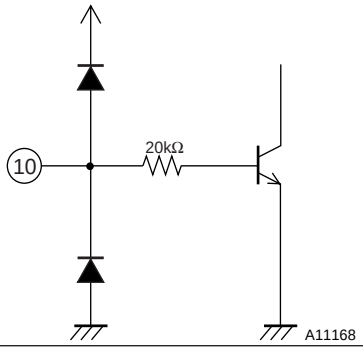
Test Circuit



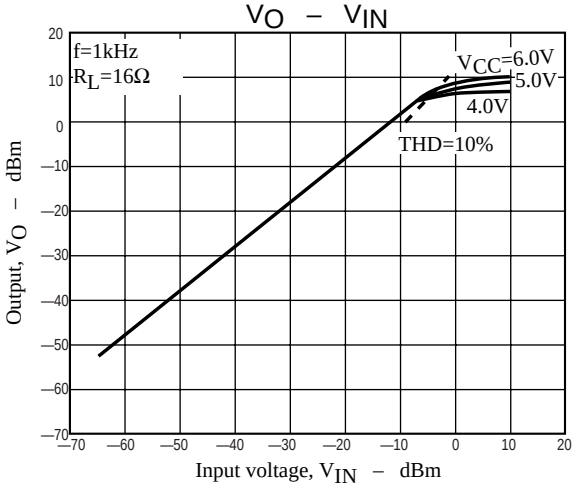
Sample Application Circuit



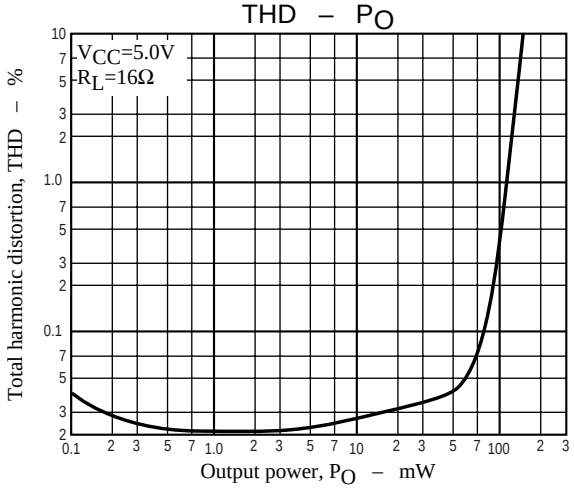
Pin Functions (V_{CC}=5.0V)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Pin function
1	P/SW1			• The system turns on when the V_{CC} is applied to this pin and turns off by connecting this pin to GND.
2 4	IN1 IN2	2.1 2.1		• Input pin connection. Input impedance is 10kΩ.
3	PRE GND			
5	REF	2.1		• 2.1V fixed bias is applied to this pin.
6	V_{CC}			
7 9	OUT2 OUT1	2.1 2.1		• Output pin connection.
8	POWER GND			
10	MT/SW			• The muting function turns on when this pin is connected to GND and turns off by applying the V_{CC} to this pin.

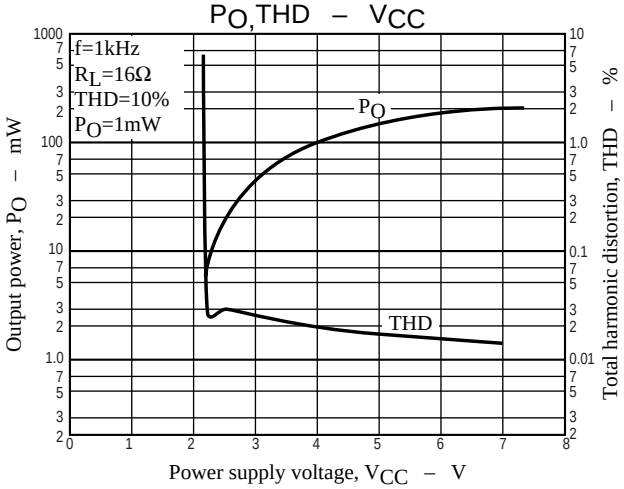
V_O – V_{IN}



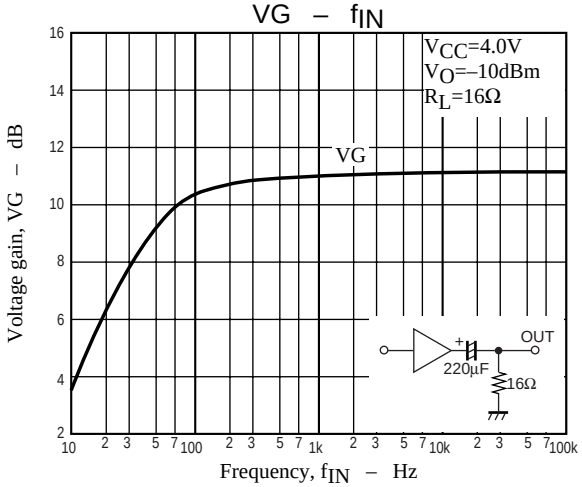
THD – P_O



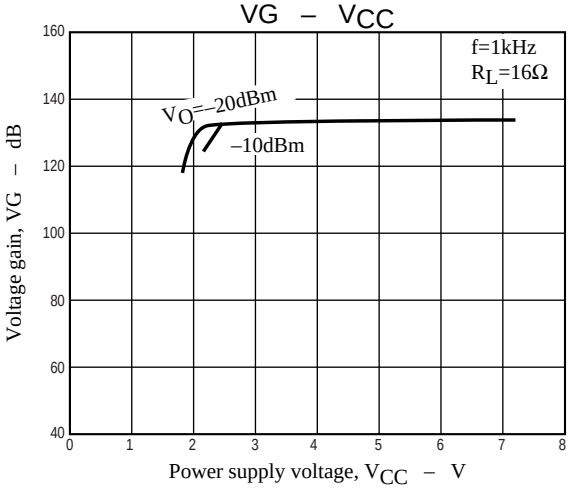
P_O, THD – V_{CC}



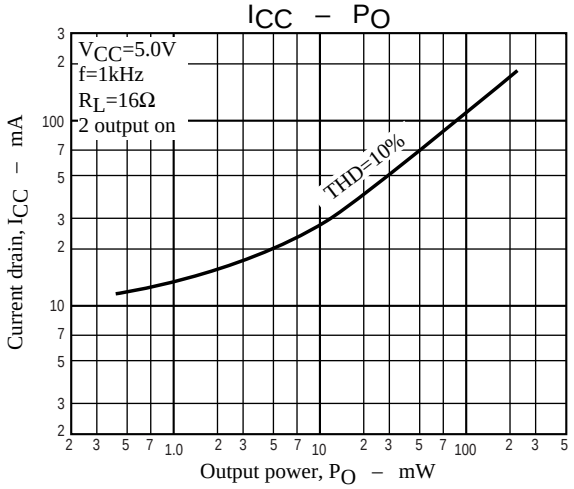
VG – f_{IN}



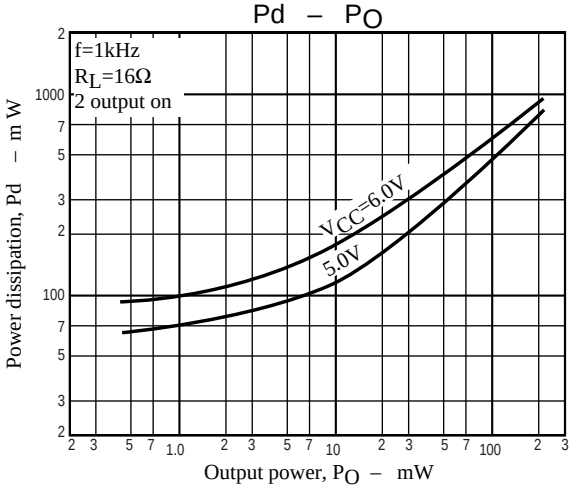
VG – V_{CC}



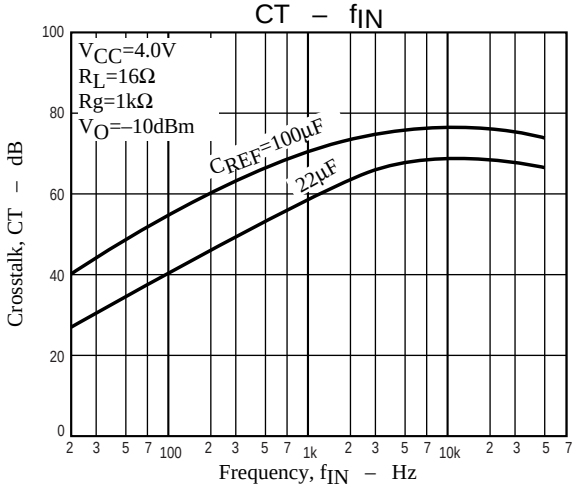
I_{CC} – P_O



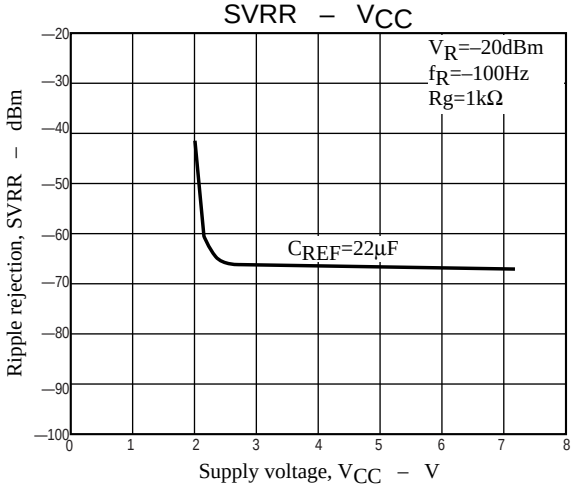
Pd – P_O



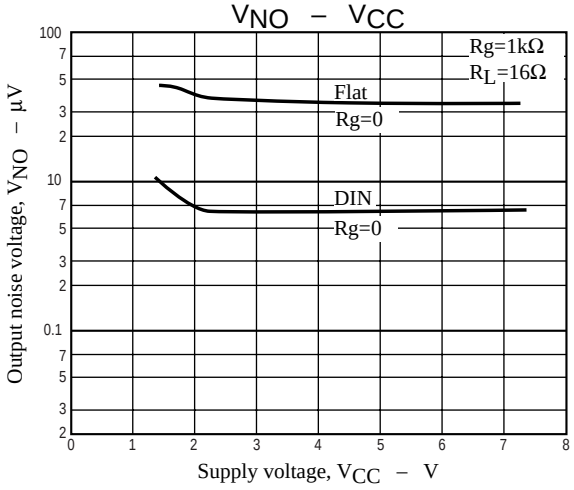
CT – f_{IN}



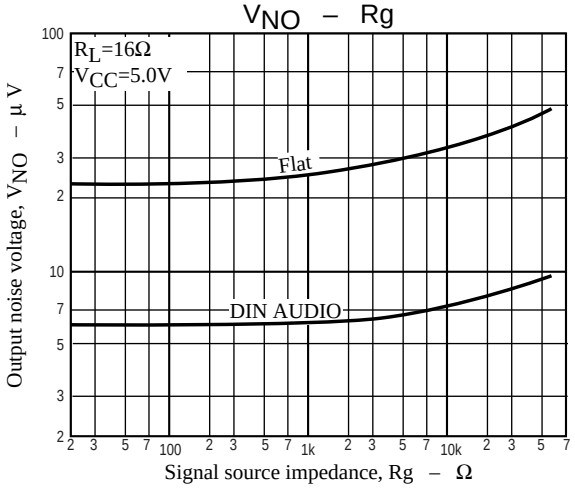
SVRR – V_{CC}



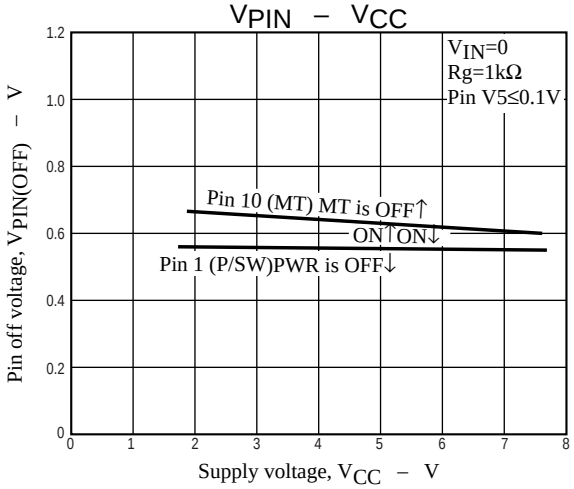
V_{NO} – V_{CC}



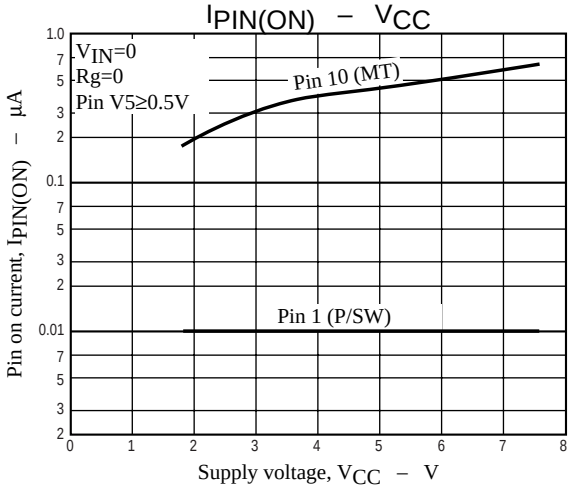
V_{NO} – Rg



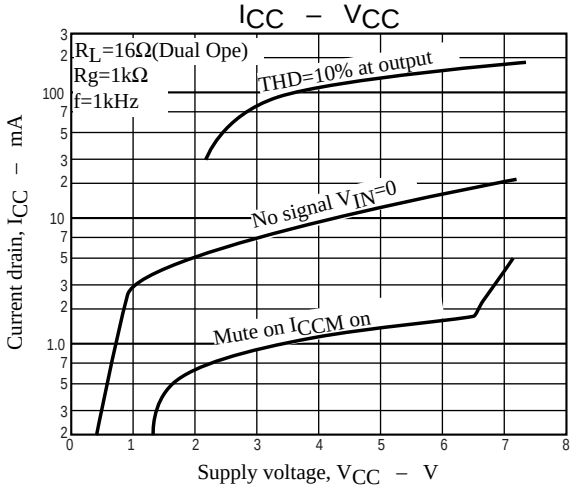
V_{PIN} – V_{CC}



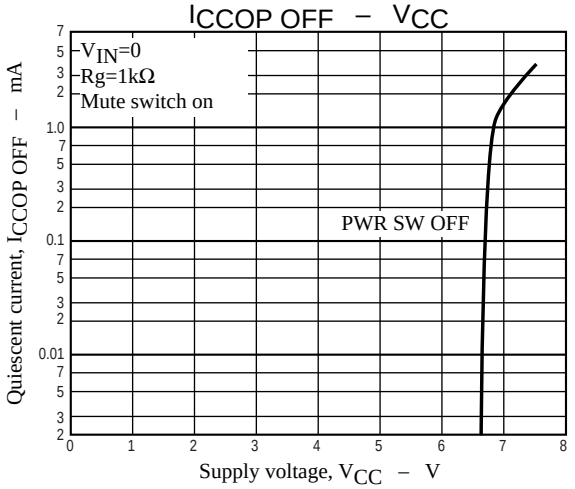
$I_{PIN(ON)}$ – V_{CC}



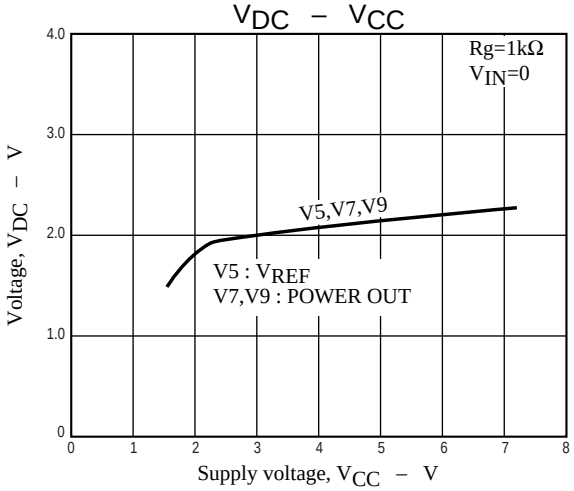
I_{CC} – V_{CC}

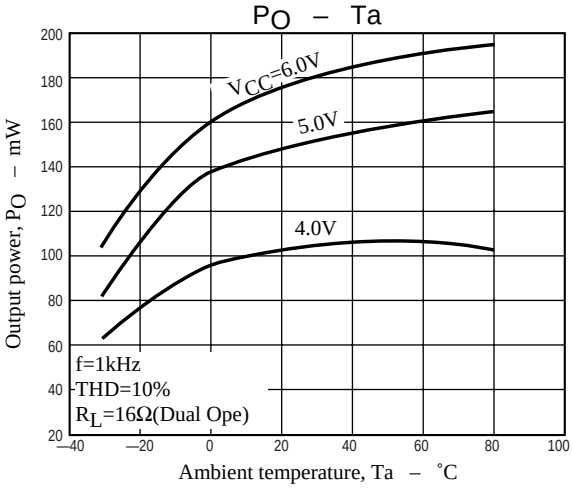


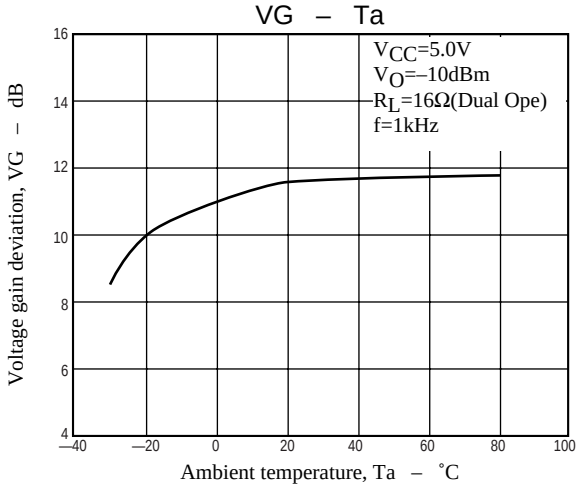
$I_{CCOP\ OFF}$ – V_{CC}

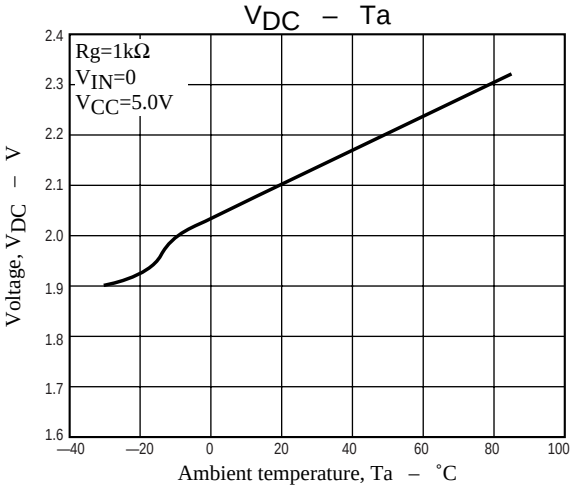


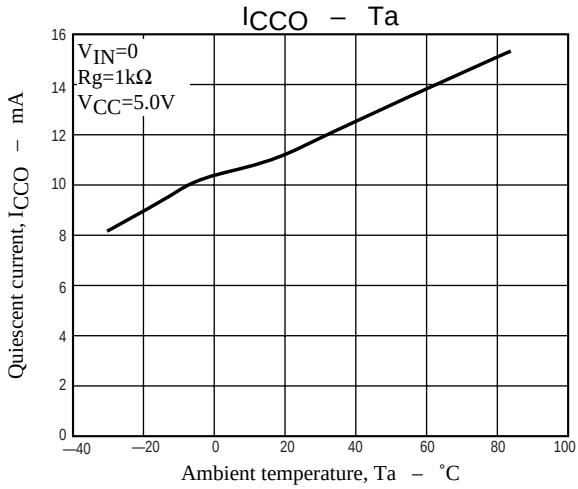
V_{DC} – V_{CC}



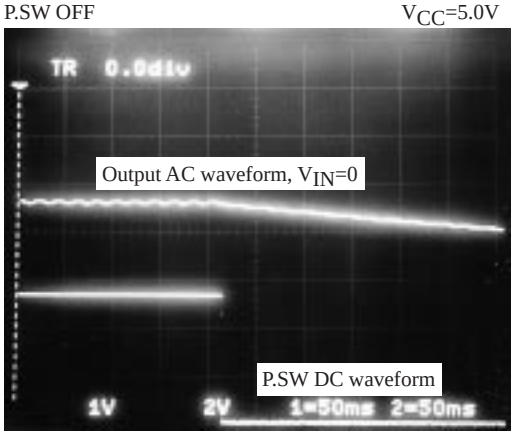




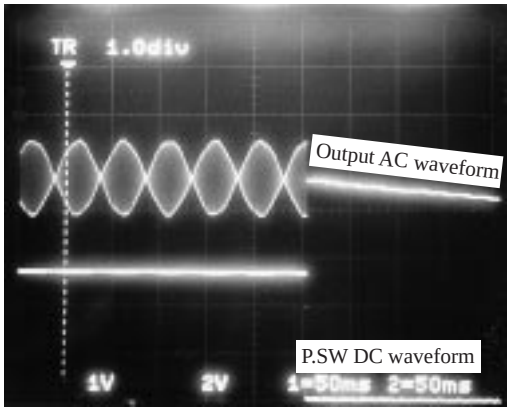




P.SW OFF V_{CC}=5.0V

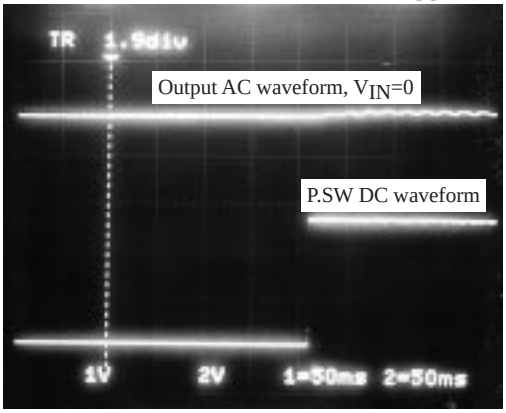


P.SW OFF

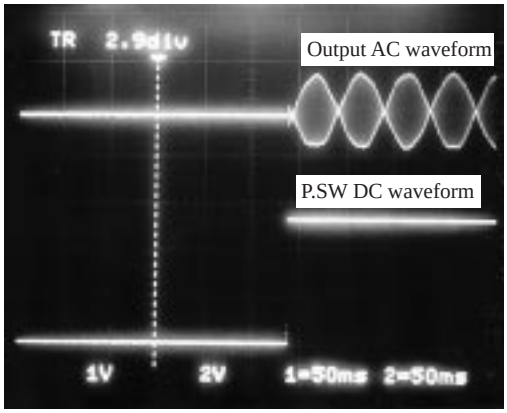


P.SW OFF

P.SW ON V_{CC}=5.0V

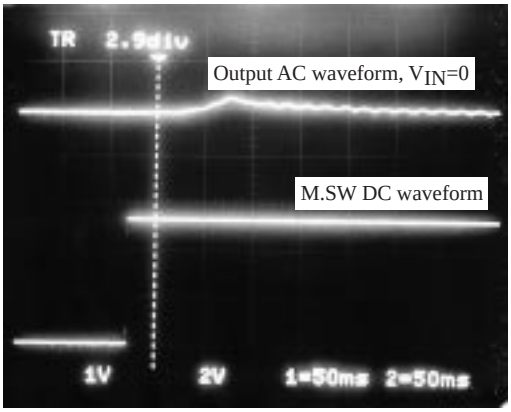


P.SW ON

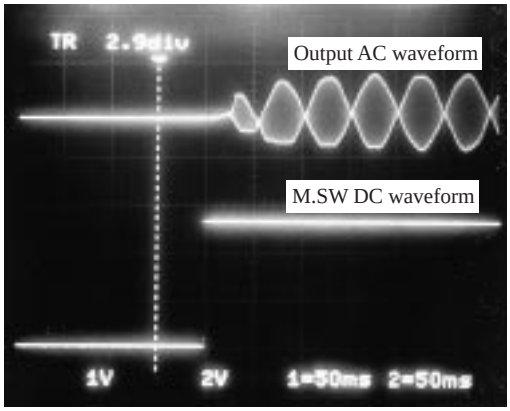


P.SW ON

M.SW OFF V_{CC}=5.0V

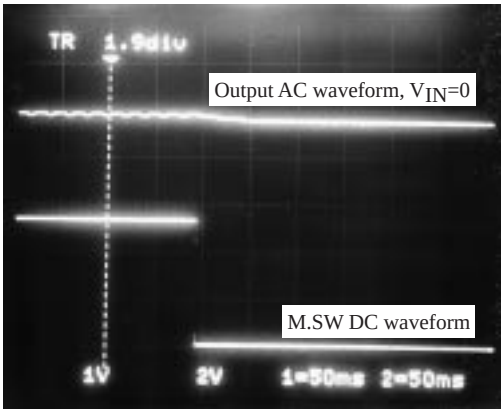


1V/div M.SW OFF

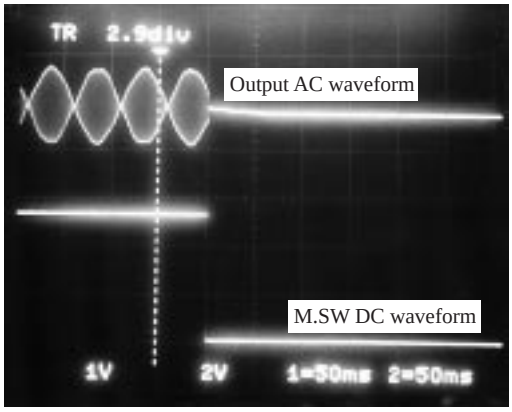


M.SW OFF

M.SW ON V_{CC}=5.0V



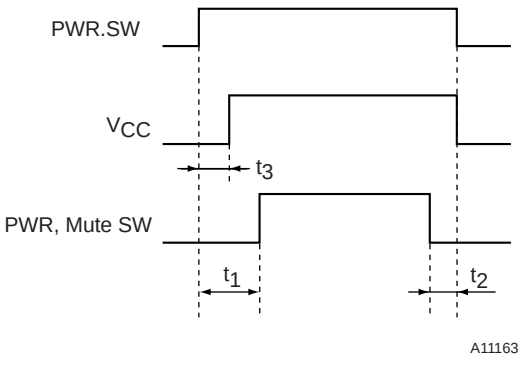
1V/div M.SW ON



M.SW ON

Application Notes

Popping noise reduction
The switching sequence shown below can minimize the popping noise.



To minimize poping noise, the PWR mute switch should be turned on t1 (about 0.1s) after power-on and turned off t2 (about 0.1s) before power-off. Turn on and off the PWR mute switch by applying V_{CC} with the PWR be in on state.