

SANYO

No.3244

LA5691D, 5691S**Voltage Regulator Driver with Watchdog Timer
(with Output ON/OFF Function)**

The LA5691 is a single-chip voltage regulator for microcomputer system monitor use that performs the functions of 5V output voltage control, watchdog timer, and voltage detector. Since the LA5691 is capable of exercising output ON/OFF controls it is especially suited for use in battery-powered equipment.

Applications

- Microcomputer system for car equipment, refrigeration/heating equipment, office automation equipment.

Functions

- Output voltage 5V_{control}
- Watchdog timer
- Reset generation at power-ON mode
- The enable pin can be used to exercise output ON/OFF control. (Active-low)

Features

- An external PNP transistor can be used to provide a low-saturation voltage regulator.
- Capable of reducing of power dissipation at standby mode ($I_{Q\ OFF} = 300\text{mA typ}$)
- CK input with edge detector
- Variable detection voltage

Maximum Ratings at $T_a = 25^\circ\text{C}$

				unit
Control Pin Voltage	$V_{\text{CONT max}}$	1sec	60	V
Control Pin Voltage	$V_{\text{CONT max}}$		41	V
Control Pin Current	$I_{\text{CONT max}}$	$*V_{\text{CC}} \geq 6\text{V}$	11	mA
Enable Pin Voltage	$V_{\text{EN max}}$		41	V
CK Input Voltage	$V_{\text{CK max}}$		25	V
Reset Pin Voltage	$V_{\text{RES max,}}$		41	V
Allowable Power Dissipation	$P_d \text{ max}$		500	mW
Operating Temperature	T_{opr}		-40 to +85	$^\circ\text{C}$
Storage Temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

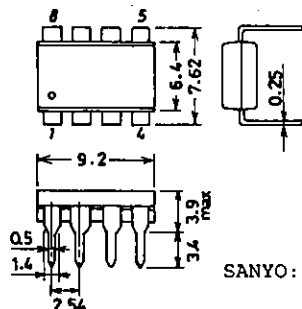
*: A PNP transistor is connected to the LA5691D, 5691S externally to provide a low-saturation voltage regulator. Therefore, $I_{\text{CONT}} \approx 100\text{mA}$ will flow, as starting current, in the V_{CC} range where the output cannot be regulated.

Operating Conditions at $T_a = 25^\circ\text{C}$

				unit
Control Pin Voltage	V_{CONT}		6 to 40	V
Control Pin Current	$I_{\text{CONT max}}$		10	mA
Reset Output Current	$I_{\text{RES max,}}$	External R pull-up (with pull-up R 10k Ω)	8	mA
Reset Detection Voltage	$V_s \text{ min}$		4	V

**Package Dimensions
(unit: mm)**

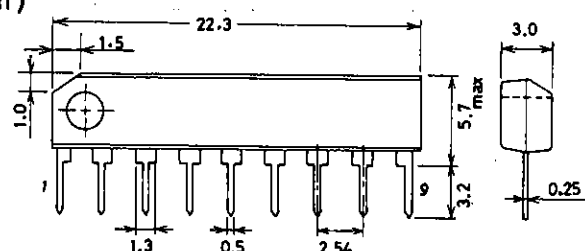
3001B



SANYO: DIP8

**Package Dimensions
(unit: mm)**

3017B



SANYO: SEP9

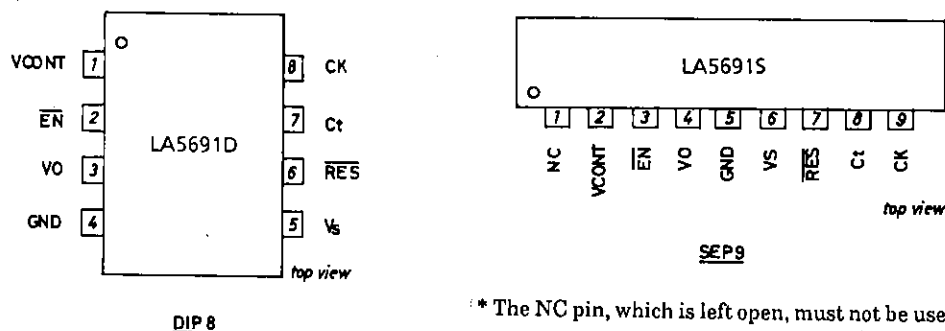
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TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

LA5691D,5691S

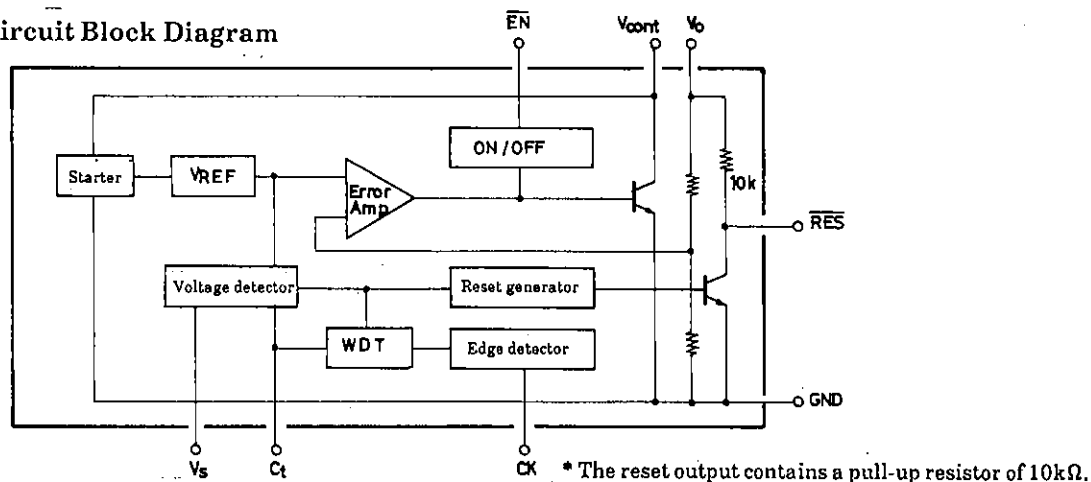
Operating Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 14\text{V}$, $I_O = 50\text{mA}$, unless otherwise specified.

	See specified Test Circuit.	min	typ	max	unit
Output Voltage	V_O	4.8	5.0	5.2	V
Line Regulation	ΔV_{OLN1} $9\text{V} \leq V_{CC} \leq 16\text{V}$		2	10	mV
	ΔV_{OLN2} $6\text{V} \leq V_{CC} \leq 40\text{V}$		4	30	mV
Load Regulation	ΔV_{OLD} $1\text{mA} \leq I_O \leq 50\text{mA}$		4	30	mV
Current Dissipation	I_{CC} $I_O = 0$		4.1	6.5	mA
Output Noise Voltage	V_{NO} $10\text{Hz} \leq f \leq 100\text{kHz}$, $V_{CK} = 0$		200		μV
Temperature Coefficient of Output Voltage	$\Delta V_O / \Delta T_a$ $I_O = 5\text{mA}$, $-40^\circ\text{C} \leq T_a \leq +85^\circ\text{C}$	± 0.2			$\text{mV}/^\circ\text{C}$
Reference Voltage	V_{REF}	1.13	1.18	1.23	V
"H"-Level CK Input Voltage	V_{IH}	2			V
"L"-Level CK Input Voltage	V_{IL}			0.8	V
"H"-Level CK Input Current	I_{IH} $V_{CK} = 5\text{V}$		0.3	0.7	mA
"L"-Level CK Input Current	I_{IL} $V_{CK} = 0$	-1.0	-0.1		μA
"H"-Level Reset Output Voltage	V_{ORH}	4.8	5.0	5.2	V
"L"-Level Reset Output Voltage 1	V_{ORL1}		40	200	mV
"L"-Level Reset Output Voltage 2	V_{ORL2} $I_{RES} = 8\text{mA}$		0.16	0.8	V
CK Input Pulse Width	t_{CKW} $V_{CK} = 5\text{V}$	3			μs
Reset Output Delay Time	t_d $C_t = 1\mu\text{F}$	7.5	10	12.5	ms
Watchdog Time	t_{WD} $C_t = 1\mu\text{F}$	3.8	5.0	6.2	ms
Watchdog Reset Time	t_{WR} $C_t = 1\mu\text{F}$	0.1	0.25	0.4	ms
Reset Hysteresis Voltage	V_{hys} $V_S = 4.5\text{V}$	100	200	300	mV
"L"-Level Output Voltage	$V_{O\text{OFF}}$ $V_{EN} = 5\text{V}$		150	300	mV
Quiescent Current	$I_{Q\text{OFF}}$ $V_{EN} = 5\text{V}$		300	600	μA
Output OFF Control Voltage	V_{ENH} Output OFF	2			V
Output ON Control Voltage	V_{ENL} Output ON			0.8	V

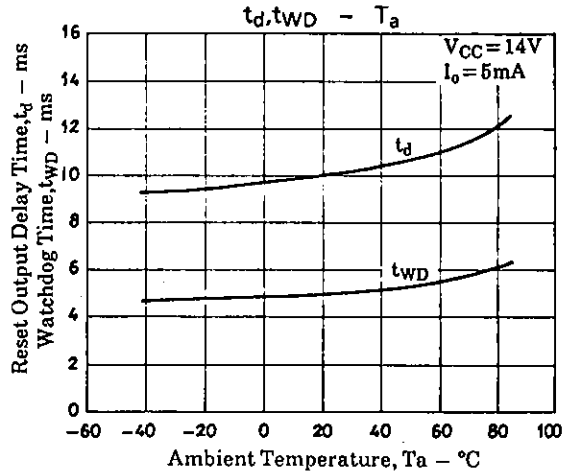
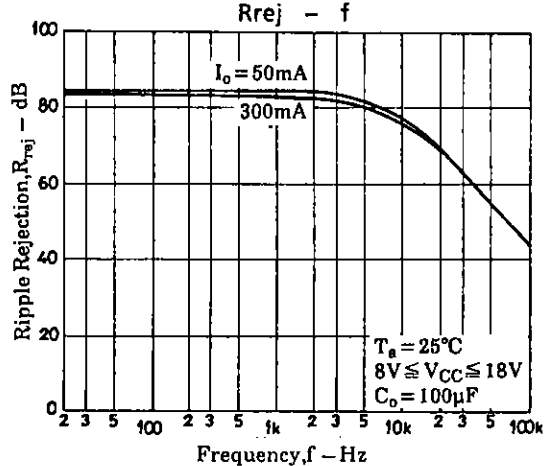
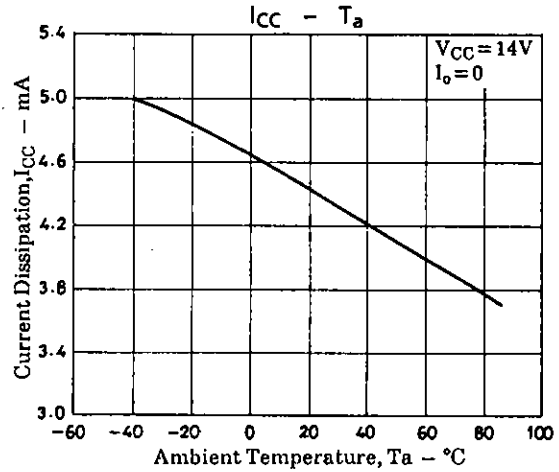
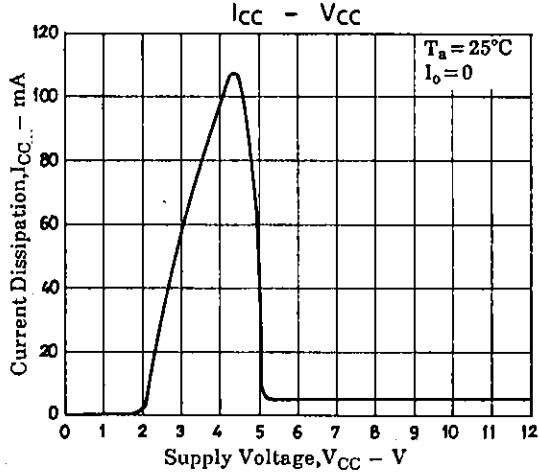
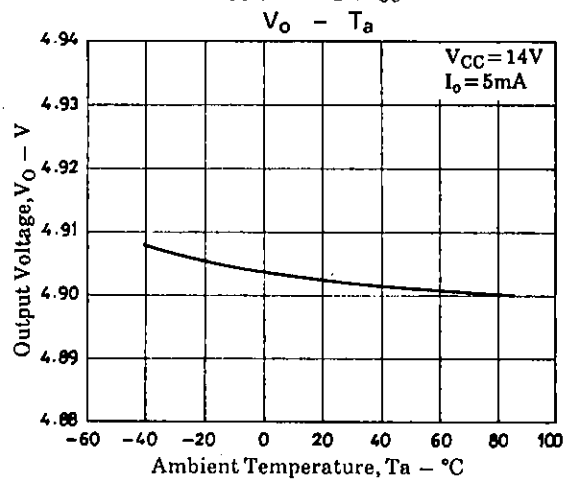
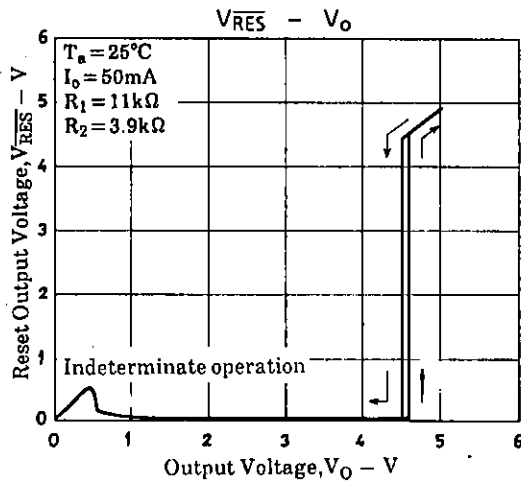
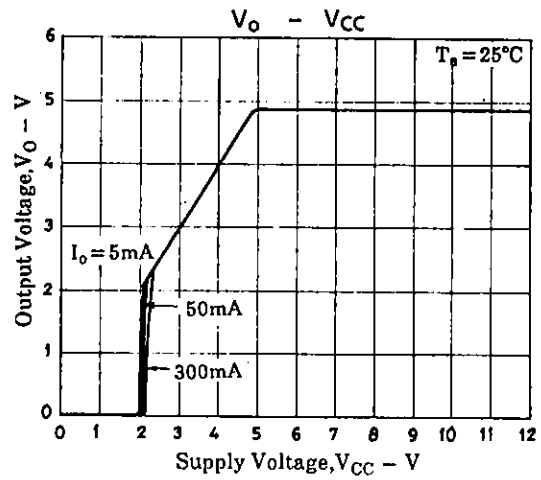
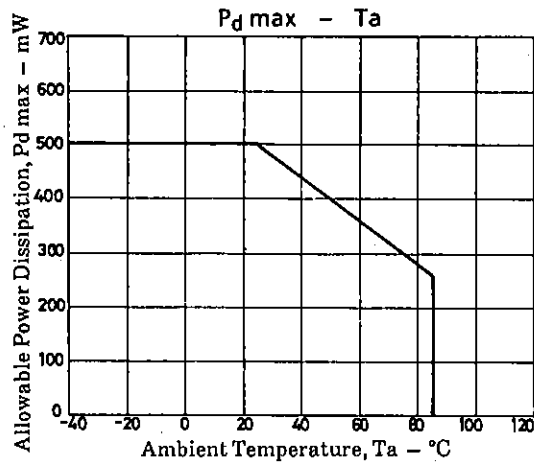
Pin Assignment

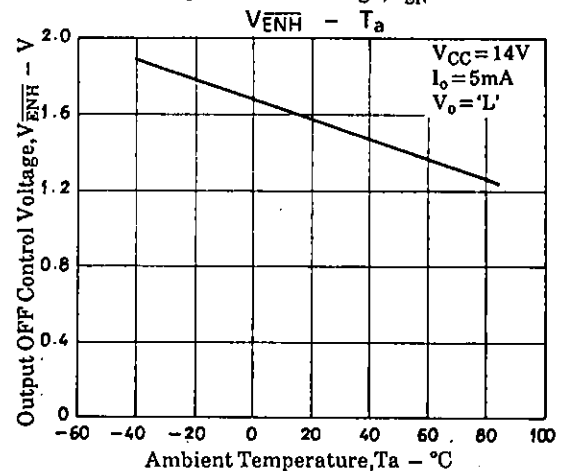
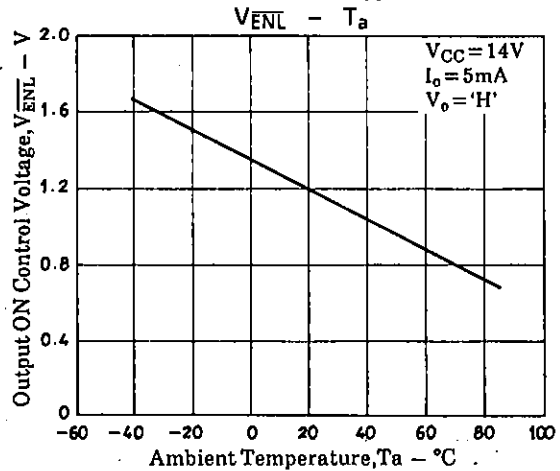
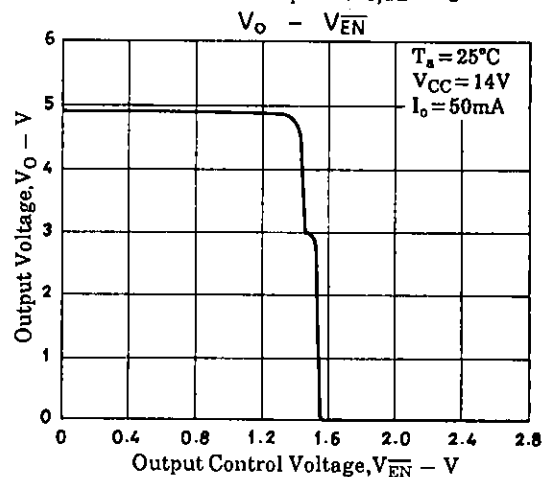
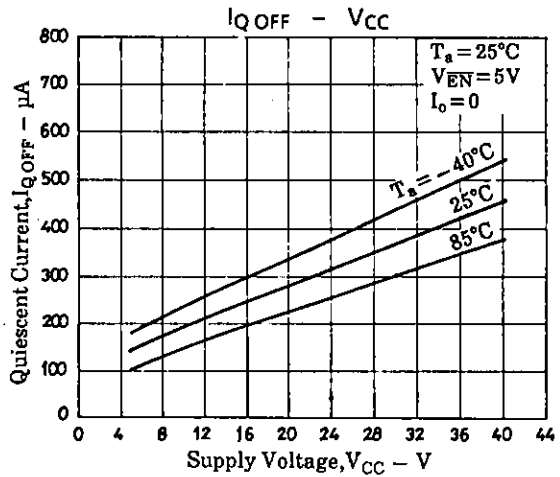
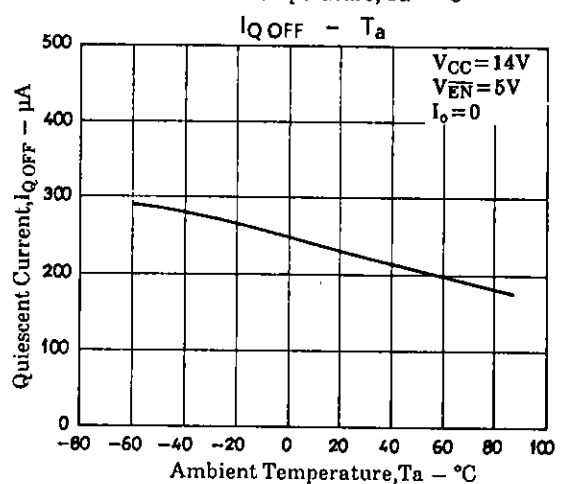
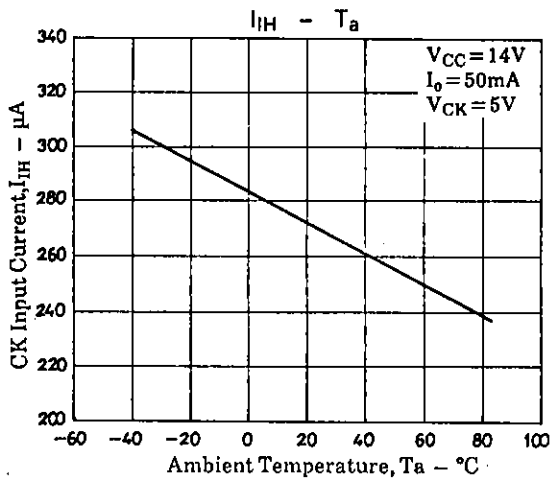
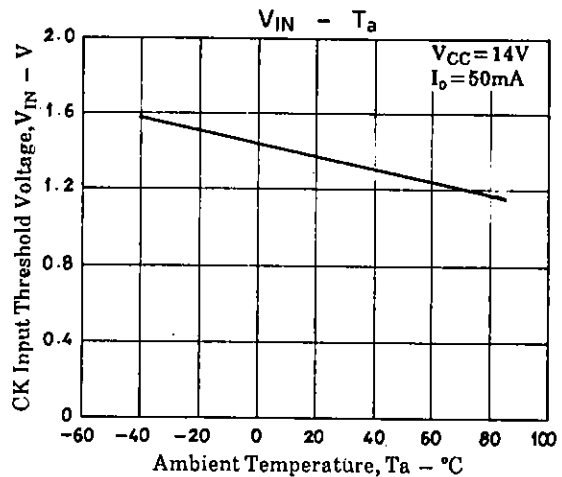
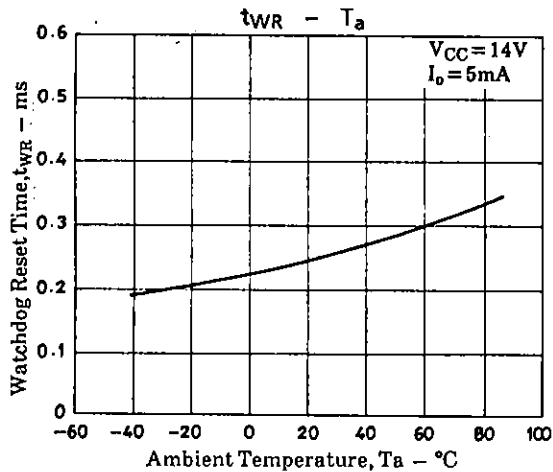


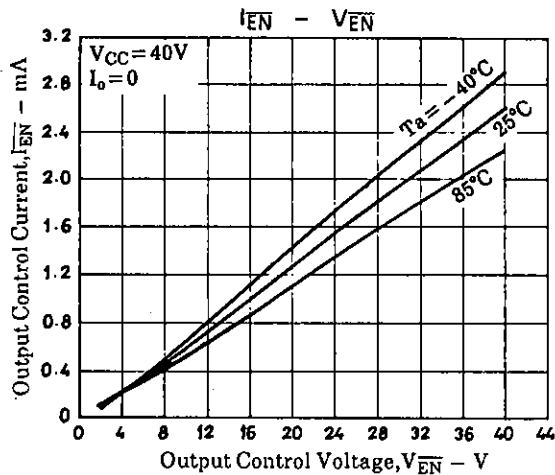
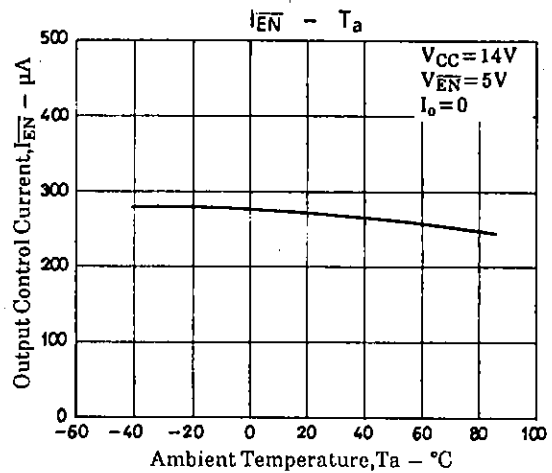
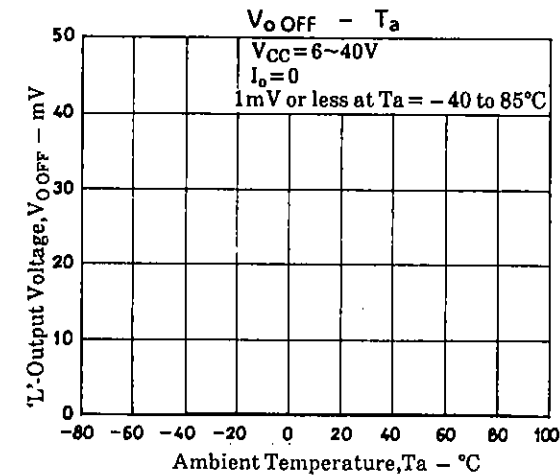
Equivalent Circuit Block Diagram



Unit (resistance: Ω)







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