

SANYO

No.1967B

LA6082D,6082S**J-FET Input
Dual Operational Amplifiers**

The LA6082 is a J-FET input dual operational amplifier. Application areas include general-purpose control equipment, measuring equipment (very low current measurement, long-integrating circuit, sample & hold circuit, impedance converter, etc.).

Features

- High slew rate
- High input impedance
- Low input bias current
- Low input offset current
- No phase compensation required

Maximum Ratings at Ta=25°C

			unit
Maximum Supply Voltage	V_{CC}/V_{EE}	± 18	V
Differential Input Voltage	V_{ID}	± 30	V
Common-Mode Input Voltage	V_{IN} (Note)	± 15	V
Allowable Power Dissipation	P_d max	570	mW
Operating Temperature	T_{opr}	-30 to +85	°C
Storage Temperature	T_{stg}	-55 to +125	°C

(Note) Allowable in the range of supply voltage. The above value is for $V_{CC}=+15V$, $V_{EE}=-15V$.

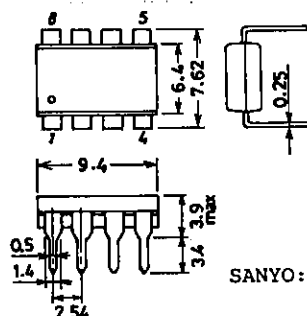
Operating Characteristics at Ta=25°C, $V_{CC}=+15V$, $V_{EE}=-15V$

		min	typ	max	unit
Input Offset Voltage	V_{IO} $R_S=50\text{ohms}$		5.0	15.0	mV
Input Offset Current	I_{IO}		5	200	pA
Input Bias Current	I_B		30	400	pA
Common-Mode Input Voltage Range	V_{ICM}	± 10			V
Common-Mode Rejection Ratio	CMR	70	76		dB
Large Amplitude Voltage Gain	VG $R_L \geq 2\text{kohms}, V_o = \pm 10V$	25	200		V/mV
Maximum Output Voltage	V_{opp1} $R_L \geq 10\text{kohms}$	± 12	± 13.5		V
	V_{opp2} $R_L \geq 2\text{kohms}$	± 10	± 12		V

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**Package Dimensions 3001B-D8IC
(unit: mm)**

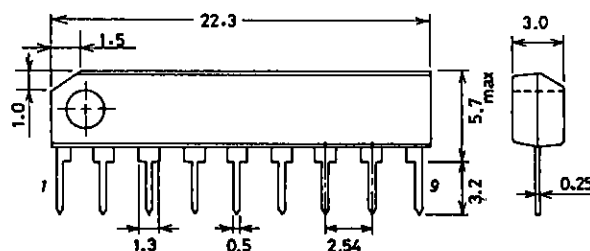
[LA6082D]



SANYO: DIP8

**Package Dimensions 3017B-S9IC
(unit: mm)**

[LA6082S]



SANYO: SEP9

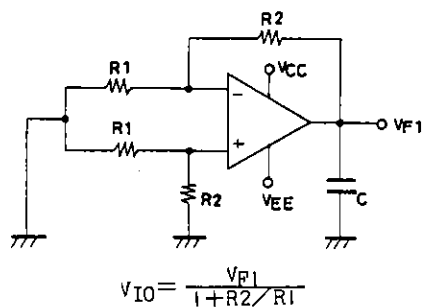
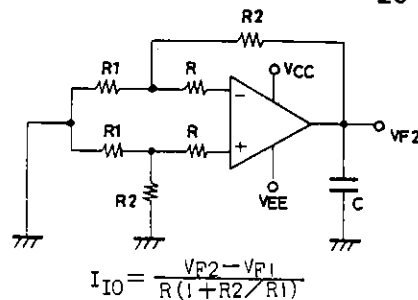
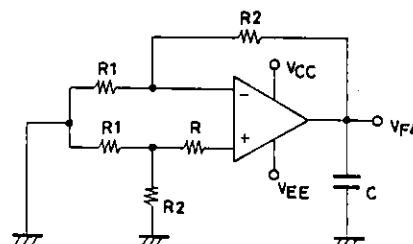
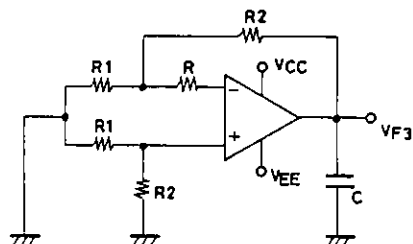
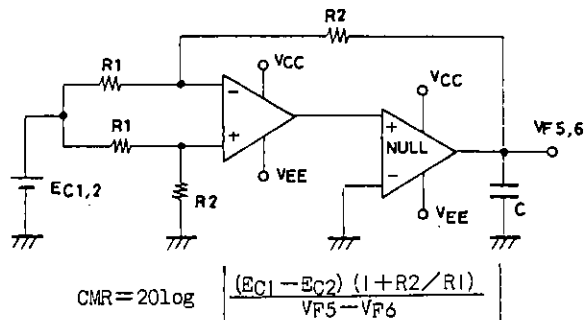
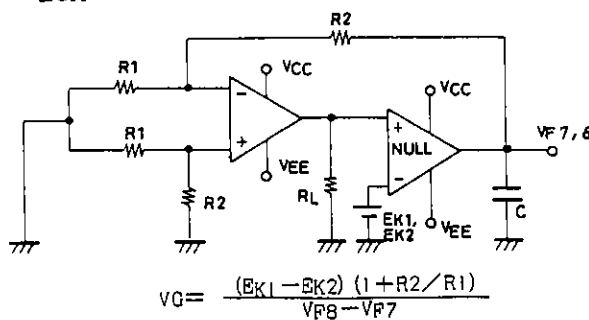
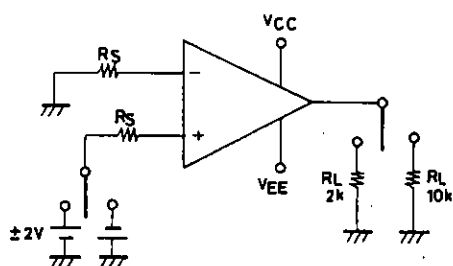
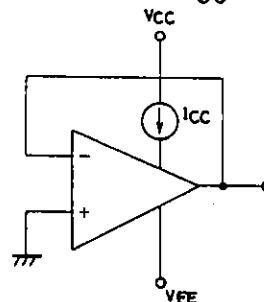
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1100YT/8077KI/0285MW, TS No1967-1/5

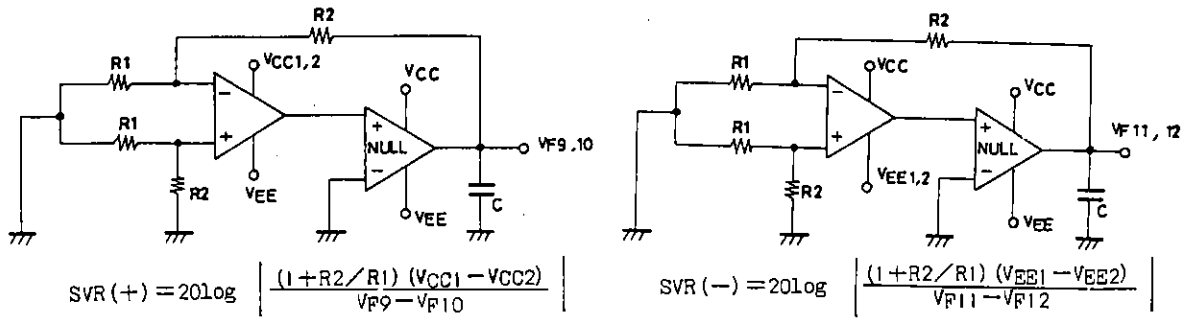
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			min	typ	max	unit
Supply Voltage Rejection Ratio	SVR		70	76		dB
Supply Current	I_{CC}	$R_L = \infty$		4	5.6	mA
Gain-Bandwidth Product	f_T	$A_V = 1$		3		MHz
Equivalent Input Noise Voltage	V_{NI}	$R_S = 100\text{ohms},$ $f = 10\text{Hz to } 10\text{kHz}$		4		μVrms
Input Resistance	r_i			10^{12}		ohm
Channel Separation	C.S			120		dB
Slew Rate	S.R	$R_L = 2\text{kohms}, C_L = 100\text{pF},$ $A_V = 1, V_{IN} = 10\text{V}$		13		V/us

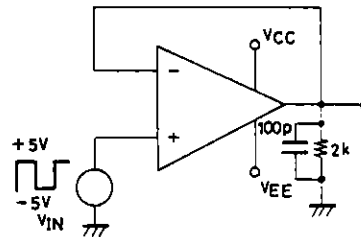
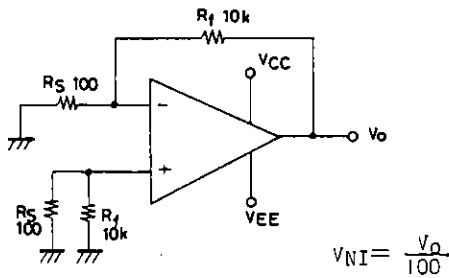
Test Circuits

1. Input Offset Voltage V_{IO} 2. Input Offset Current I_{IO} 3. Input Bias Current I_B 4. Common-Mode Rejection Ratio CMR
Common-Mode Input Voltage Range V_{ICM} 5. Voltage Gain V_G 6. Maximum Output Voltage V_{OPP} 7. Supply Current I_{CC} Unit (resistance: Ω)

8. Supply Voltage Rejection Ratio SVR

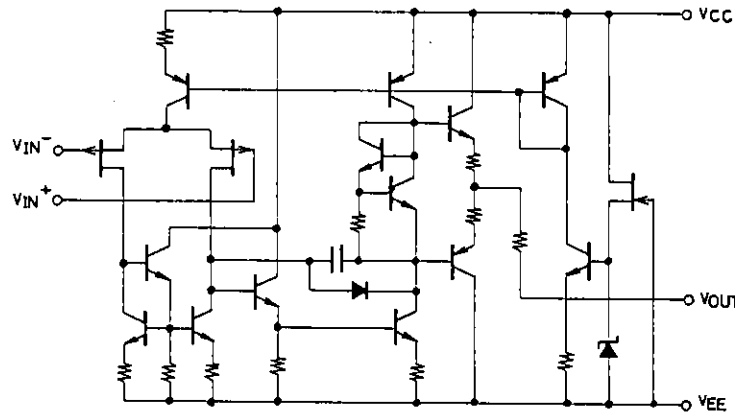


9. Equivalent Input Noise Voltage V_{NI} 10. Slew Rate SR

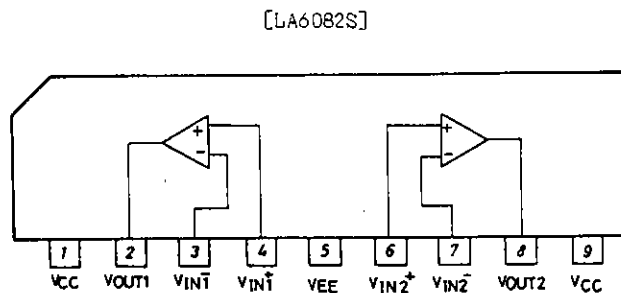
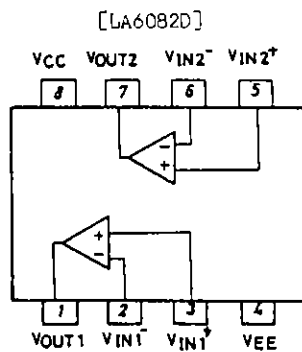


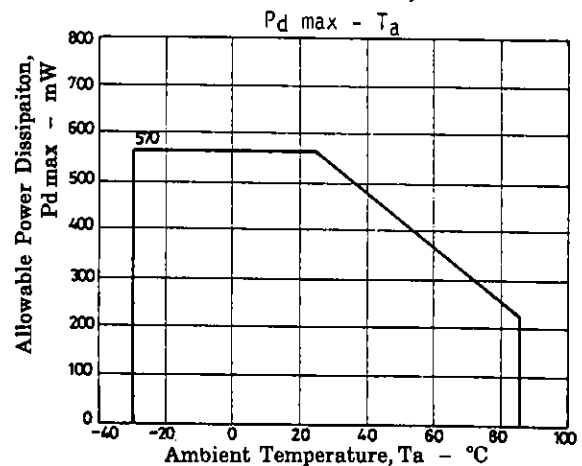
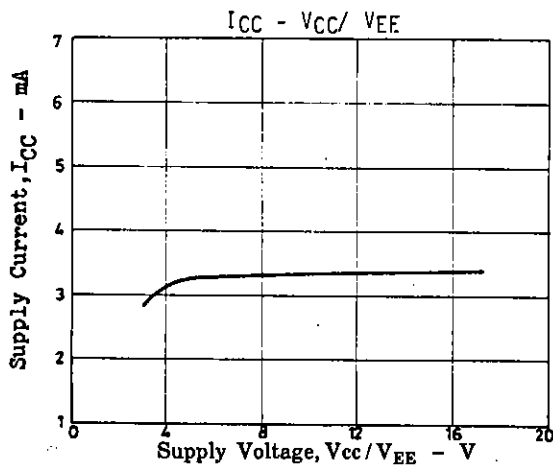
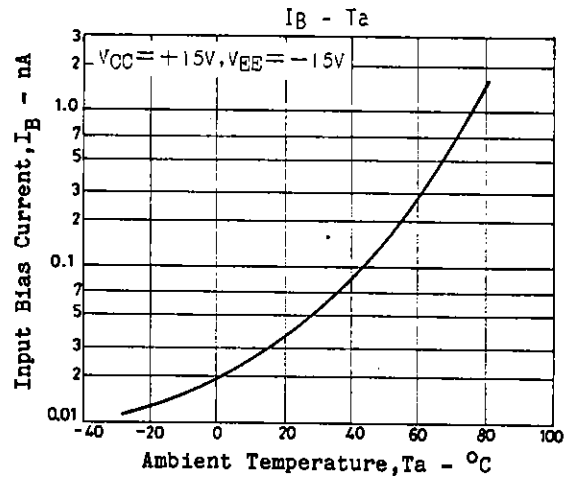
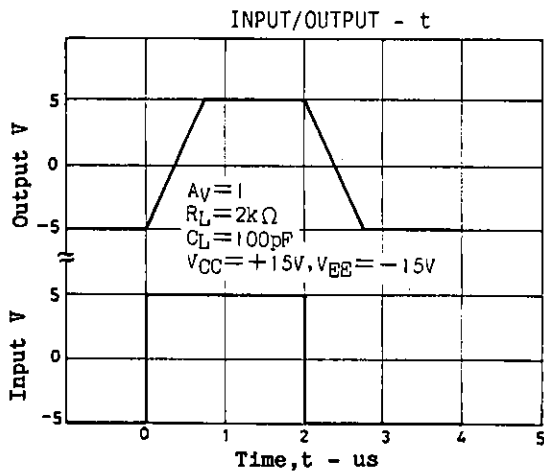
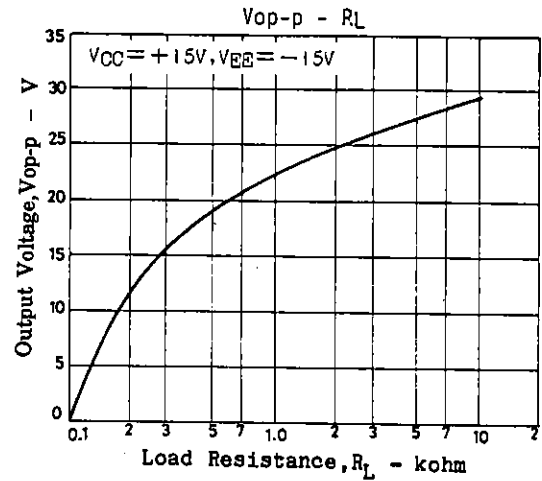
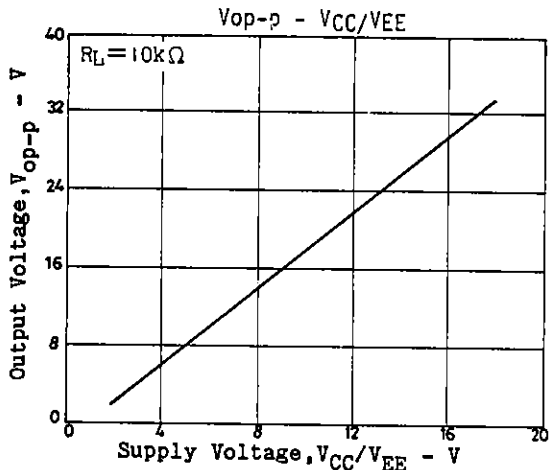
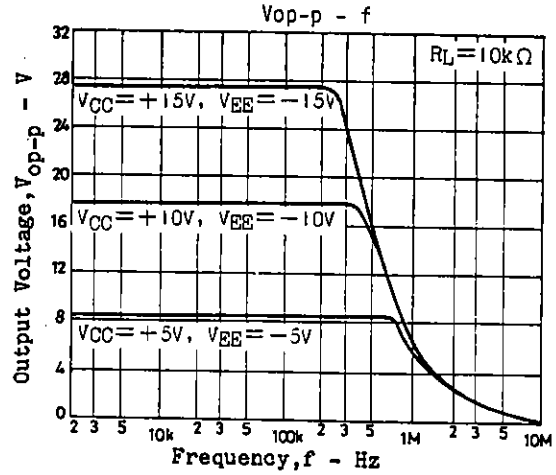
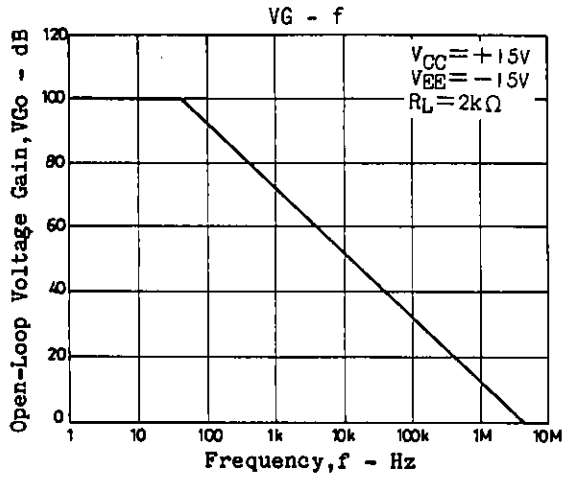
Equivalent Circuit

Unit (resistance:Ω capacitance:F)

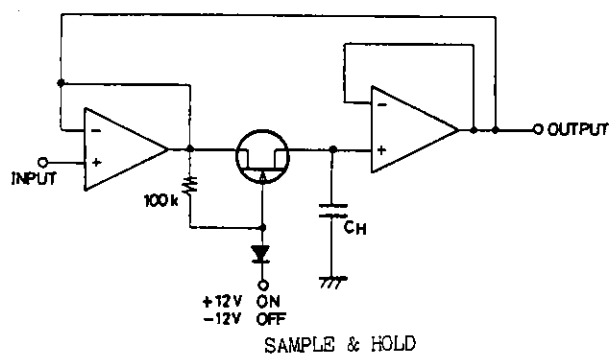
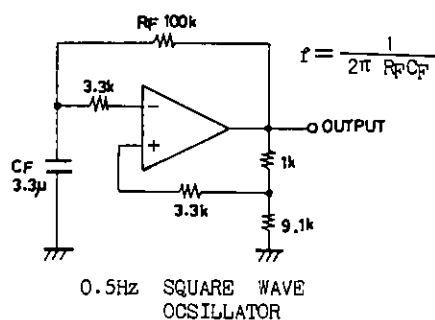


Pin Assignment





Application Circuits

Unit (resistance: Ω , capacitance: F)

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