

SANYO

No.1958A

LA6083D**J-FET Input
Dual Operational Amplifier**

The LA6083D is a J-FET input dual operational amplifier. Application areas include general-purpose control equipment, measuring equipment (very low current measurement, long-integrating circuit, sample & hold circuit, impedance converter, etc.).

Features

- High slew rate
- High input impedance
- Low input bias current
- Low input offset current
- No phase compensation required
- With offset null pins

Maximum Ratings at $T_a=25^{\circ}\text{C}$

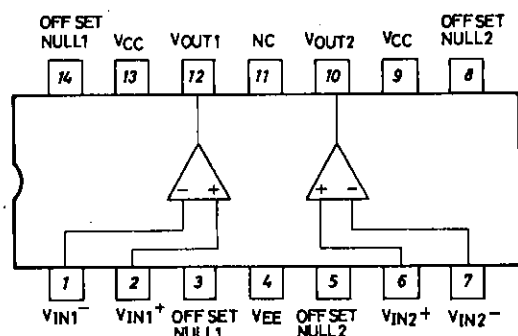
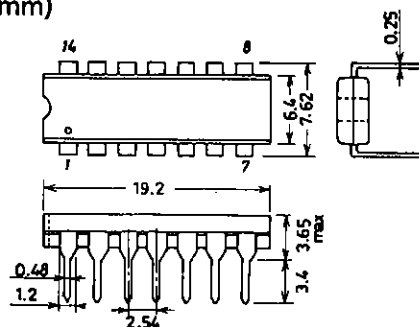
			unit
Maximum Supply Voltage	V_{CC}/V_{EE}	± 18	V
Differential Input Voltage	V_{ID}	± 30	V
Common-Mode Input Voltage	V_{IN} (Note)	± 15	V
Allowable Power Dissipation	P_d max	720	mW
Operating Temperature	T_{opr}	-30 to +85	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	-55 to +125	$^{\circ}\text{C}$

(Note) Allowable in the range of supply voltage. The above value is for $V_{CC}=+15\text{V}$, $V_{EE}=-15\text{V}$.

Operating Characteristics at $T_a=25^{\circ}\text{C}$, $V_{CC}=+15\text{V}$, $V_{EE}=-15\text{V}$

		min	typ	max	unit
Input Offset Voltage	V_{IO} $R_S=50\text{ohms}$		5.0	15.0	mV
Input Offset Current	I_{IO}		5	200	pA
Input Bias Current	I_B		30	400	pA
Common-Mode Input Voltage Range	V_{ICM}	± 10			V
Common-Mode Rejection Ratio	CMR	70	76		dB
Large Amplitude Voltage Gain	V_G $R_L \geq 2\text{kohms}$, $V_o = \pm 10\text{V}$	25	200		V/mV
Maximum Output Voltage	V_{opp1} $R_L \geq 10\text{kohms}$	± 12	± 13.5		V
	V_{opp2} $R_L \geq 2\text{kohms}$	± 10	± 12		V

Continued on next page.

Pin Assignment**Package Dimensions 3003A-D14IC
(unit : mm)**

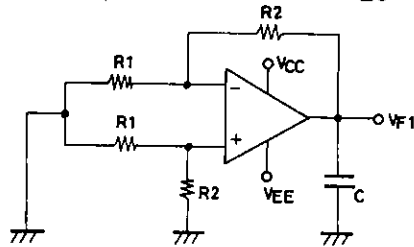
SANYO: DIP14

SANYO Electric Co., Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

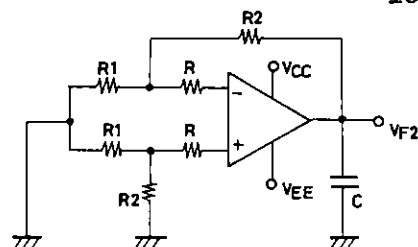
8067KI/0285MW, TS №1958-1/5

Continued from preceding page.

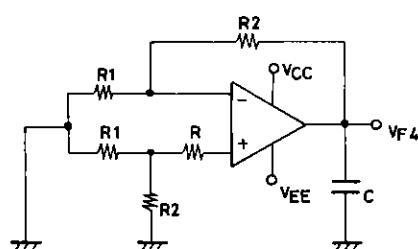
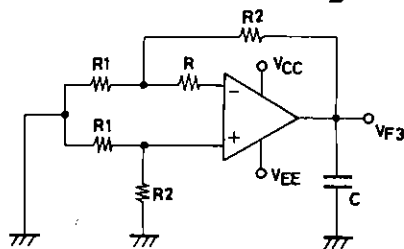
			min	typ	max	unit
Supply Voltage Rejection Ratio	SVR		70	76		dB
Supply Current	I_{CC}	$R_L = \infty$		4	5.6	mA
Gain-Bandwidth Product	f_T	$A_V = 1$		3		MHz
Equivalent Input Noise Voltage	V_{NI}	$R_S = 100\text{ohms},$ $f = 10\text{Hz to } 10\text{kHz}$		4		μVrms
Input Resistance	r_i			10^{12}		ohm
Channel Separation	ch sep			120		dB
Slew Rate	S·R	$R_L = 2\text{kohms}, C_L = 100\text{pF},$ $A_V = 1, V_{IN} = 10\text{V}$		13		V/us

Test Circuits**1. Input Offset Voltage V_{IO}** 

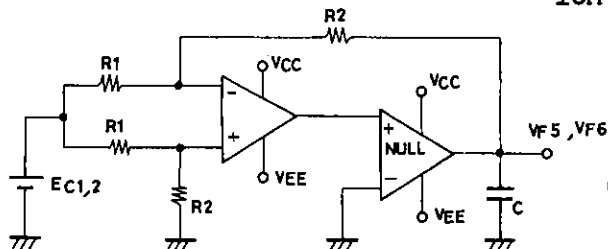
$$V_{IO} = \frac{VF1}{1 + R2/R1}$$

2. Input Offset Current I_{IO} 

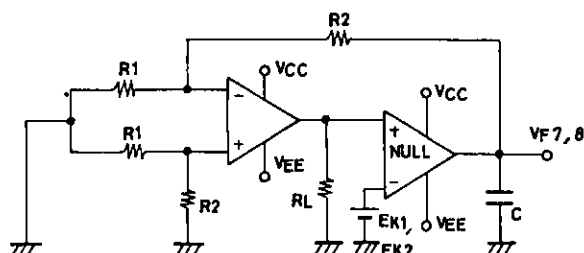
$$I_{IO} = \frac{VF2 - VF1}{R(1 + R2/R1)}$$

3. Input Bias Current I_B 

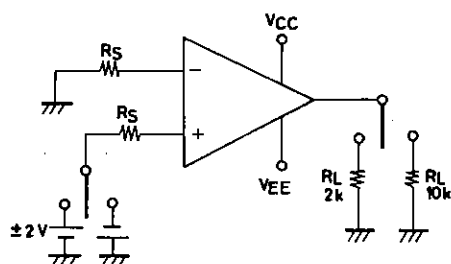
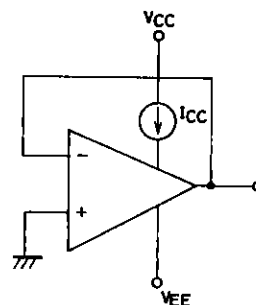
$$I_B = \frac{VF4 - VF3}{2R(1 + R2/R1)}$$

**4. Common-Mode Rejection Ratio CMR
Common-Mode Input Voltage Range V_{ICM}** 

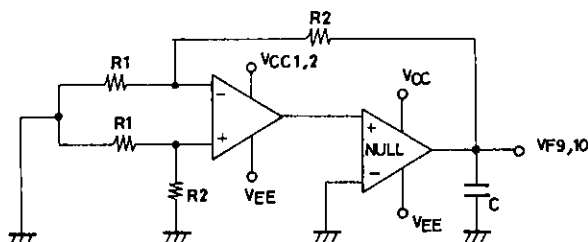
$$CMR = 20 \log \left| \frac{(EC1 - EC2)(1 + R2/R1)}{VF5 - VF6} \right|$$

5. Voltage Gain V_G 

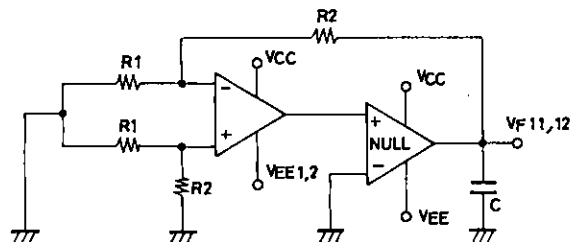
$$V_G = \frac{(EK1 - EK2)(1 + R2/R1)}{VF8 - VF7}$$

6. Maximum Output Voltage V_{opp} Unit (resistance: Ω)7. Supply Current I_{CC} 

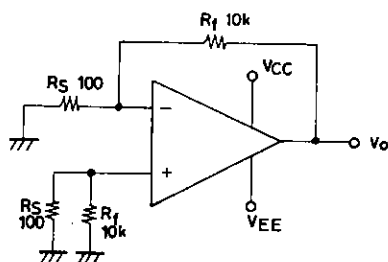
8. Supply Voltage Rejection Ratio SVR



$$SVR (+) = 20 \log \left| \frac{(1 + R2/R1) (V_{CC1} - V_{CC2})}{V_{F9} - V_{F10}} \right|$$

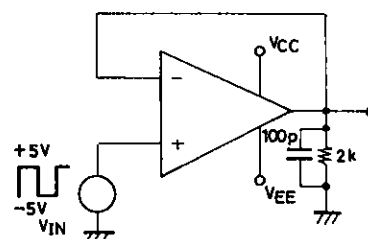


$$SVR (-) = 20 \log \left| \frac{(1 + R2/R1) (V_{EE1} - V_{EE2})}{V_{F11} - V_{F12}} \right|$$

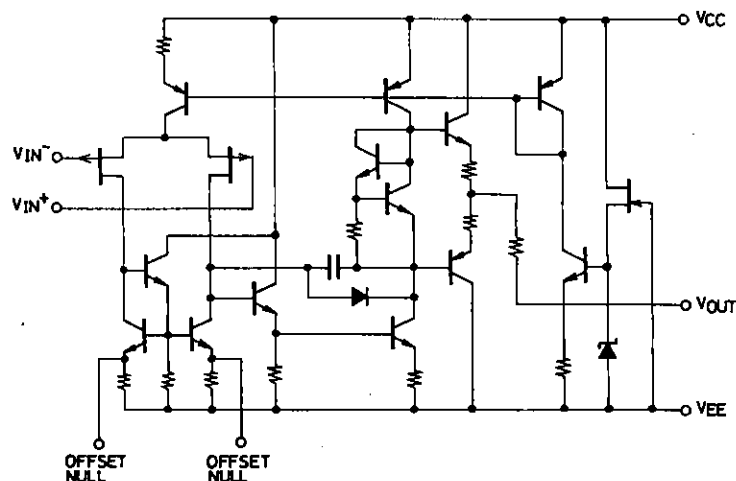
9. Equivalent Input Noise Voltage V_{NI} 

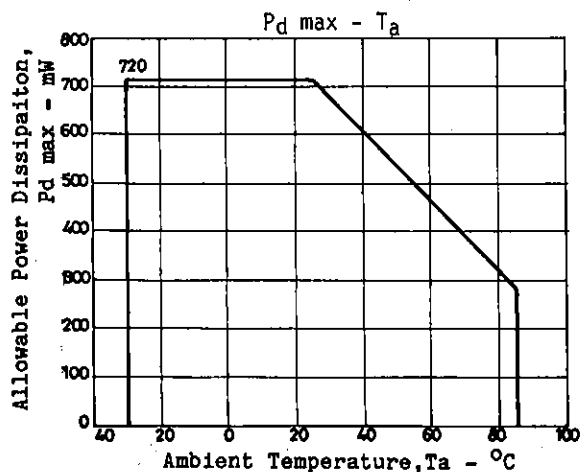
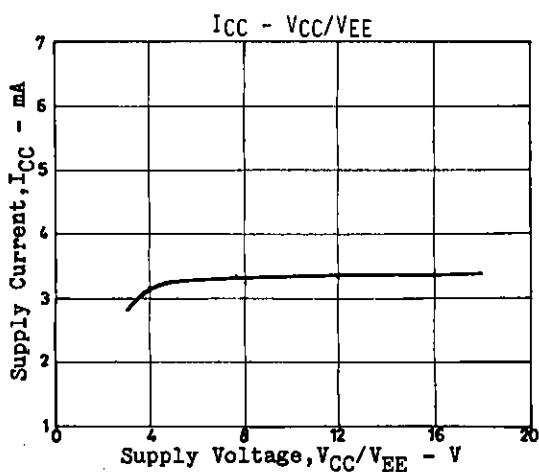
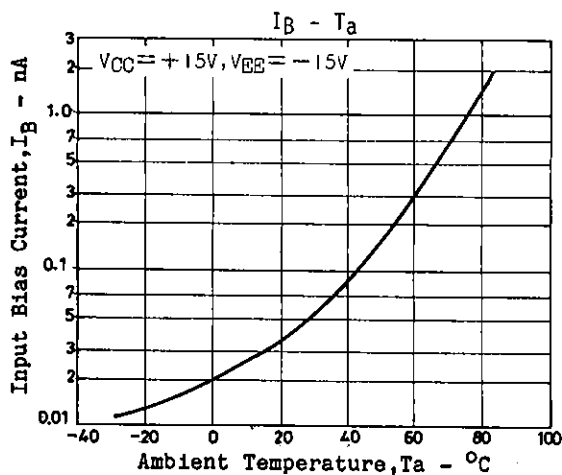
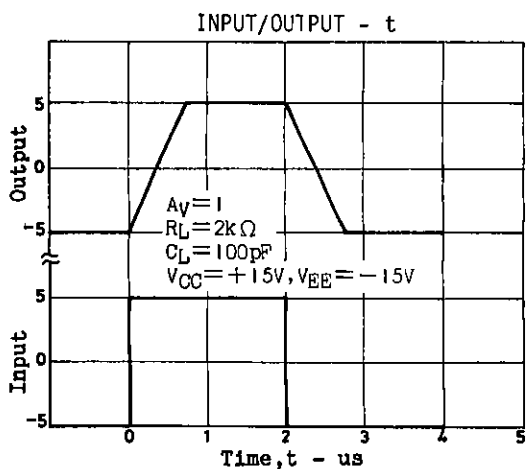
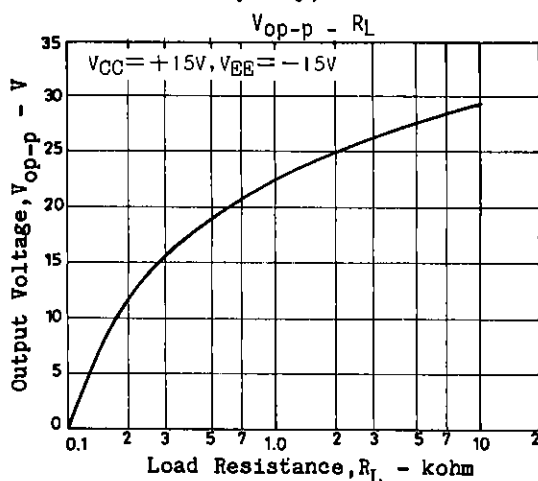
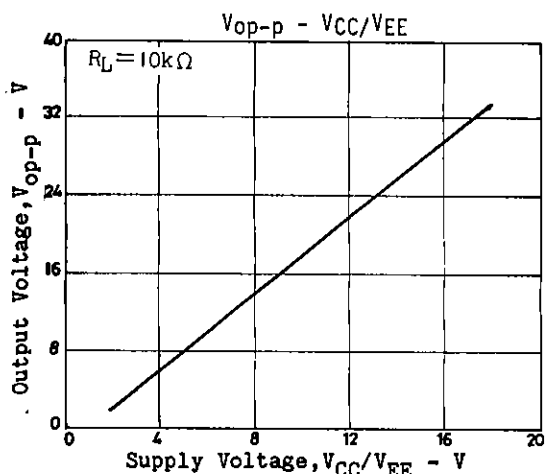
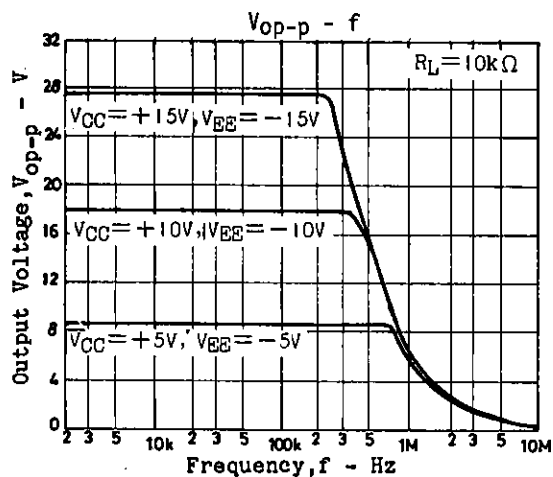
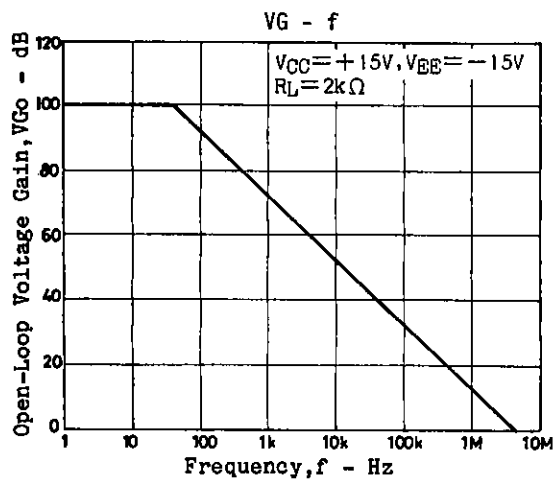
$$V_{NI} = \frac{V_O}{100}$$

10. Slew Rate SR

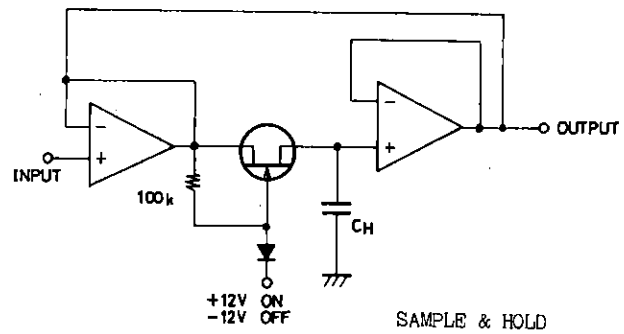
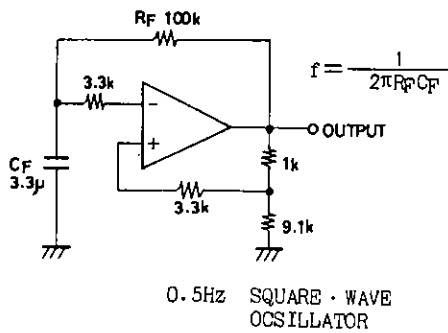
Unit (resistance: Ω capacitance: F)

Equivalent Circuit



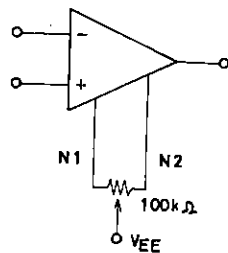


Sample Application Circuits



Unit (resistance:Ω capacitance:F)

Voltage offset adjust circuit



- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use;
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.