



LA7780M

QPSK Downconverter for CATV Systems

Overview

The LA7780M is a downconverter for QPSK data demodulation for digital CATV transmission. This IC integrates a preamplifier, an AGC amplifier, a mixer, an oscillator, a post-amplifier, and other circuits in a single chip, and provides all the functions required from cable signal input through output to the A/D converter.

Features

- Since a preamplifier is built in, the LA7780M has adequate sensitivity to handle the input signal from the cable directly.
(Input signal level: -30 to +30 dBm)
- Both internal and external AGC are supported as the AGC amplifier drive technique.
- The output amplitude of the post amplifier used to drive the A/D converter is 2 Vp-p (typical).
- Applications can be designed to use either a crystal or an inductor oscillator.

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max	Pins 5, 6, and 17	7.0	V
Circuit voltage	V max	Pins 4, 12, and 24	V _{CC}	V
Circuit current	I ₄	The pin 4 output current	30	mA
	I ₁₃	The pin 13 sink current	2	mA
	I ₁₆	The pin 16 sink current	2	mA
Allowable power dissipation	Pd max	Ta ≤ 70°C	540	mW
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-55 to +150	°C

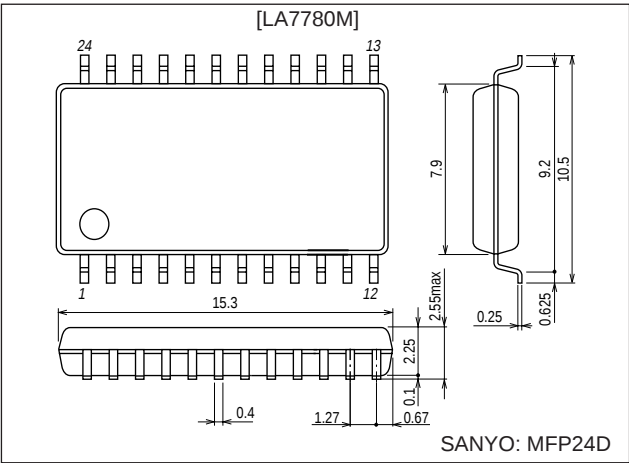
Functions

- Preamplifier
- AGC amplifier
- Mixer
- Oscillator
- Post amplifier
- IF AGC (internal/external)
- AGC detector

Package Dimensions

unit: mm

3108-MFP24D



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Operating Conditions at $T_a = 25^\circ\text{C}$

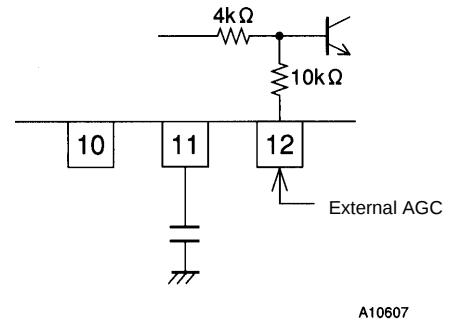
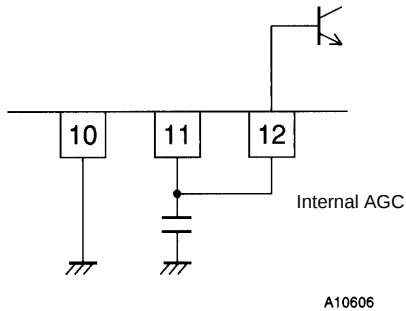
Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}	Pins 5, 6, and 17	5.0	V
Operating supply voltage range	$V_{CC\text{ op}}$	Pins 5, 6, and 17	4.5 to 5.5	V

AC Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$, internal AGC mode, Pin 24 is left open.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit current	I_{total}	Pins 4, 5, 6, and 17: no signal	64	80	95	mA
RF input frequency range	$f_{\text{(in)}}$	Pins 1, 8, and 9	30		150	MHz
IF output level	$V_{O(\text{IF})}$	Pin 13: *1	1.6	2.0	2.5	Vp-p
IF output IM3	$V_{O(\text{IM3})}$	Pin 13: *2	40			dB
IF output frequency bandwidth	BW	Pin 13: *3	15			MHz
Local oscillator frequency range	$f_{\text{(LO)}}$	Pins 18, 19, 20, and 21	30		200	MHz
AGC amplifier input sensitivity	$V_{\text{in(RF2)}}$	Pins 8 and 9: *4	-25	-21	-17	dBmV
AGC range	GR	Pin 13: IF output level $< \pm 1\text{ dB}$	60	80		dB
AGC flatness	$\Delta V_{O(\text{IF})}$	Pin 13: Compare with the state when $V_{\text{in(RF2)}} = 30\text{ dBmV}$	-1	0	+1	dB
Preamplifier gain	$G_{\text{(RF1)}}$	Pin 4: *5	17	19	21	dB
Maximum preamplifier output level	$V_{O\text{max}}$	Pin 4: *6	50			dBmV
Oscillator output level	$V_{O(\text{OSC})}$	Pin 23: The pin 23 frequency is 1/2 that of the local oscillator	500	800	1000	mVp-p

Operating Modes

Mode	Pin 10	Pin 11	Pin 12
Internal AGC	GND	With a capacitor between pin 11 and ground	Connected to pin 11
External AGC (Narrow control range: 3 to 5 V)	GND (AGC divider inactive)	With a capacitor between pin 11 and ground	External AGC voltage supply Pin 12 = high impedance
External AGC (Wide control range: 0 to 5 V)	Open (AGC divider active)	With a capacitor between pin 11 and ground	External AGC voltage supply Pin 12 = low impedance (14 k Ω)



Note: In internal AGC mode, the IF output level can be adjusted by varying the pin 24 DC voltage.

Caution:

Note 1.

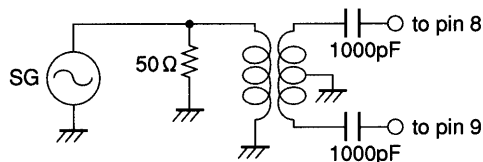
Input: SG = 69.55 MHz, 20 dBm V

Other conditions:

Internal AGC mode

Pin 24 left open.

Output: The post amplifier output (pin 13) at 5 MHz

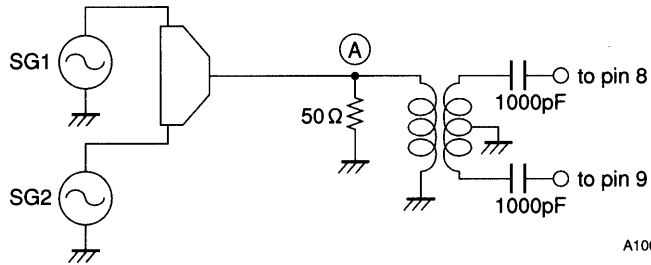


Transfer ratio = 1 : 1

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Note 2.

Input: SG1 = 69.55 MHz, SG2 = 70.55 MHz



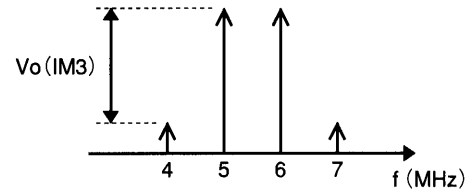
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Point (A) = 20 dBmV (69.55 MHz) + 20 dBmV (70.55 MHz)

Other conditions:

Internal AGC mode
Pin 24 left open.

Output: The post amplifier output (pin 13)



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Note 3.

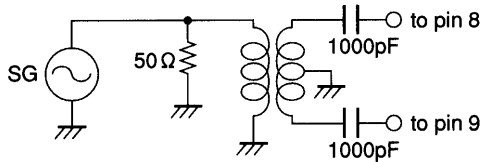
Post amplifier output level = -3 dB

Remove the low-pass filter between pins 14 and 16.

(Short the coil of 27 μ H and remove the capacitors of 27 pF and 15 pF.)

Note 4.

Input: SG1 = 69.55 MHz



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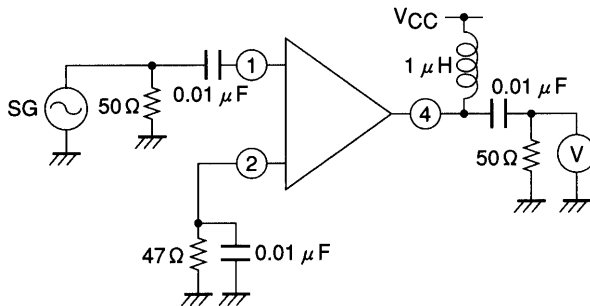
Other conditions:

Internal AGC mode
Pin 24 left open.

Output: The signal level such that the post amplifier output (pin 13) falls by -3 dB.

Note 5.

SG = 75 MHz, 20 dBm V

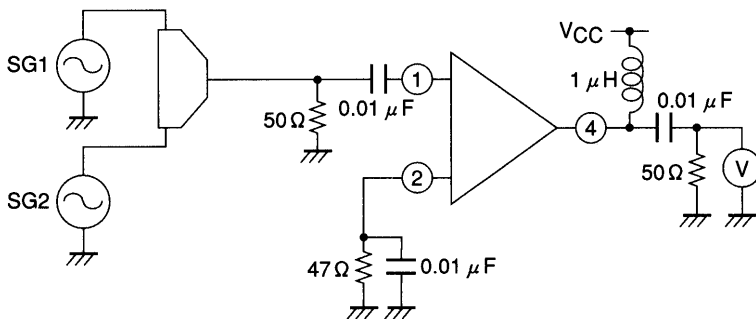


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Note 6.

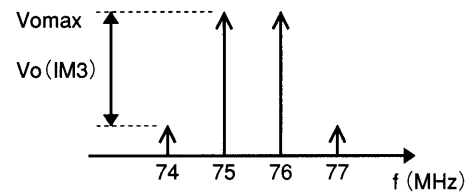
SG1 = 75 MHz, SG2 = 76 MHz,

Adjust the pin 1 level until the IM3 in the pin 4 output is 40 dB.



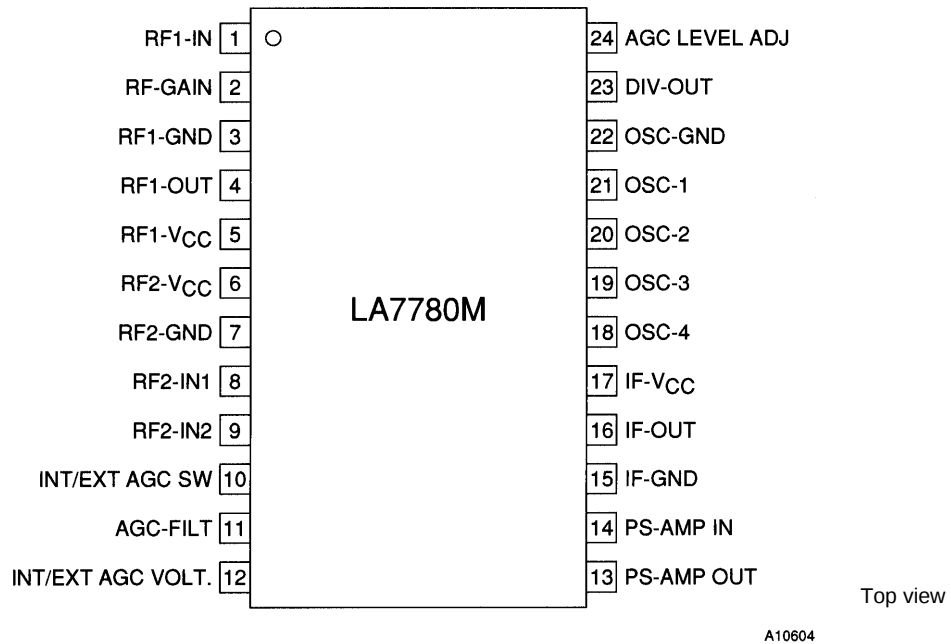
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Output: RF1-OUT (pin 4)
 $V_{O(IM3)} = 40$ dB



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Pin Assignment

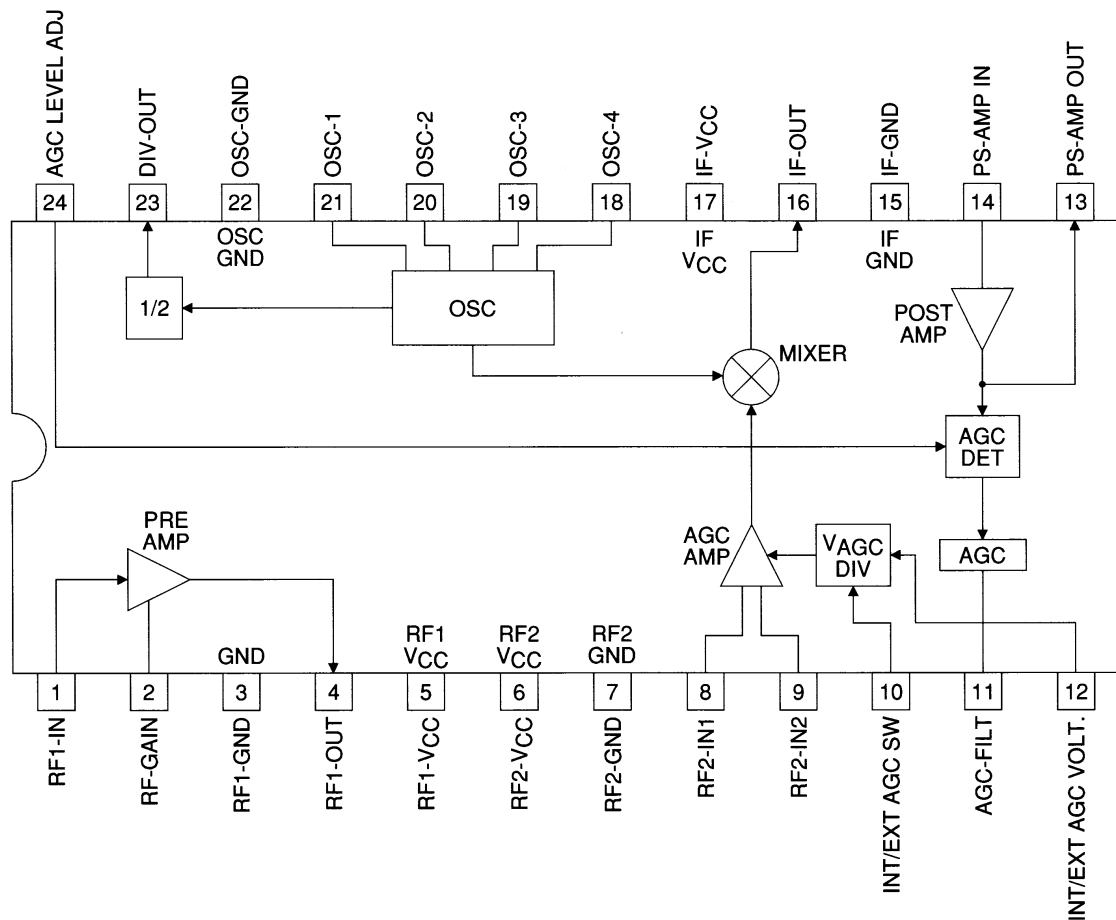


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Usage Notes

- The oscillator may stop if the power supply rise time is extremely short. To prevent this problem, insert a 500 k Ω resistor between pin 18 and ground or between pin 21 and ground. (This applies when a crystal oscillator is used.)
- This IC should be used with the pin 13 output level between 1 V_{p-p} and 2 V_{p-p}.
- Use a low-pass filter with a 6-dB attenuation between pins 14 and 16.
- Since the high-frequency process is adopted, care must be taken to prevent the influence of static electricity.

Block Diagram



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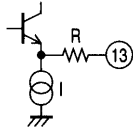
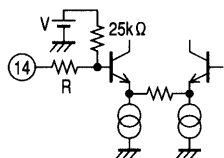
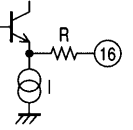
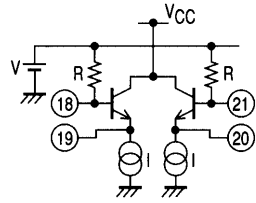
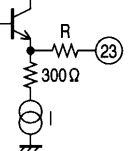
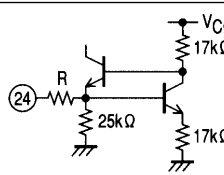
Pin Descriptions

Pin No.	Function	Pin voltage (V)	Note	Equivalent circuit
1	RF1 input	2.8		A10615
2	RF gain	1.3	Impedance connected to pin 2 must be $> 45 \Omega$	A10616
3	GND	0		
4	RF1 output	Open collector		A10617
5	V _{CC}	5.0		
6	V _{CC}	5.0		
7	GND	0		
8	RF2 input (1)	2.5	V = 2.5 V	A10618
9	RF2 input (2)	2.5	R = 1 kΩ	
10	Internal/external AGC switch	0 (GND) 1.0 (open)	Pin 10 → GND : Internal or external AGC (narrow control range) Pin 10 → open : External AGC (wide control range)	A10619
11	AGC filter 2	Open collector	I ₁ = 20 μA I ₂ = 100 μA I ₃ , I ₄ & Q ₁ are switched on and off by pin 10.	A10620
12	AGC filter 1	Open base (Pin 10 → GND) 4.0 (Pin 10 open)		

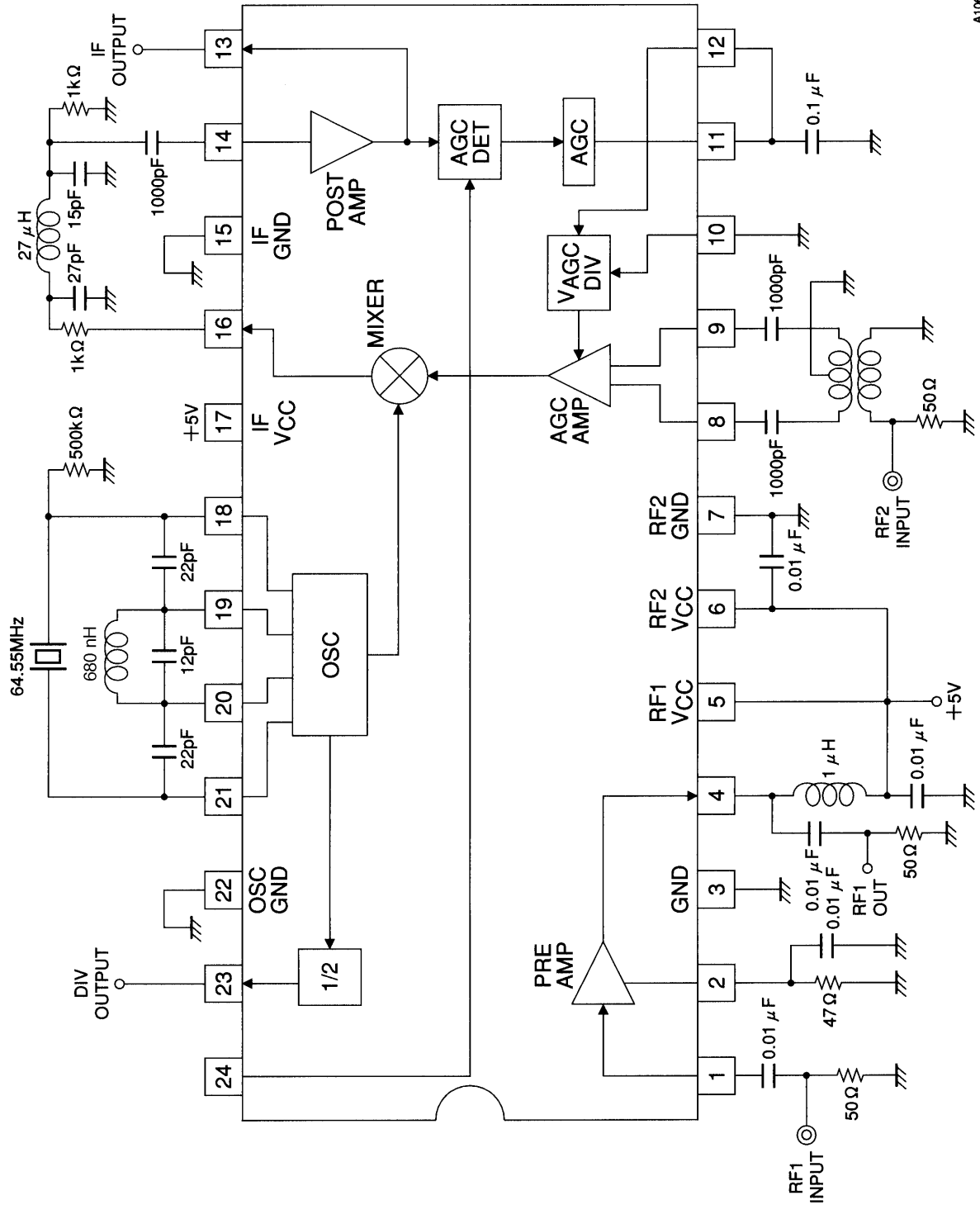
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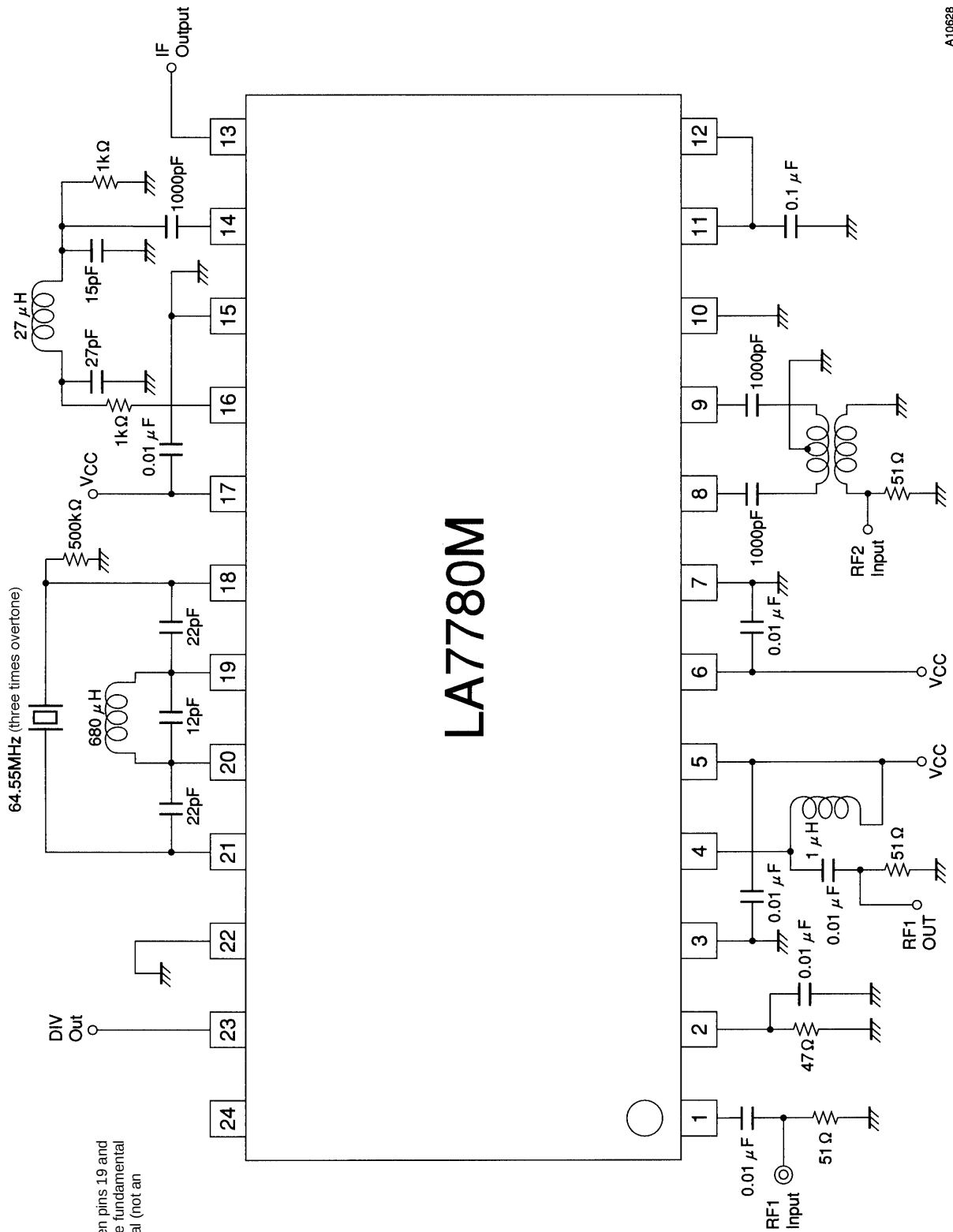
Pin No.	Function	Pin voltage (V)	Note	Equivalent circuit
13	Post-amp output	2, 3	$R = 30\ \Omega$ $I = 7\ \text{mA}$	 A10621
14	Post-amp input	2.0	$V = 2.1\ \text{V}$ $R = 300\ \Omega$	 A10622
15	GND	0		
16	IF output	1.7	$R = 100\ \Omega$ $I = 3.5\ \text{mA}$	 A10623
17	V_{CC}	5.0		
18 19 20 21	Oscillator input 4 Oscillator input 3 Oscillator input 2 Oscillator input 1	3.0 3.0	$V = 3.0\ \text{V}$ $R = 5\ \text{k}\Omega$ $I = 1\ \text{mA}$	 A10624
22	GND	0		
23	Divider output	3.3	$R = 100\ \Omega$ $I = 1\ \text{mA}$	 A10625
24	Output level adjustment	2.5	$R = 25\ \text{k}\Omega$	 A10626

Test Circuit



A10627

Sample Application Circuit



*: The choke coil between pins 19 and 20 is not required if the fundamental frequency of the crystal (not an overtone) is used.

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