

SANYO

No 4699A

LC32464P, M-80**256 K (65536 words × 4 bits) DRAM
Fast Page Mode**

Overview

The LC32464P, M is a CMOS dynamic RAM operating on a single 5 V power source and having a 65536 words × 4 bits configuration. Equipped with high speed and low power dissipation, the LC32464P, M is suited for a wide variety of applications ranging from computer main memory and expansion memory to commercial equipment. Address inputs utilizes a multiplexed address bus which permits it to be enclosed in a compact plastic package. The LC32464P, M supports $\overline{\text{CAS}}$ -before $\overline{\text{RAS}}$ refresh and $\overline{\text{RAS}}$ -only refresh within 4 ms with 256 row address (A0 to A7) selection.

Features

- 65536 words × 4 bits configuration.
- $\overline{\text{RAS}}$ access time/cycle time/power dissipation

Parameter		LC32464P, M-80
RAS access time		80 ns
Cycle time		160 ns
Power dissipation (max.)	Operating	385 mW
	Standby	5.5 mW (CMOS level)/ 11 mW (TTL level)

- Single 5 V ± 10% power supply.
- All input and output (I/O) TTL compatible.
- Supports fast page mode and read-modify-write.
- Supports output caching control using early write and Output Enable ($\overline{\text{OE}}$) control.
- 4 ms refresh using 256 refresh cycles.
- Supports $\overline{\text{RAS}}$ -only refresh, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh and hidden refresh.
- Packages

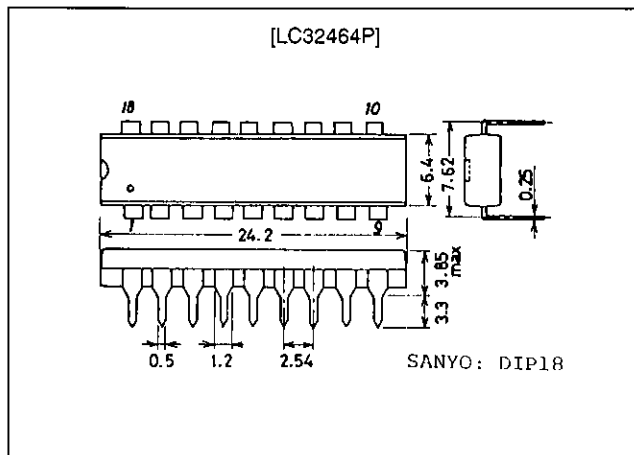
DIP 18-pin plastic package: LC32464P

MFP 24-pin plastic package: LC32464M

Package Dimensions

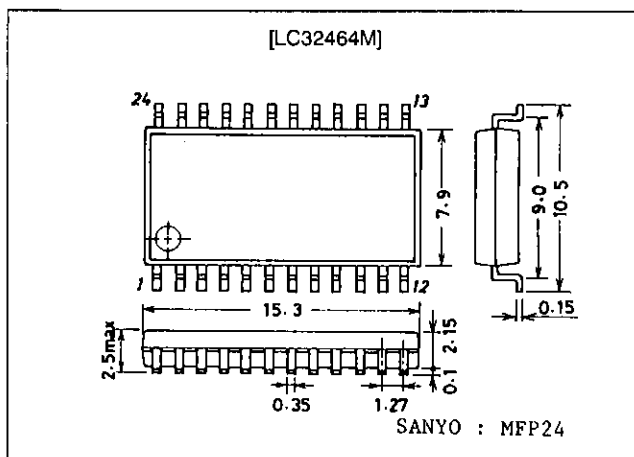
unit : mm

3007A-DIP18

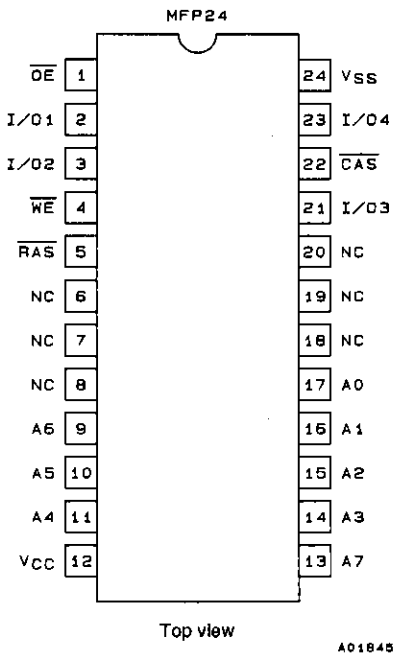
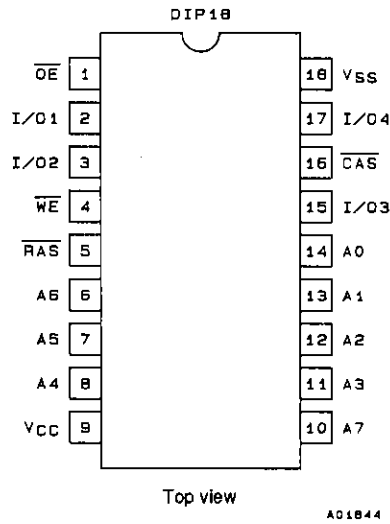


unit : mm

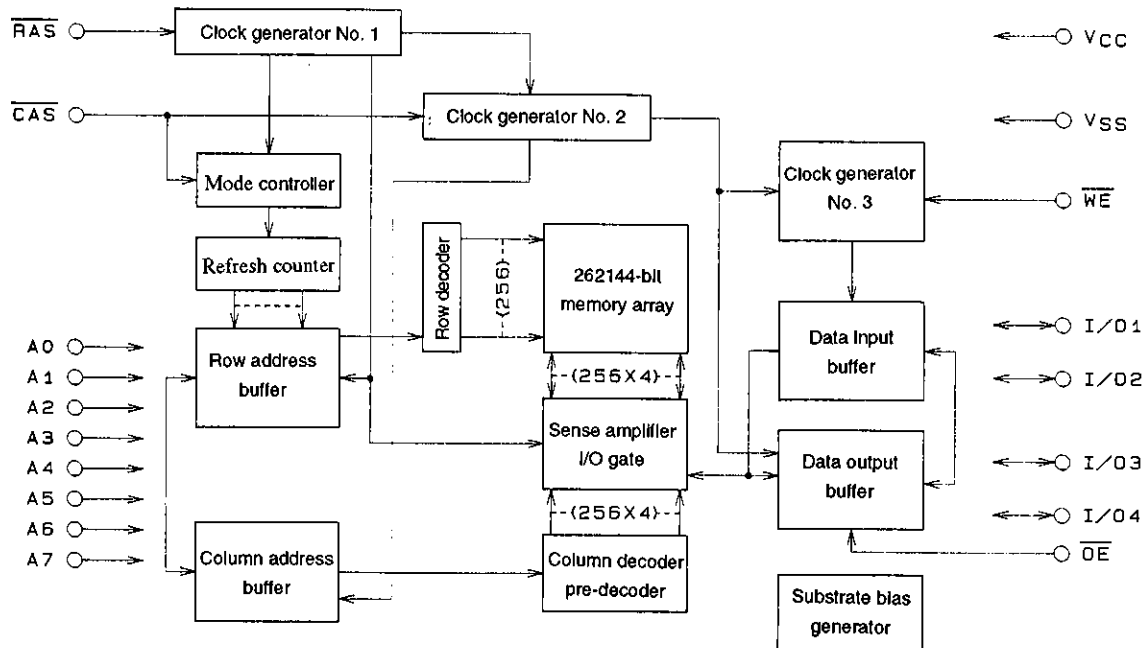
3045B-MFP24



Pin Assignment



Block Diagram



Specifications

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Maximum supply voltage	V_{CC} max	-1.0 to +7.0	V	1
Input voltage	V_{IN}	-1.0 to +7.0	V	1
Output voltage	V_{OUT}	-1.0 to +7.0	V	1
Allowable power dissipation	P_d max	600	mW	1
Output short-circuit current	I_{OUT}	50	mA	1
Operating temperature range	T_{opr}	0 to +70	°C	1
Storage temperature range	T_{stg}	-55 to +150	°C	1

Note: 1) Stresses greater than the above listed maximum values may result in damage to the device.

DC Recommended Operating Ranges at $T_a = 0$ to +70°C

Parameter	Symbol	min	typ	max	Unit	Note
Power supply voltage	V_{CC}	4.5	5.0	5.5	V	2
Input high level voltage	V_{IH}	2.4		6.5	V	2
Input low level voltage	V_{IL}	-1.0		+0.8	V	2

Note: 2) All voltages are referenced to V_{SS} . A bypass capacitor of about 0.1 μ F should be connected between the device V_{CC} and V_{SS} pins.

DC Electrical Characteristics at $T_a = 0$ to +70°C, $V_{CC} = 5\text{ V} \pm 10\%$

Parameter	Symbol	Conditions	min	max	Unit	Note
Operating current (Average current during operation)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$, address cycling: $t_{RC} = t_{RC\ min}$		70	mA	3, 4
Standby current	I_{CC2}	$\overline{RAS} = \overline{CAS} = V_{IH}$		2	mA	
$\overline{RAS}$ -only refresh current	I_{CC3}	$\overline{RAS}$ cycling: $\overline{CAS} = V_{IH}$; $t_{RC} = t_{RC\ min}$		70	mA	3
Fast page mode current	I_{CC4}	$\overline{RAS} = V_{IL}$, $\overline{CAS}$, address cycling: $t_{PC} = t_{PC\ min}$		55	mA	3, 4
Standby current	I_{CC5}	$\overline{RAS} = \overline{CAS} = V_{CC} - 0.2\text{ V}$		1	mA	
$\overline{CAS}$ -before- $\overline{RAS}$ refresh current	I_{CC6}	$\overline{RAS}$, $\overline{CAS}$ cycling: $t_{RC} = t_{RC\ min}$		70	mA	3
Input leakage current	I_{IL}	$0\text{ V} \leq V_{IN} \leq 6.5\text{ V}$, pins other than measuring pin = 0 V	-10	+10	μ A	
Output leakage current	I_{OL}	D_{OUT} disable, $0\text{ V} \leq V_{OUT} \leq 5.5\text{ V}$	-10	+10	μ A	
Output high level voltage	V_{OH}	$I_{OUT} = -5.0\text{ mA}$	2.4		V	
Output low level voltage	V_{OL}	$I_{OUT} = 4.2\text{ mA}$		0.4	V	

Note: 3) All current values are measured at minimal cycle rate. Since current flows immoderately, if cycle time is longer than shown here, current value becomes smaller.

4) I_{CC1} and I_{CC4} are dependent on output loads. Maximum values for I_{CC1} and I_{CC4} represent values with output open.

AC Electrical Characteristics at $T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$ (note 5, 6, 7)

Parameter	Symbol	min	max	Unit	Note
Random read or write cycle time	t_{RC}	160		ns	
Read-write/read-modify-write cycle time	t_{RWC}	215		ns	
Fast page mode cycle time	t_{PC}	55		ns	
Fast page mode read-write/read-modify-write cycle time	t_{PRWC}	100		ns	
$\overline{\text{RAS}}$ access time	t_{RAC}		80	ns	8, 13
$\overline{\text{CAS}}$ access time	t_{CAC}		20	ns	8, 13
Column address access time	t_{AA}		40	ns	8, 14
$\overline{\text{CAS}}$ precharge access time	t_{CPA}		45	ns	8
Output low-impedance time from $\overline{\text{CAS}}$ low	t_{CLZ}	5		ns	8
Output buffer turn-off delay time	t_{OFF}	0	20	ns	9
Rise or fall time	t_T	3	50	ns	7
$\overline{\text{RAS}}$ precharge time	t_{RP}	70		ns	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	80	10000	ns	
$\overline{\text{RAS}}$ pulse width for fast page mode only	t_{RASP}	80	100000	ns	
$\overline{\text{RAS}}$ hold time	t_{RSH}	20		ns	
$\overline{\text{CAS}}$ hold time	t_{CSH}	80		ns	
$\overline{\text{CAS}}$ pulse width	t_{CAS}	20	10000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}	25	60	ns	13
$\overline{\text{RAS}}$ column address delay time	t_{RAD}	17	40	ns	14
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	10		ns	
$\overline{\text{CAS}}$ precharge time for fast page mode only	t_{CP}	10		ns	
Row address setup time	t_{ASR}	0		ns	
Row address hold time	t_{RAH}	12		ns	
Column address setup time	t_{ASC}	0		ns	
Column address hold time	t_{CAH}	20		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	t_{AR}	60		ns	
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	40		ns	
Read command setup time	t_{RCS}	0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	t_{RCH}	0		ns	10
Read command hold time referenced to $\overline{\text{RAS}}$	t_{RRH}	0		ns	10
Write command hold time	t_{WCH}	15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	t_{WCR}	60		ns	
Write command pulse width	t_{WP}	15		ns	

Continued on next page.

Continued from preceding page.

Parameter	Symbol	min	max	Unit	Note
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	25		ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	20		ns	
Data input setup time	t_{DS}	0		ns	11
Data input hold time	t_{DH}	20		ns	11
Data input hold time referenced to $\overline{\text{RAS}}$	t_{DHR}	60		ns	
Refresh period	t_{REF}		4	ms	
Write command setup time	t_{WCS}	0		ns	12
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	t_{CWD}	50		ns	12
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t_{RWD}	105		ns	12
Column address to $\overline{\text{WE}}$ delay time	t_{AWD}	65		ns	12
$\overline{\text{CAS}}$ setup time for $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh	t_{CSR}	10		ns	
$\overline{\text{CAS}}$ hold time for $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh	t_{CHR}	20		ns	
$\overline{\text{RAS}}$ precharge time to $\overline{\text{CAS}}$ active time	t_{RPC}	10		ns	
$\overline{\text{CAS}}$ precharge time for $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ counter test	t_{CPT}	40		ns	
$\overline{\text{CAS}}$ precharge time for $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh	t_{CPN}	15		ns	
$\overline{\text{RAS}}$ hold time referenced to $\overline{\text{OE}}$	t_{ROH}	20		ns	
$\overline{\text{OE}}$ access time	t_{OEA}		20	ns	
$\overline{\text{OE}}$ delay time	t_{OED}	20		ns	
$\overline{\text{OE}}$ output buffer turn-off delay time	t_{OEZ}	0	20	ns	
$\overline{\text{OE}}$ command hold time	t_{OEH}	20		ns	
Data input to $\overline{\text{CAS}}$ delay time	t_{DZC}	0		ns	15
Data input to $\overline{\text{OE}}$ delay time	t_{DZO}	0		ns	15

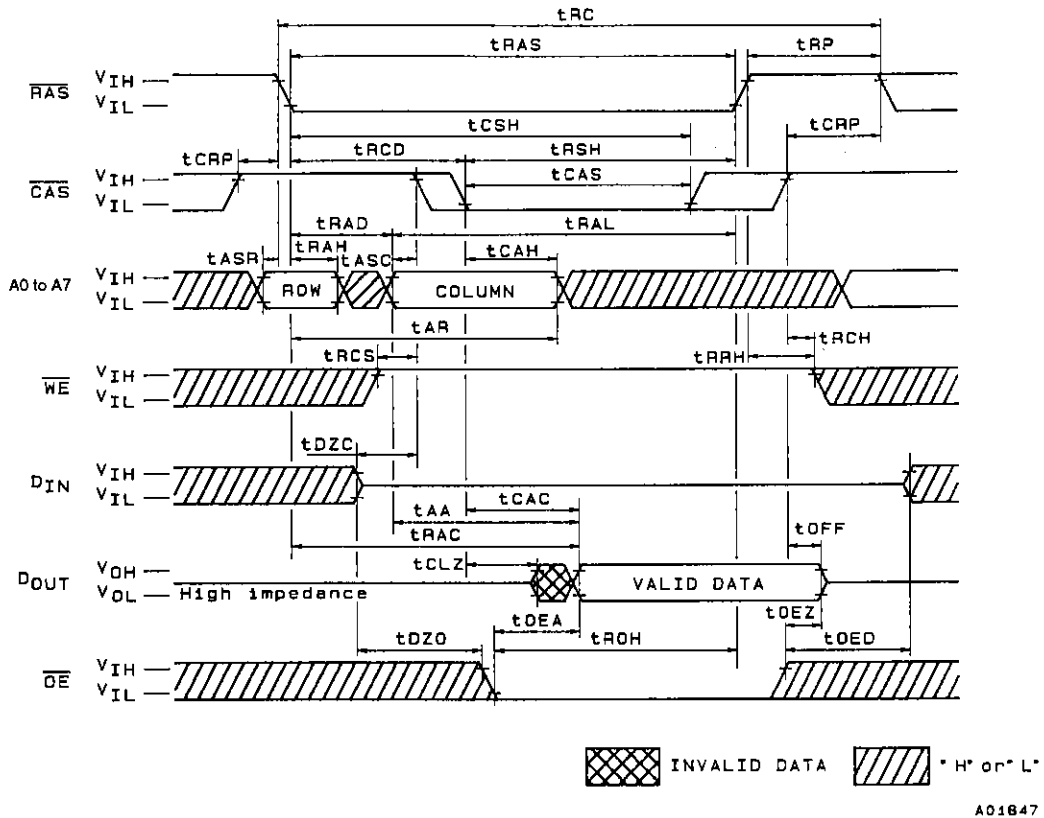
Input/Output Capacitance at $T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{\text{CC}} = 5\text{ V} \pm 10\%$

Parameter	Symbol	min	max	Unit
Input capacitance (A_0 to A_7)	C_{IN1}		5	pF
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C_{IN2}		7	pF
I/O capacitance (I/O_1 to I/O_4)	$C_{\text{I/O}}$		7	pF

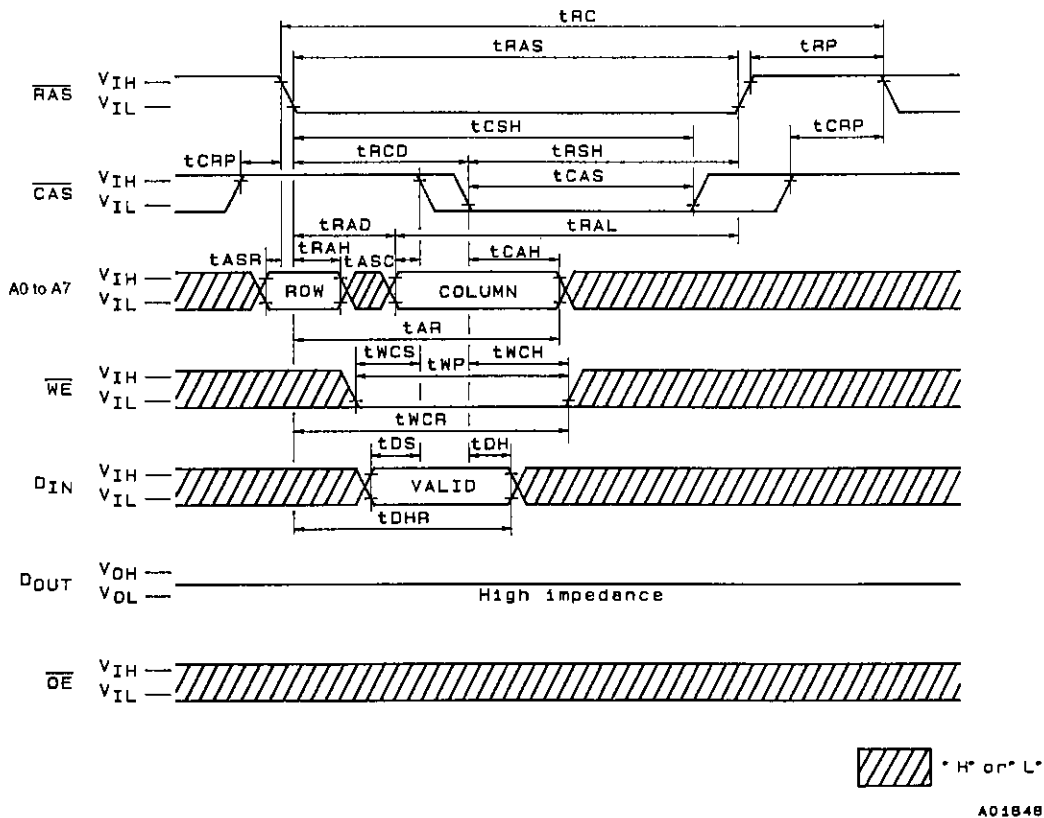
- Notes:
- 5) After the power is turned on, 200 μ s are required after the arrival of V_{CC} stabilized current before memory is initialized and begins operation. In addition, before memory operation initializes, approximately 8 cycles worth of $\overline{RAS}$ dummy cycles are required. When the on-chip refresh counter is applied, approximately 8 cycles worth of $\overline{CAS}$ -before- $\overline{RAS}$ dummy cycles are required instead of the $\overline{RAS}$ dummy cycles.
 - 6) Measured at $t_T = 5$ ns.
 - 7) When measuring input signal timing, V_{IH} (min) and V_{IL} (max) are used for reference points. In addition, rise and fall time are defined between V_{IH} and V_{IL} .
 - 8) Measured using an equivalent of 100 pF and two standard TTL loads.
 - 9) t_{OFF} (max) is defined as the time until output voltage can no longer be measured when output switches to a high impedance condition.
 - 10) Operation is guaranteed if either t_{RRH} or t_{RCH} is satisfied.
 - 11) These parameters are measured from the falling edge of $\overline{CAS}$ for an early-write cycle, and from the falling edge of $\overline{WE}$ for a read-write/read-modify-write cycle.
 - 12) t_{WCS} , t_{CWD} , t_{RWD} and t_{AWD} are not restrictive operating parameters for memory in that they specify the operating mode. If $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle switches to an early-write cycle and output pins switch to high impedance throughout the cycle. If $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{RWD} \geq t_{RWD}(\text{min})$ and $t_{AWD} \geq t_{AWD}(\text{min})$, the cycle switches to a read-write/read-modify-write cycle and data outputs equal information in the selected cells. If neither of the above conditions are satisfied, output pins are in an undefined state.
 - 13) $t_{RCD}(\text{max})$ does not indicate a restrictive operating parameter but instead represents the point at which the access time $t_{RAC}(\text{max})$ is guaranteed. If $t_{RCD} \geq t_{RCD}(\text{max})$, access time is determined according to t_{CAC} .
 - 14) $t_{RAD}(\text{max})$ does not indicate a restrictive operating parameter but instead represents the point at which the access time $t_{RAC}(\text{max})$ is guaranteed. If $t_{RAD} \geq t_{RAD}(\text{max})$, access time is determined according to t_{AA} .
 - 15) Operation is guaranteed if either t_{DZC} or t_{DZO} is satisfied.

Timing Chart

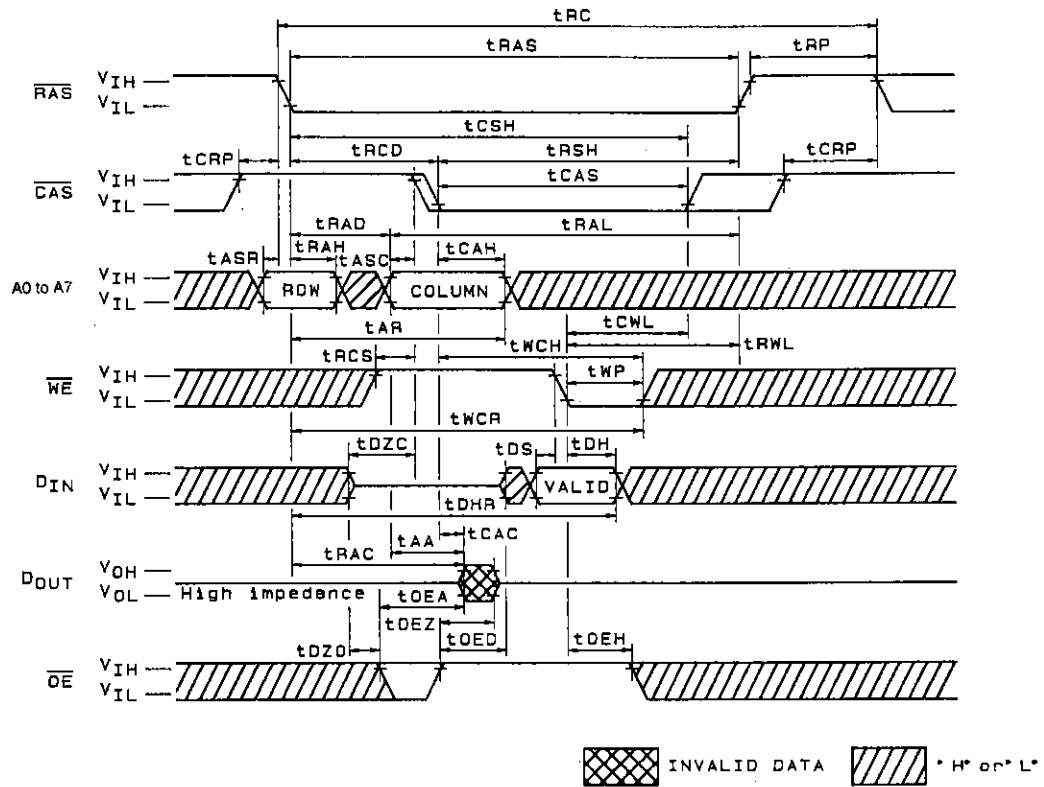
Read Cycle



Write Cycle (Early-write)

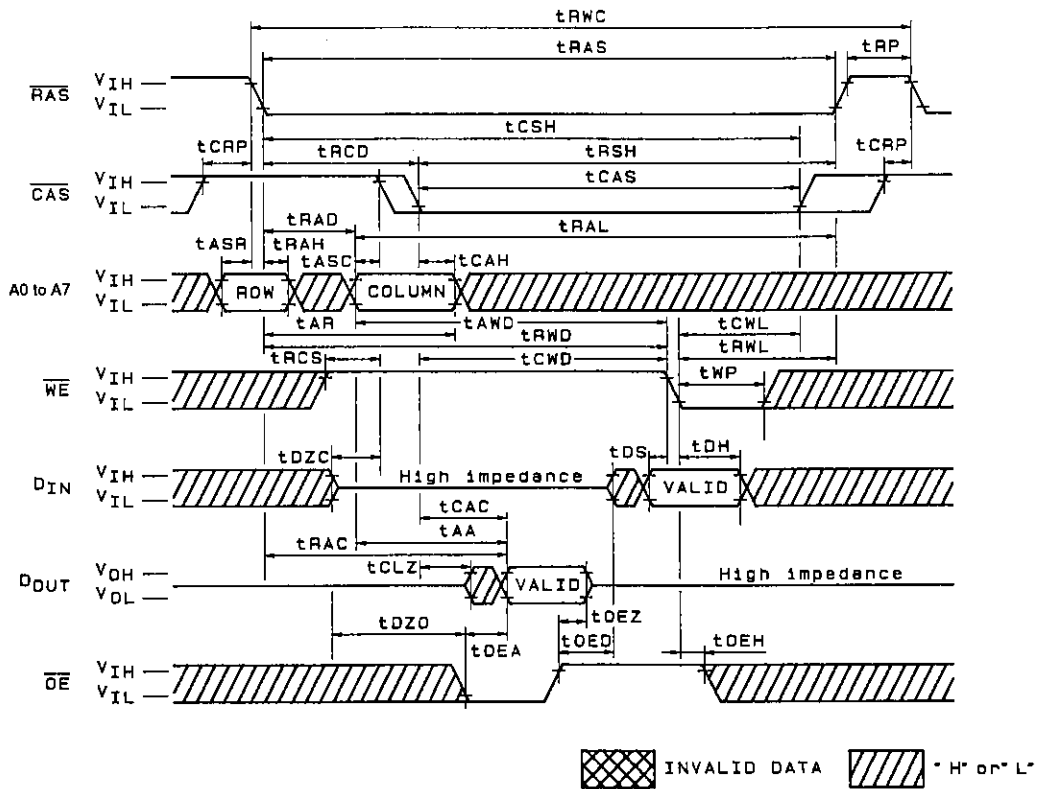


Write Cycle ($\overline{OE}$ Control)



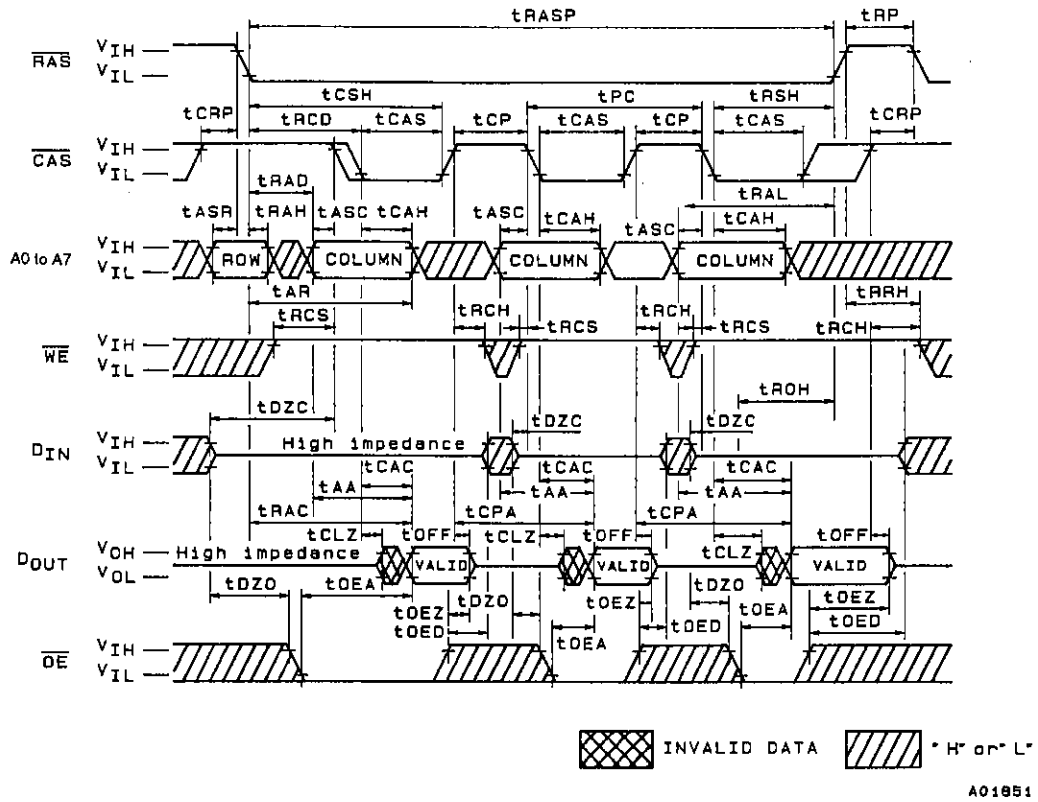
A01849

Read-Write/Read-Modify-Write Cycle

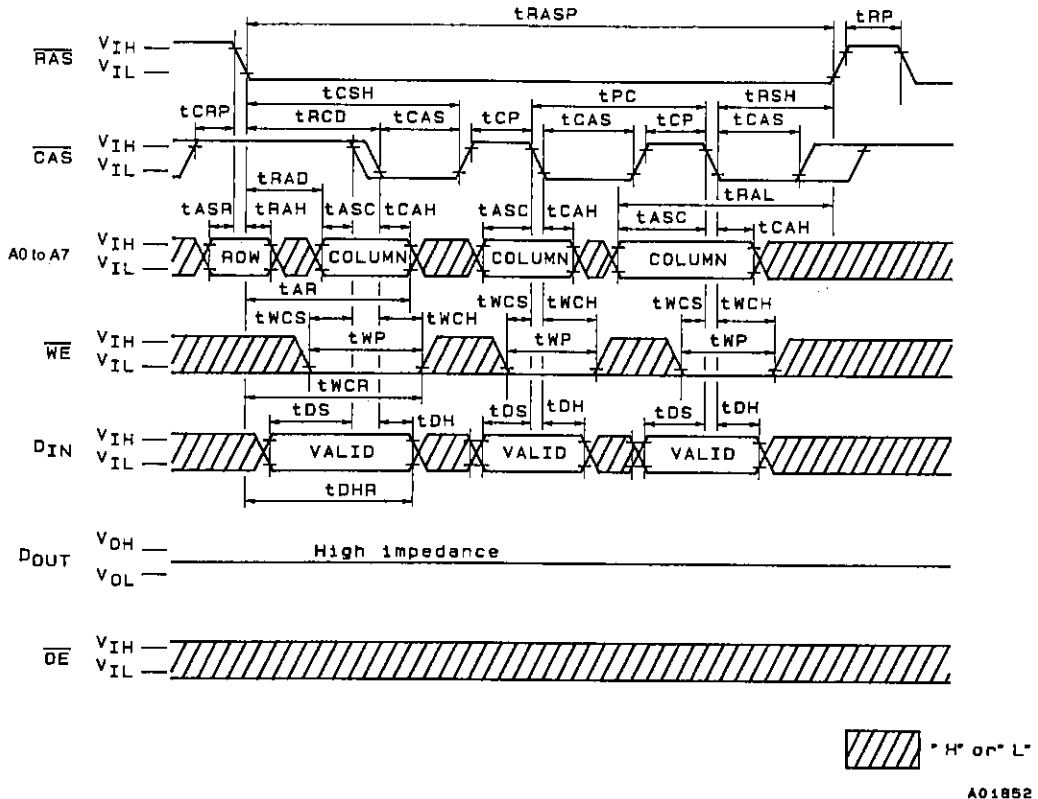


A01850

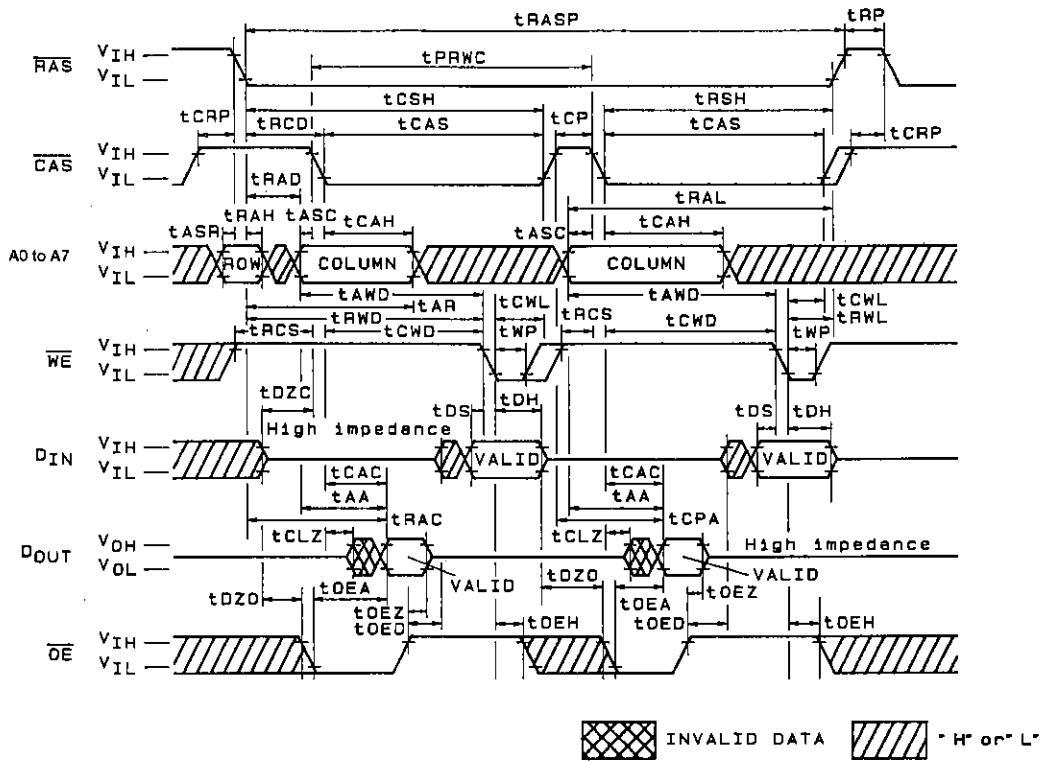
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

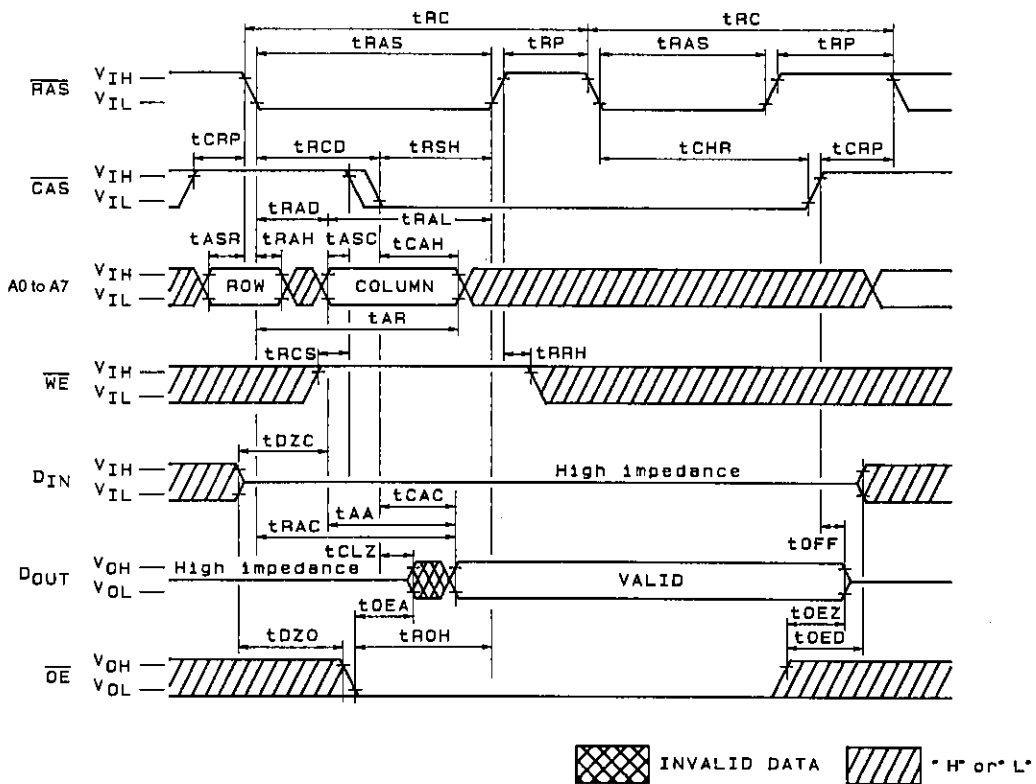


Fast Page Mode Read-Write/Read-Modify-Write Cycle

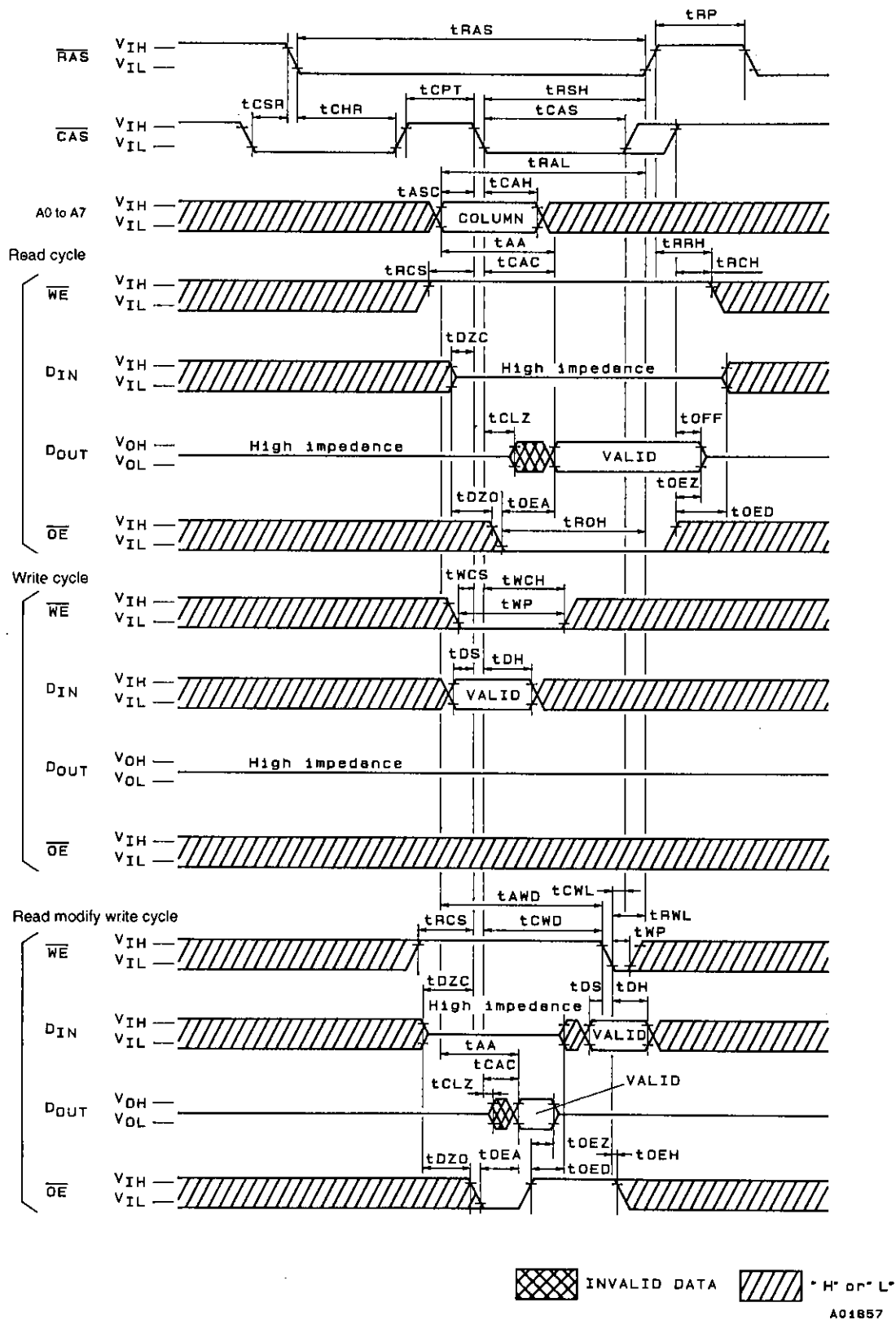


A01853

Hidden Refresh Cycle



A01854

CAS-Before-RAS Refresh Counter Test Cycle

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of April, 1996. Specifications and information herein are subject to change without notice.