

SANYO**LC7940YD,7941YD****Dot-matrix LCD Drivers**

Overview

The LC7940YD and LC7941YD are segment driver ICs for driving large, dot-matrix LCD displays. They read 4-bit parallel or serial input, display data from a controller into an 80-bit latch, and then generate LCD drive signals corresponding to that data.

The LC7940YD and LC7941YD feature mirror-image pin assignments, allowing them to be used together to increase component density. They are designed to be used with the LC7942YD common driver to drive large LCD panels.

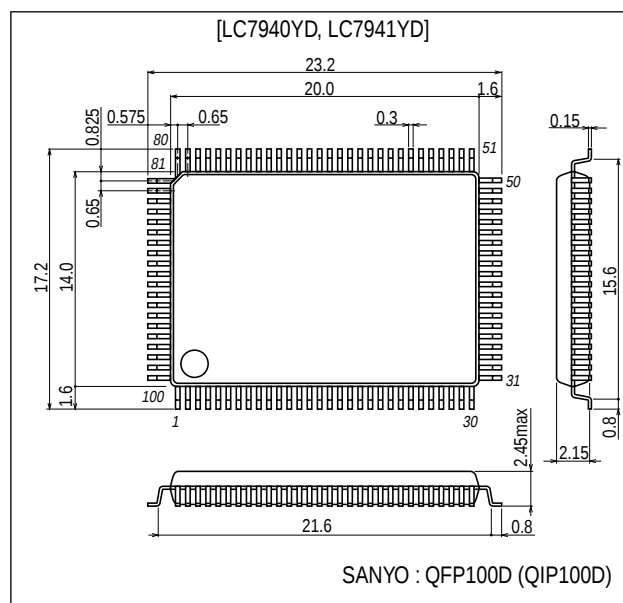
Features

- 80 built-in LCD display drive circuits
- 1/8 to 1/128 display duty cycle
- Serial or 4-bit parallel data input
- Chip disable for low power dissipation for large-sized panels
- Bias supply voltages can be supplied externally
- Operating supply voltage and ambient temperature
 - 2.7 to 5.5 V logic supply (V_{DD}) at $T_a = -20$ to $+85^\circ\text{C}$
 - 8 to 20V LCD supply ($V_{DD} - V_{EE}$) at $T_a = -20$ to $+85^\circ\text{C}$
- CMOS process
- 100-pin flat plastic package

Package Dimensions

unit: mm

3180-QIP100D



Specifications

Absolute Maximum Ratings at $T_a = 25 \pm 2^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Ratings	Unit
Logic supply voltage	V_{DD} max	-0.3 to +7.0	V
LCD supply voltage, See Note below.	$V_{DD} - V_{EE}$ max	0 to 22	V
Input voltage	V_I max	-0.3 to $V_{DD} + 0.3$	V

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Parameter	Symbol	Ratings	Unit
Operating temperature range	T_{opr}	-20 to +85	°C
Storage temperature range	T_{stg}	-40 to +125	°C

Note

$V_{DD} \geq V_1 > V_3 > V_4 > V_{EE}$

Recommended Operating Conditions at $T_a = -20$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Logic supply voltage	V_{DD}		2.7	–	5.5	V
LCD supply voltage	$V_{DD} - V_{EE}$	See Notes 1 and 2.	8	–	20	V
HIGH-level input voltage	V_{IH}	CP, CDI, DI1 to DI3, M, SDI, P/S, DISPOFF and LOAD	$0.8V_{DD}$	–	–	V
LOW-level input voltage	V_{IL}	CP, CDI, DI1 to DI3, M, SDI, P/S, DISPOFF and LOAD	–	–	$0.2V_{DD}$	V
CP shift clock frequency	f_{CP}			–	3.3	MHz
CP pulsewidth	t_{WC}		100	–	–	ns
LOAD pulsewidth	t_{WL}		100	–	–	ns
DIin and SDI to CP setup time	t_{SETUP}		80	–	–	ns
DIin and SDI to CP hold time	t_{HOLD}		80	–	–	ns
CP to LOAD time	t_{CL1}		0	–	–	ns
	t_{CL2}		100	–	–	ns
LOAD to CP time	t_{LC}		100	–	–	ns
CP rise time	t_R		–	–	50	ns
CP fall time	t_F		–	–	50	ns
LOAD rise time	t_{RL}		–	–	50	ns
LOAD fall time	t_{FL}		–	–	50	ns

Notes

- $V_{DD} \geq V_1 > V_3 > V_4 > V_{EE}$
- At turn ON, the LCD supply should be energized after or simultaneously with the logic supply. At turn OFF, the logic supply should be cut after or simultaneously with the LCD supply.

Electrical Characteristics at $T_a = 25 \pm 2^\circ\text{C}$, $V_{SS} = 0\text{V}$, $V_{DD} = 2.7$ to 5.5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
HIGH-level input current	I_{IH}	$V_{IN} = V_{DD}$; LOAD, CP, CDI, P/S, DI1 to DI3, SDI, M, and DISPOFF	–	–	1	μA
LOW-level input current	I_{IL}	$V_{IN} = V_{SS}$; LOAD, CP, CDI, P/S, DI1 to DI3, SDI, M, and DISPOFF	–	–	–1	μA
CDO HIGH-level output voltage	V_{OH}	$I_{OH} = -400\text{ }\mu\text{A}$	$V_{DD} - 0.4$	–	–	V
CDO LOW-level output voltage	V_{OL}	$I_{OL} = 400\text{ }\mu\text{A}$	–	–	0.4	V
O1 to O80 driver ON resistance	R_{ON}	$V_{DD} - V_{EE} = 18\text{ V}$, $ V_{DE} - V_O = 0.25\text{ V}$. See note	–	2	4	$\text{k}\Omega$

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
V_{DD} to V_{SS} standby supply current	I_{ST}	$CDI = V_{DD}$, $V_{DD} - V_{EE} = 18\text{ V}$, $f_{CP} = 3.3\text{ MHz}$, no output load ; V_{SS}	–	–	200	μA
V_{DD} to V_{SS} operating supply current	I_{SS}	$V_{DD} - V_{EE} = 18\text{ V}$, $f_{CP} = 3.3\text{ MHz}$, $I_{LOAD} = 5.156\text{ kHz}$, $f_M = 52\text{ Hz}$; V_{SS}	–	–	1.0	mA
V_{DD} to V_{EE} operating supply current	I_{EE}	$V_{DD} - V_{EE} = 18\text{ V}$, $f_{CP} = 3.3\text{ MHz}$, $f_{LOAD} = 5.156\text{ kHz}$, $f_M = 52\text{ Hz}$; V_{EE}	–	–	0.1	mA
CP input capacitance	C_I	$f_{CP} = 3.3\text{ MHz}$; CP	–	5	–	pF

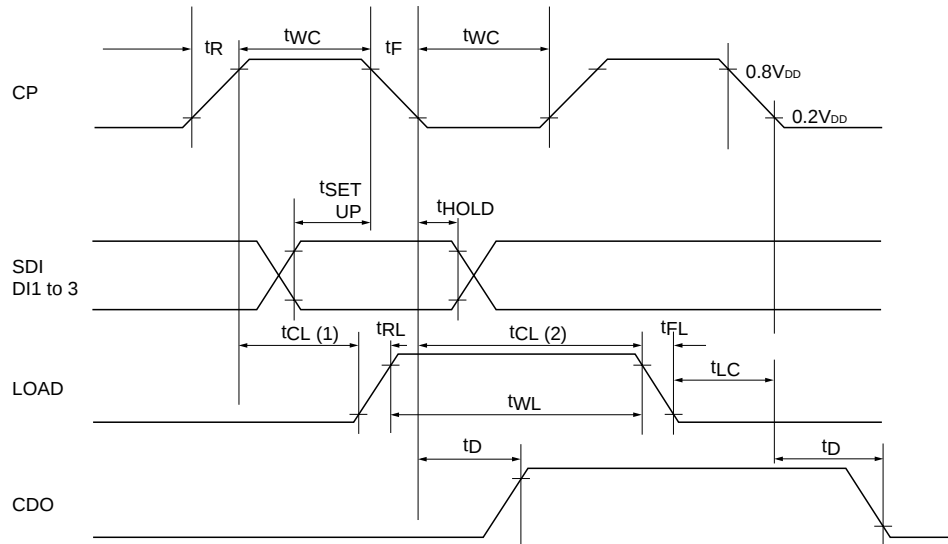
Note

$V_{DD} = V_1$ or V_3 , or V_4 or V_{EE} , $V_1 = V_{DD}$, $V_3 = 9/11 \times (V_{DD} - V_{EE})$, $V_4 = 2/11 \times (V_{DD} - V_{EE})$

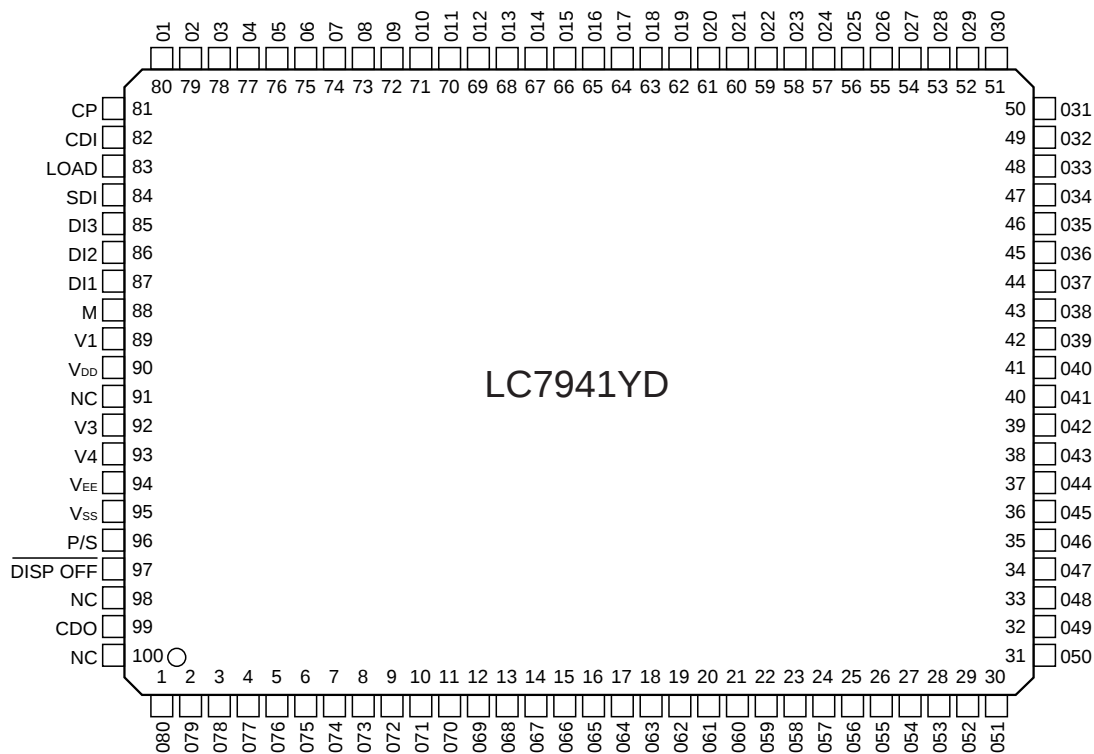
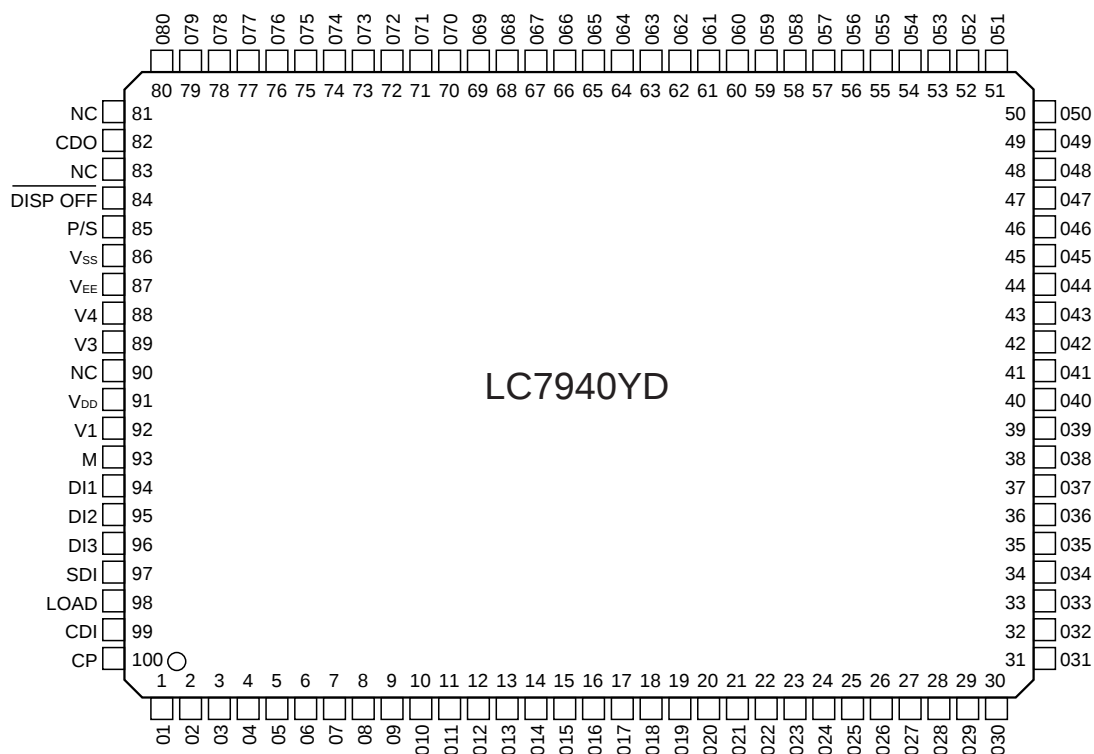
Switching Characteristics at $T_a = 25 \pm 2^\circ\text{C}$, $V_{SS} = 0\text{ V}$, $V_{DD} = 2.7$ to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
CDO output delay time	t_D	$C_L = 30\text{ pF}$	–	–	200	ns

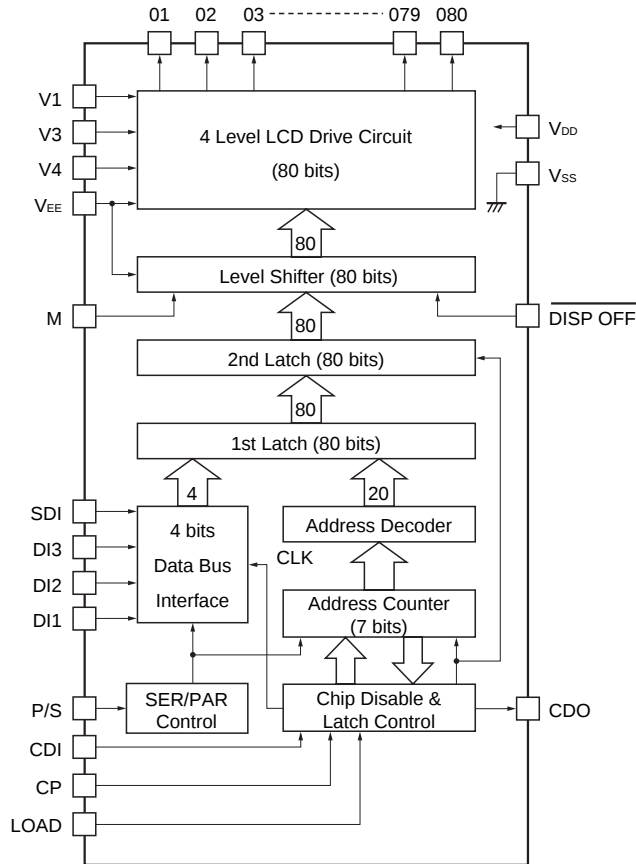
Switching Characteristics Waveform



Pad Layout (Top view)



Block Diagram



Pin Functions

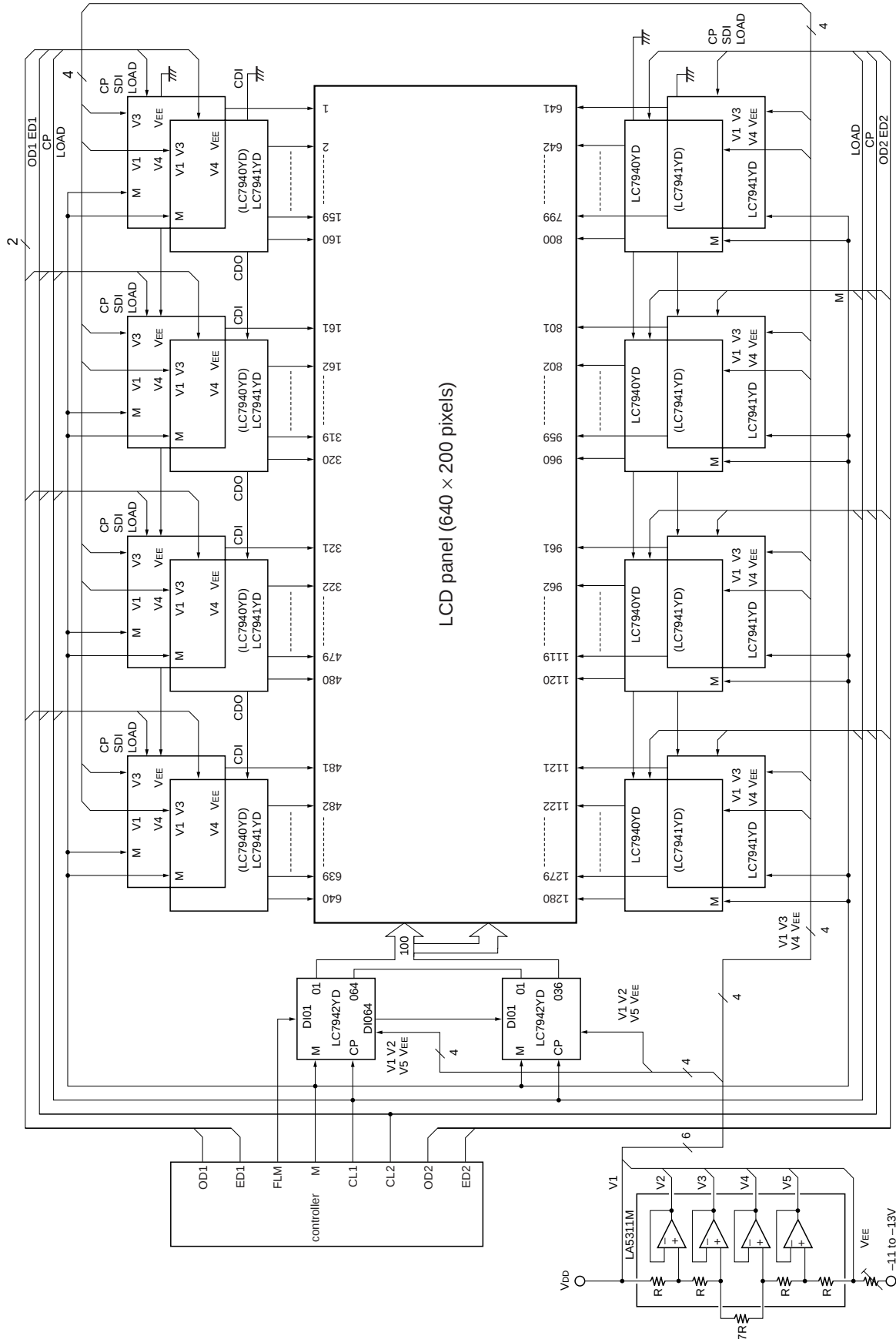
Pin No.		Symbol	I/O	Functions
LC7940YD	LC7941YD			
91	90	V_{DD}	Supply	$V_{DD} - V_{SS}$ is the logic supply. $V_{DD} - V_{EE}$ is the LCD supply.
86	95	V_{SS}		
87	94	V_{EE}		
92	89	V_1	Supply	LCD panel drive voltage supplies V_1 and V_{EE} are selected levels. V_3 and V_4 are not-selected levels.
89	92	V_3		
88	93	V_4		
100	81	CP	I	Display data Input clock (falling-edge trigger).
99	82	CDI	I	Chip disable. Data is read in when LOW, and not read in when HIGH.
98	83	LOAD	I	Display data latch clock (falling-edge trigger). On the falling edge, the LCD drive signals set by the display data are output.
97	84	SDI	I	Serial data input.

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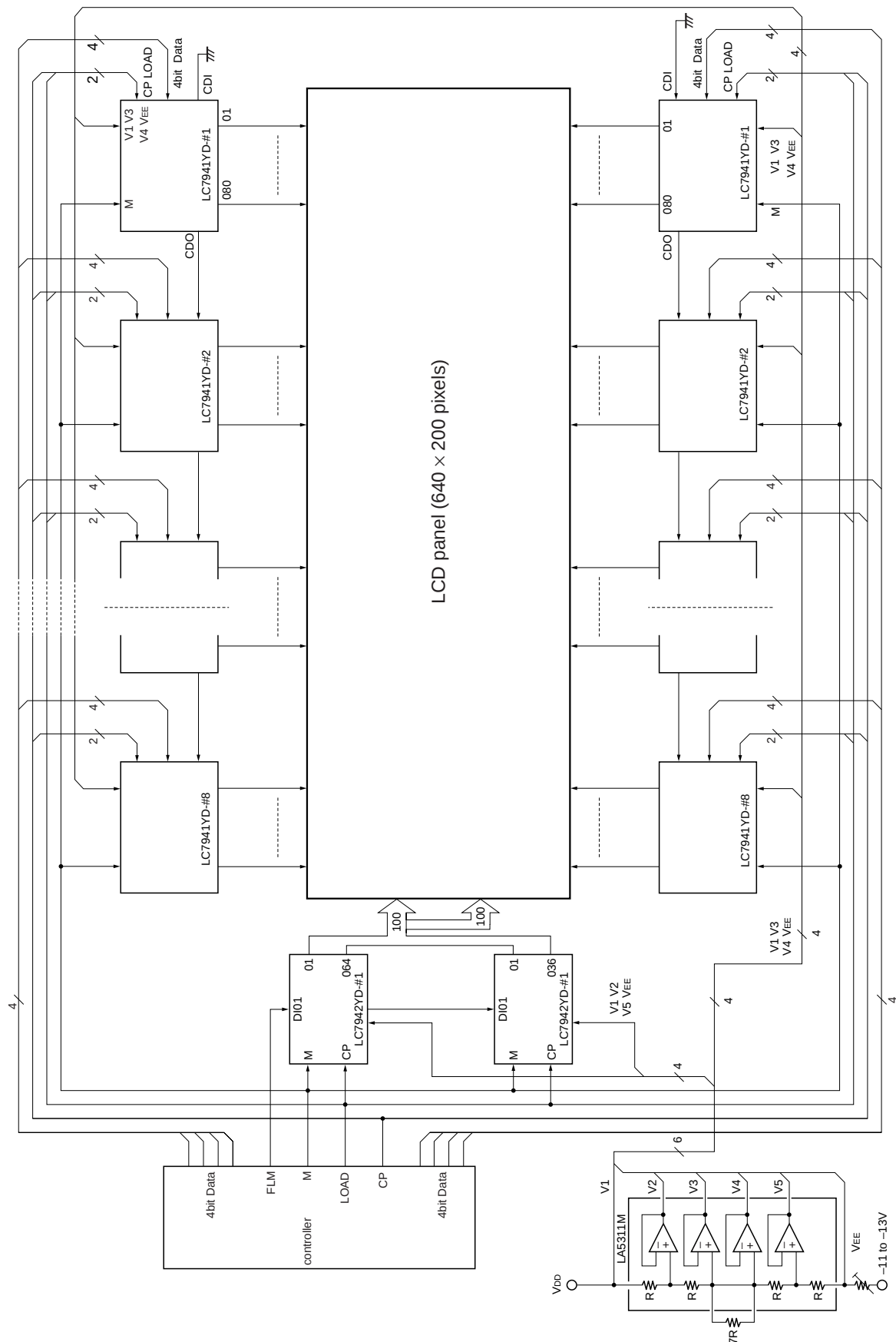
Pin No.		Synbol	I/O	Functions																								
LC7940YD	LC7941YD																											
96	85	DI3	I	4–bit parallel data input pins.																								
95	86	DI2		<table><tr><th>Data input</th><th colspan="4">LCD driver outputs</th></tr><tr><td>SDI</td><td>O4</td><td>O8</td><td rowspan="4">→</td><td>O80</td></tr><tr><td>DI3</td><td>O3</td><td>O7</td><td>O79</td></tr><tr><td>DI2</td><td>O2</td><td>O6</td><td>O78</td></tr><tr><td>DI1</td><td>O1</td><td>O5</td><td>O77</td></tr></table>	Data input	LCD driver outputs				SDI	O4	O8	→	O80	DI3	O3	O7	O79	DI2	O2	O6	O78	DI1	O1	O5	O77		
Data input	LCD driver outputs																											
SDI	O4	O8		→	O80																							
DI3	O3	O7			O79																							
DI2	O2	O6			O78																							
DI1	O1	O5	O77																									
94	87	D11	In serial data input mode, DI1 to DI3 should all be tied HIGH or LOW.																									
93	88	M	I	LCD panel drive voltage output alternation control signal.																								
85	96	P/S	I	Data input mode select. 4–bit parallel input when HIGH, and serial input when LOW																								
82	99	CDO	O	Cascade connection pin for extension segment drivers. Data is read out when HIGH. Goes LOW after data is read out. Connected to the CDI input of the next chip.																								
1 to 80	80 to 1	OI to O80	O	LCD drive outputs. The output drive level is determined by the display data, M signal and DISP OFF input as shown below.																								
				<table><tr><th>M</th><th>Q</th><th>DISP OFF</th><th>Output</th></tr><tr><td>LOW</td><td>LOW</td><td>HIGH</td><td>V₃</td></tr><tr><td>LOW</td><td>HIGH</td><td>HIGH</td><td>V₁</td></tr><tr><td>HIGH</td><td>LOW</td><td>HIGH</td><td>V₄</td></tr><tr><td>HIGH</td><td>HIGH</td><td>HIGH</td><td>V_{EE}</td></tr><tr><td>×</td><td>×</td><td>LOW</td><td>V₁</td></tr></table>	M	Q	DISP OFF	Output	LOW	LOW	HIGH	V ₃	LOW	HIGH	HIGH	V ₁	HIGH	LOW	HIGH	V ₄	HIGH	HIGH	HIGH	V _{EE}	×	×	LOW	V ₁
				M	Q	DISP OFF	Output																					
				LOW	LOW	HIGH	V ₃																					
				LOW	HIGH	HIGH	V ₁																					
				HIGH	LOW	HIGH	V ₄																					
HIGH	HIGH	HIGH	V _{EE}																									
×	×	LOW	V ₁																									
Note x = don't care (tied HIGH or LOW)																												
84	97	DISPOFF	I	O1 to O80 output control input pin. When LOW, V1 is output on the O1 to O80 outputs, See the truth table.																								
81	91	NC	–	No connection.																								
83	98	NC																										
90	100	NC																										

Application Notes

LCD Panel 1



LCD Panel 2

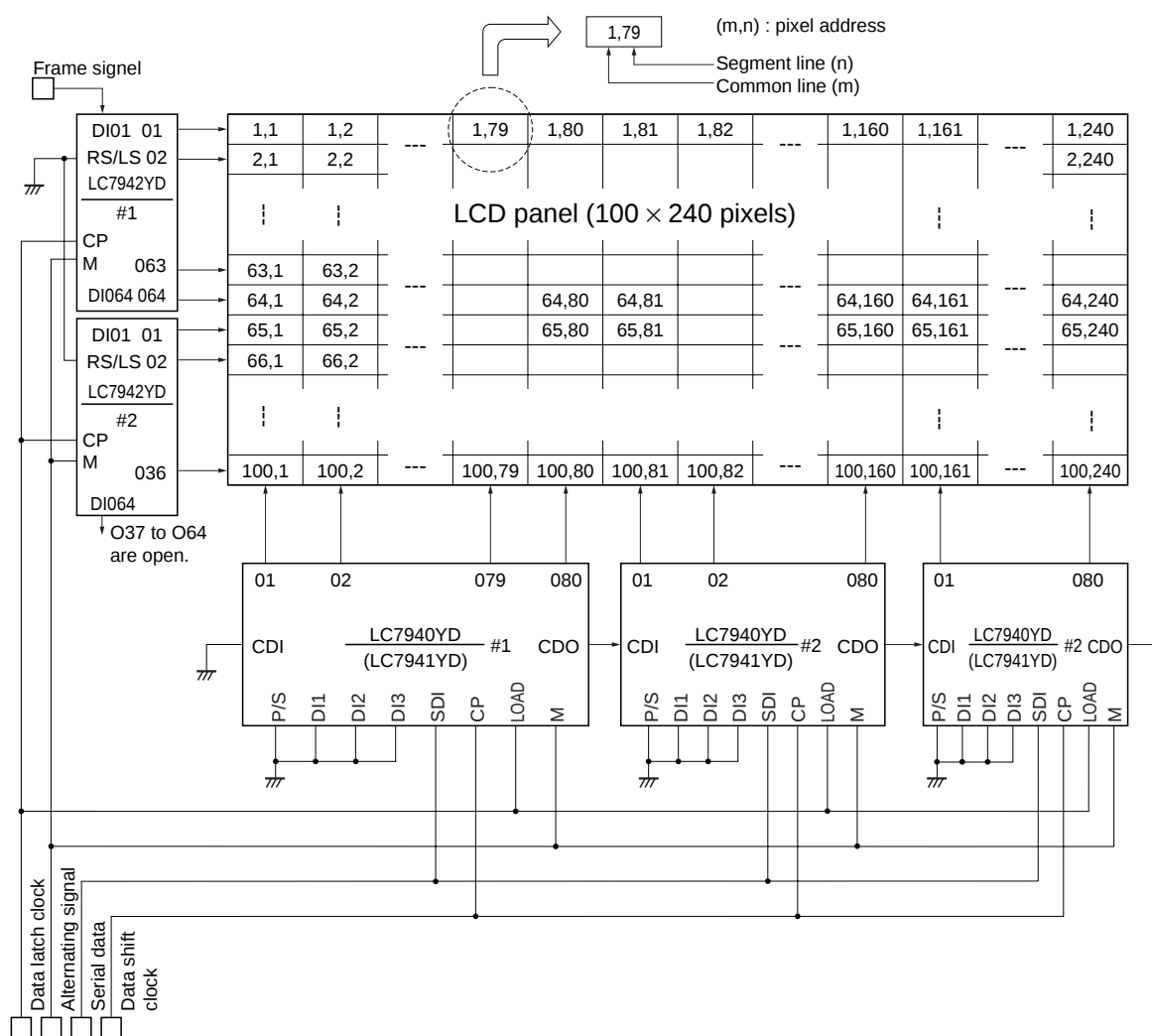


100 × 240-pixel LCD Panel Application

A 100 × 240-pixel LCD panel requires the following drivers.

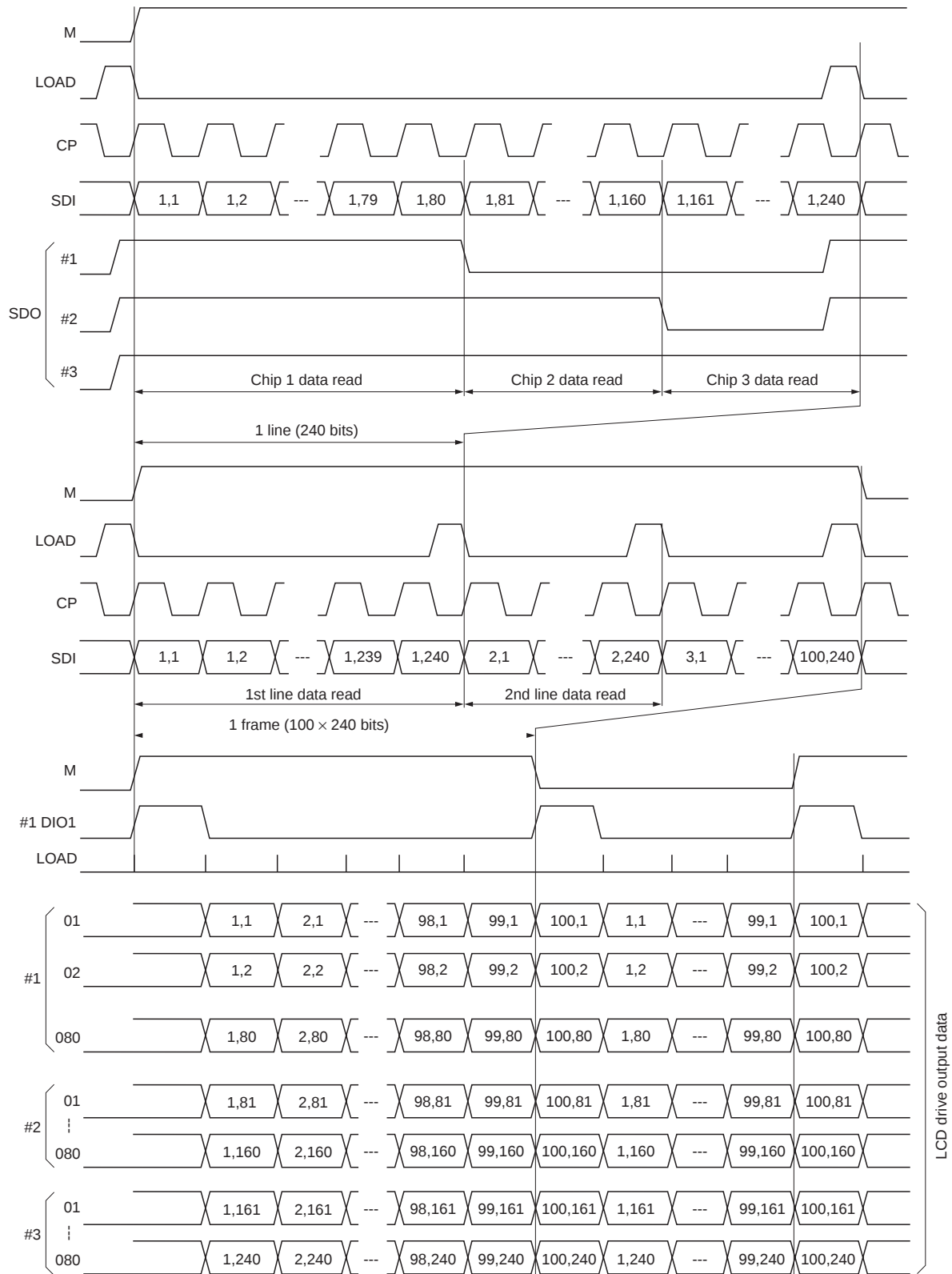
- 3 × LC7940YD (or LC7941YD) drivers
- 2 × LC7942YD drivers

An example using 1/100 duty cycle is shown below.



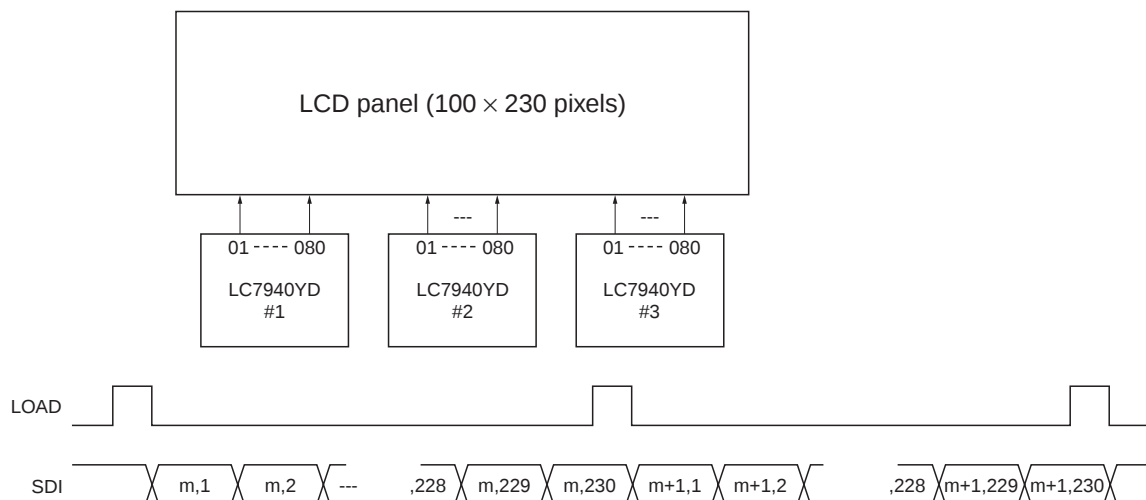
1. The LC7942YD chips are cascaded by connecting DIO64 on chip 1 to DIO1 on chip 2. For a 100-bit shift register, 037 to 064 on chip 2 are left open.
2. The LC7940YD (or LC7941YD) chips are cascaded by connecting CDO on chip 1 to CDI on chip 2, and CDO on chip 2 to CDI on chip 3. CDI on chip 1 is tied to GND, and CDO on chip 3 is not used. This configuration allows the input of 240-bit serial data.

100 x 240-pixel LCD Panel Timing Diagram



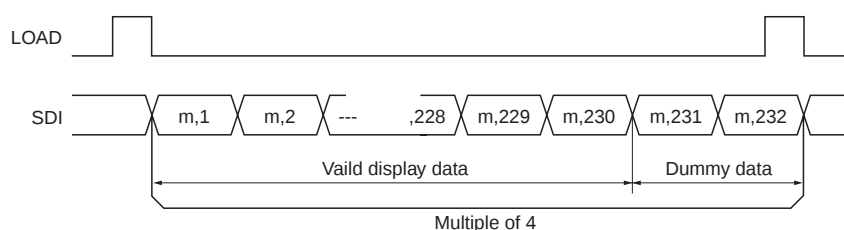
Segment Data Not Multiples of 4

Example.



If this timing data is sent, data elements (m, 229), (m, 230), (m+1, 229), (m+1, 230)... will not appear in the output (O69 and O70 on chip 3). This is because the LC7940YD (or LC7941YD) converts serial/parallel data

in 4-bit units, which also decreases power dissipation. For data that is not a multiple of 4, like 230, the following scheme is used.



In this case, (m, 231) is output on O71 on chip 3, and (m, 232) on O72 on chip 3. However, these outputs are not connected to the panel and are, therefore, invalid.

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