Ordering number: EN 6159

CMOS IC

LC7942YC

Dot-matrix LCD Driver

Overview

The LC7942YC is a common driver IC for driving large, dot–matrix LCD displays. It features a built–in 64–bit bidirectional shift register and a 4–level LCD driver. It can also be connected in cascade to increase the number of bits.

The LC7942YC is designed to be used with LC7940YC or LC7941YC segment drivers to drive large LCD panels.

Features

- 64 built–in LCD display drive circuits
- l/64 to 1/128 display duty cycle
- Input/outputs for cascade connection
- Bias supply voltages can be supplied externally
- Operating supply voltage and ambient temperature
  - 2.7 to 5.5V logic supply (V_{DD}) at Ta = –20 to +85 °C
  - 8 to 20 V LCD supply (V_{DD} – V_{EE}) at Ta = –20 to +85 °C
- CMOS process

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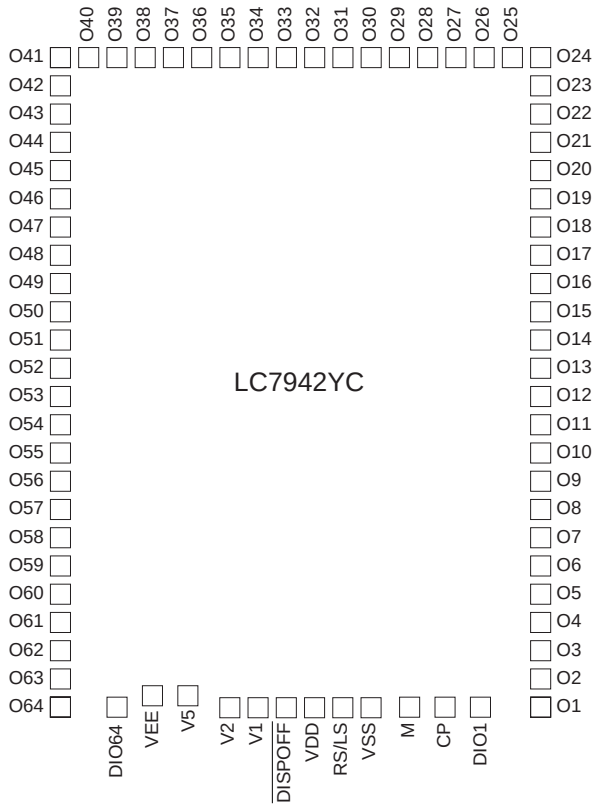
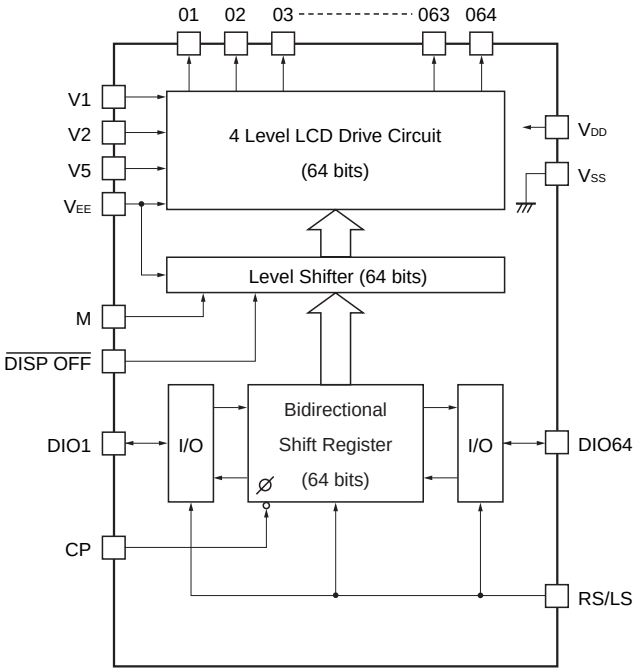
Pad Layout (Top view)



Block Diagram



LC7942YC Pad Location							
chip size : 3.200 mm x 3.970 mm							
Pin_No.	**Name**	**X**	**Y**	**Pin_No.**	**Name**	**X**	**Y**
41	O1	-1425.9	1808	11	O51	1425.9	-213
42	O2	-1425.9	1635	12	O52	1425.9	-70
43	O3	-1425.9	1465	13	O53	1425.9	70
44	O4	-1425.9	1298	14	O54	1425.9	213
45	O5	-1425.9	1134	15	O55	1425.9	359
46	O6	-1425.9	973	16	O56	1425.9	508
47	O7	-1425.9	815	17	O57	1425.9	660
48	O8	-1425.9	660	18	O58	1425.9	815
49	O9	-1425.9	508	19	O59	1425.9	973
50	O10	-1425.9	359	20	O60	1425.9	1134
51	O11	-1425.9	213	21	O61	1425.9	1298
52	O12	-1425.9	70	22	O62	1425.9	1465
53	O13	-1425.9	-70	23	O63	1425.9	1635
54	O14	-1425.9	-213	24	O64	1425.9	1808
55	O15	-1425.9	-359	25	DIO64	1096	1768
56	O16	-1425.9	-508	26	---	---	---
57	O17	-1425.9	-660	27	V_{EE}	880	1728
58	O18	-1425.9	-815	28	V_5	689	1728
59	O19	-1425.9	-973	29	V_2	498	1768
60	O20	-1425.9	-1134	30	V_1	318	1768
61	O21	-1425.9	-1298	31	$\overline{\text{DISPOFF}}$	143	1768
62	O22	-1425.9	-1465	32	V_{DD}	-37	1753
63	O23	-1425.9	-1635	33	RS/LS	-213	1753
64	O24	-1425.9	-1808	34	V_{SS}	-393	1753
65	O25	-1236	-1808	35	---	---	---
66	O26	-1053	-1808	36	M	-598	1768
67	O27	-875	-1808	37	---	---	---
68	O28	-704	-1808	38	CP	-835	1768
69	O29	-538	-1808	39	---	---	---
70	O30	-378	-1808	40	DIO1	-1056	1768
71	O31	-223	-1808				
72	O32	-73	-1808				
73	O33	73	-1808				
74	O34	223	-1808				
75	O35	378	-1808				
76	O36	538	-1808				
77	O37	704	-1808				
78	O38	875	-1808				
79	O39	1053	-1808				
80	O40	1236	-1808				
1	O41	1425.9	-1808				
2	O42	1425.9	-1635				
3	O43	1425.9	-1465				
4	O44	1425.9	-1298				
5	O45	1425.9	-1134				
6	O46	1425.9	-973				
7	O47	1425.9	-815				
8	O48	1425.9	-660				
9	O49	1425.9	-508				
10	O50	1425.9	-359				

Pin Functions

<table>
<tr><th>Number</th><th>Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>32</td><td>V_{DD}</td><td rowspan="3">Supply</td><td rowspan="3">$V_{DD} - V_{ss}$ is the logic supply.
$V_{DD} - V_{EE}$ is the LCD supply.</td></tr>
<tr><td>34</td><td>V_{SS}</td></tr>
<tr><td>27</td><td>V_{EE}</td></tr>
<tr><td>30</td><td>V_1</td><td rowspan="3">Supply</td><td rowspan="3">LCD panel drive voltage supplies.
V_1 and V_{EE} are selected levels.
V_2 and V_5 are not–selected levels.</td></tr>
<tr><td>29</td><td>V_2</td></tr>
<tr><td>28</td><td>V_5</td></tr>
<tr><td>38</td><td>CP</td><td>I</td><td>Display data input clock (falling–edge trigger).</td></tr>
<tr><td>40</td><td>DIO1</td><td>I/O</td><td rowspan="3">
<table>
<tr><th>RS/LS</th><th>DIO1</th><th>DIO64</th><th>Shift direction</th></tr>
<tr><td>LOW (rlght shift)</td><td>Input</td><td>Output</td><td>O1 → O64</td></tr>
<tr><td>HIGH (left shift)</td><td>Output</td><td>Input</td><td>O64 → O1</td></tr>
</table>
</td></tr>
<tr><td>25</td><td>DIO64</td><td>I/O</td></tr>
<tr><td>33</td><td>RS/LS</td><td>I</td></tr>
<tr><td>36</td><td>M</td><td>I</td><td>LCD panel drive voltage output alternation control signal.</td></tr>
<tr><td>31</td><td>$\overline{\text{DISP OFF}}$</td><td>I</td><td>O1 to O64 output control input pins.</td></tr>
<tr><td>41 to 80</td><td>O1 to O40</td><td rowspan="2">O</td><td rowspan="2">LCD drive outputs
The output drive level is determined by the display data, M signal and $\overline{\text{DISPOFF}}$ input as show below.
<table>
<tr><th>M</th><th>Q</th><th>$\overline{\text{DISPOFF}}$</th><th>Output</th></tr>
<tr><td>LOW</td><td>LOW</td><td>HIGH</td><td>V_2</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>HIGH</td><td>V_{EE}</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>HIGH</td><td>V_5</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>HIGH</td><td>V_1</td></tr>
<tr><td>×</td><td>×</td><td>LOW</td><td>V_1</td></tr>
</table>
Note
× = don't care (tied HIGH or LOW)</td></tr>
<tr><td>1 to 24</td><td>O41 to O64</td></tr>
<tr><td>26</td><td>NC</td><td rowspan="4">–</td><td rowspan="4">No connection.</td></tr>
<tr><td>35</td><td>NC</td></tr>
<tr><td>37</td><td>NC</td></tr>
<tr><td>39</td><td>NC</td></tr>
</table>

Specifications

The following electrical characteristics apply when sealed in a Sanyo standard QIC-80 package.

Absolute Maximum Ratings at Ta = 25 ±2°C, V_{SS} = 0 V

Parameter	Symbol	Ratings	Unit
Logic supply voltage	V_{DD} max	–0.3 to +7.0	V
LCD supply voltage. See note.	$V_{DD} - V_{EE}$ max	0 to 22	V
Input voltage	V_I max	–0.3 to V_{DD} + 0.3	V
Operating temperature range	T_{opr}	–20 to +85	°C
Storage temperature range	T_{stg}	–40 to +125	°C

Note

$V_{DD} \geq V_1 > V_2 > V_5 > V_{EE}$

Allowable Operating Ranges at Ta = –20 to +85 °C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Logic supply voltage	V_{DD}		2.7	—	5.5	V
LCD supply voltage	$V_{DD} - V_{EE}$	See notes 1 and 2.	8	—	20	V
DIO1, DIO64, CP, M, RS/LS and $\overline{\text{DISPOFF}}$ HIGH–level input voltage	V_{IH}		$0.8V_{DD}$	—	—	V
DIO1, DIO64, CP, M, RS/LS and $\overline{\text{DISPOFF}}$ LOW–level input voltage	V_{IL}		—	—	$0.2V_{DD}$	V
CP shift clock frequency	f_{CP}		—	—	1	MHz
CP pulsewidth	t_{WC}		125	—	—	ns
DIO1 and DIO64 to CP setup time	t_{SETUP}		l00	—	—	ns
DIOl and DIOS4 to CP hold time	t_{HOLD}		l00	—	—	ns
CP rise time	t_R		—	—	50	ns
CP fall time	t_F		—	—	50	ns

Notes

1. $V_{DD} \geq V_1 > V_2 > V_5 > V_{EE}$
2. At turn ON, the LCD supply should be energized after or simultaneously with the logic supply. At turn OFF, the logic supply should be cut after or simultaneously with the LCD supply.

Electrical Characteristics at Ta = 25 ± 2 C, V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
DIO1, DIO64, CP, M, RS/LS and $\overline{\text{DISPOFF}}$ HIGH–level input current	I_{IH}	$V_{IN} = V_{DD}$	—	—	1	µA
DIO1, DIO64, CP, M, RS/LS and $\overline{\text{DISPOFF}}$ LOW–level input current	I_{IL}	$V_{IN} = V_{SS}$	–1	—	—	µA
DIO1 and DIO64 HIGH–level output voltage	V_{OH}	I_{OH} = –400 µA	V_{DD} – 0.4	—	—	V
DIO1 and DIO64 LOW–level output voltage	V_{OL}	I_{OL} = 400 µA	—	—	0.4	V
O1 to O64 driver ON resistance	R_{ON}	$V_{DD} - V_{EE}$ = 18 V, $V_{DD} - V_{OL}$ = 0.25 V, V_{DD} = 4.5 V	—	—	1.5	kΩ
V_{DD} static supply current	I_{DD}	$V_{DD} - V_{EE}$ = 18 V, CP = V_{DD}	—	—	100	µA
CP input capacitance	C_I	f_{CP} = 1 MHz	—	5	—	pF

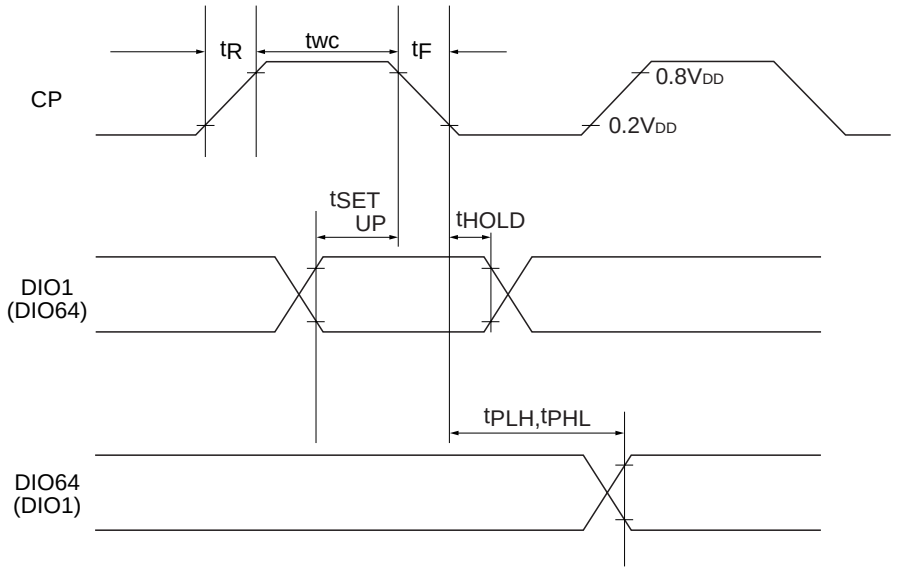
Note

$V_{DE} = V_1$ or V_2 or V_5 or V_{EE}, $V_l = V_{DD}$, $V_2 = 10/11 \times (V_{DD} - V_{EE})$, $V_5 = l/11 \times (V_{DD} - V_{EE})$

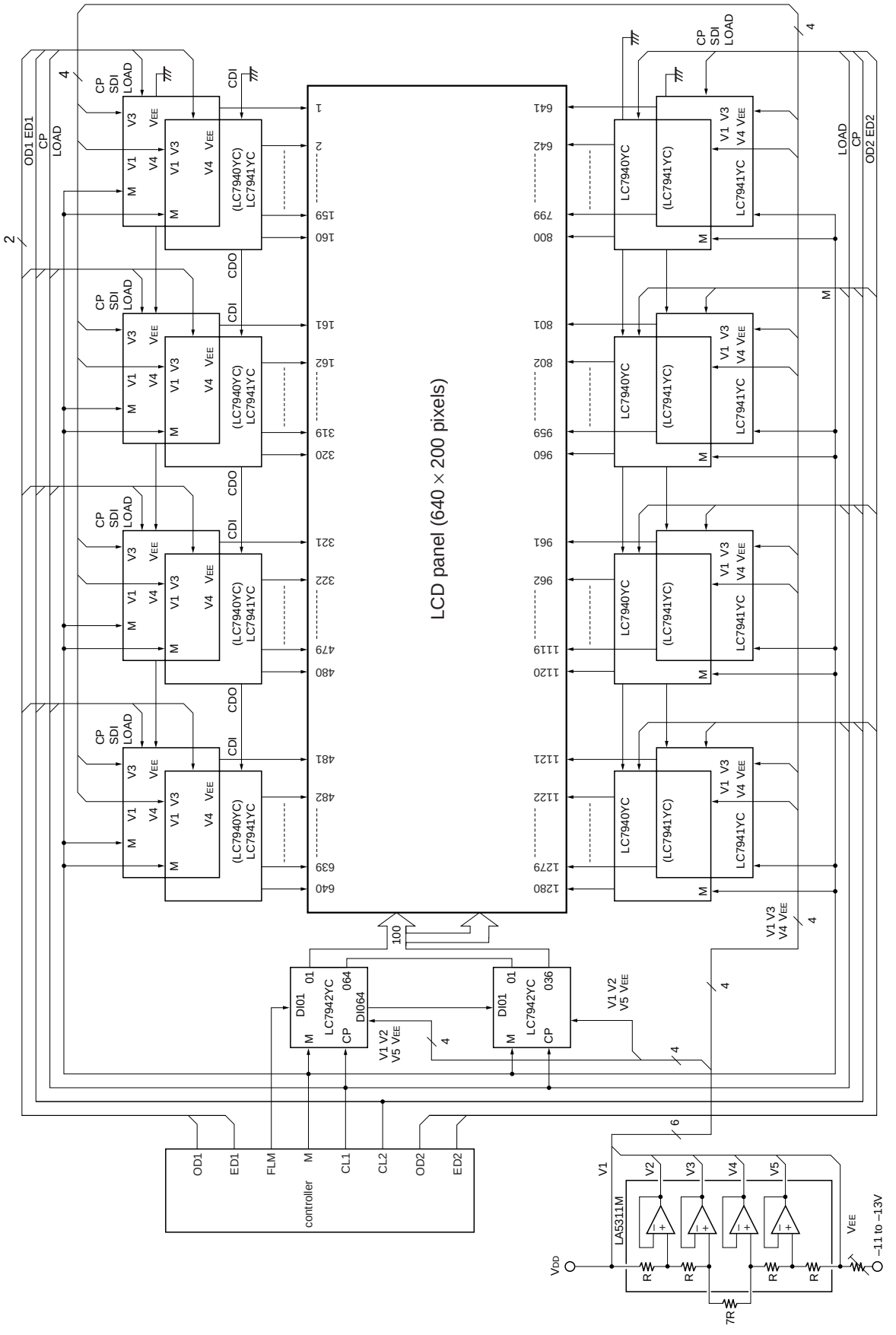
Switching Characteristics at Ta = 25 ± 2 °C, V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output delay time	t_{PLH}	C_L = 30 pF	–	–	250	ns
	t_{PHL}		–	–	250	

Switching Characteristics Waveform



LCD Panel


LCD panel (640 × 200 pixels)
LC7940YC
LC7941YC
(LC7940YC)
LC7941YC
LC7942YC
LA5311M
controller
OD1
ED1
FLM
M
CL1
CL2
OD2
ED2
CP
SDI
LOAD
CDI
CDO
V1
V2
V3
V4
V5
VEE
VDD
R
7R
–11 to –13V