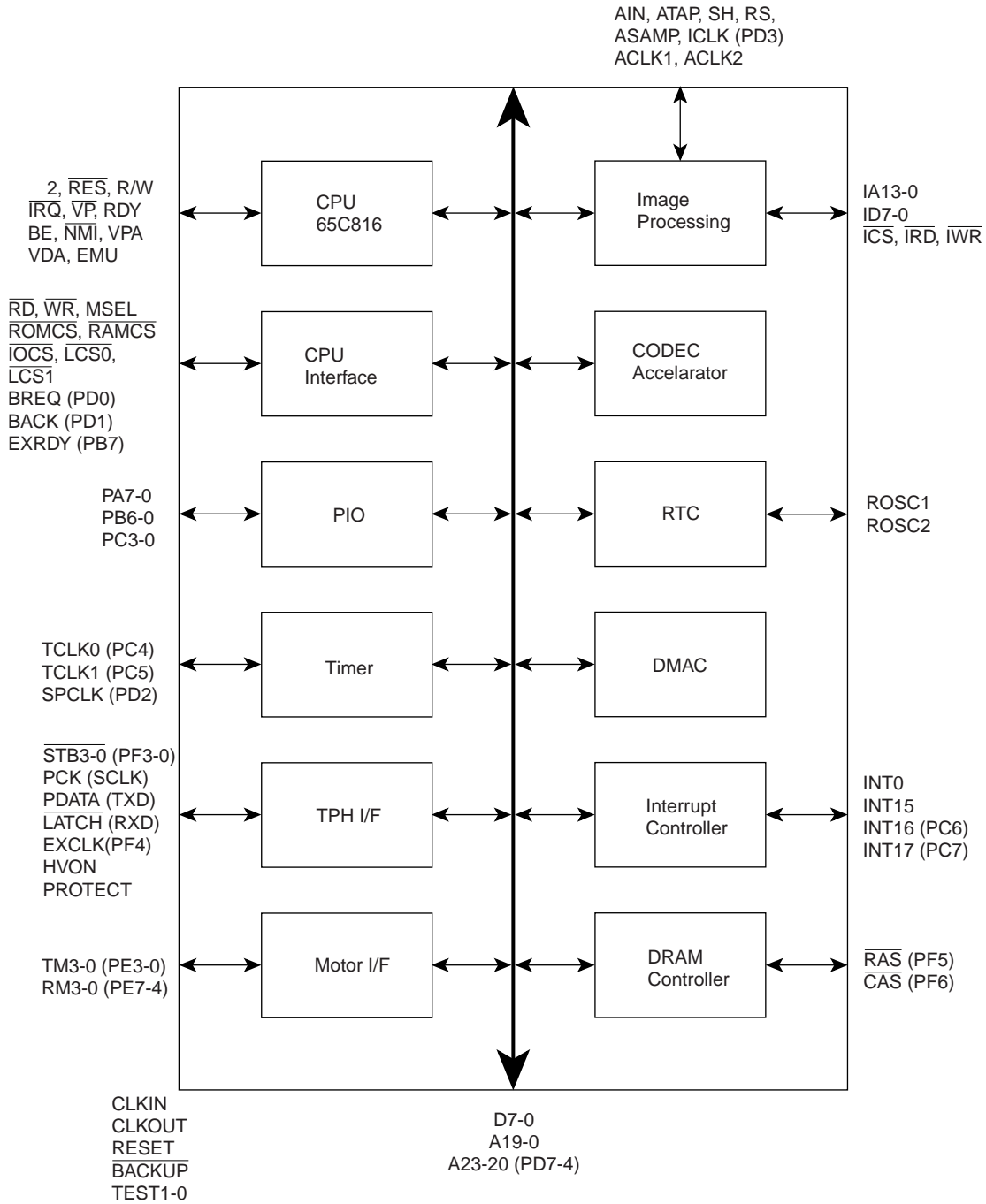




**Block Diagram**



**Pin Functions**

Number	Name	I/O <sup>1</sup>	Description
1	V <sub>SS</sub>	P	Ground connection pin
2	$\overline{RD}$	O	Read signal from CPU
3	$\overline{WR}$	O	Write signal from CPU
4	$\overline{ROMCS}$	O	Program ROM chip select signal
5	$\overline{RAMCS}$	O	Work RAM chip select signal

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Number	Name	I/O <sup>1</sup>	Description
6	$\overline{\text{IOCS}}$	O	External I/O chip select signals
7	$\overline{\text{LCS0}}$	O	
8	$\overline{\text{LCS1}}$	O	
9	MSEL	I	CPU memory space select signal
10	INT0	I	External interrupt request signals
11	INT15	I	
12	D7	B	Data bus
13	D6	B	
14	D5	B	
15	D4	B	
16	D3	B	
17	D2	B	
18	D1	B	
19	D0	B	
20	V <sub>DD</sub>	P	Supply pin
21	V <sub>SS</sub>	P	Ground connection pin
22	A23(PD7)	B	Address bus/General-purpose port D
23	A22(PD6)	B	
24	A21(PD5)	B	
25	A20(PD4)	B	
26	A19	O	Address bus
27	A18	O	
28	A17	O	
29	A16	O	
30	$\phi 2$	O	ICE system clock
31	$\overline{\text{RES}}$	O	ICE reset signal
32	R/W	I	ICE read/write signal
33	$\overline{\text{IRQ}}$	O	ICE interrupt request signal
34	$\overline{\text{VP}}$	I	ICE vector address signal
35	RDY	O	ICE ready signal
36	BE	O	ICE bus enable signal
37	VPA	I	ICE valid program address signal
38	VDA	I	ICE valid data address signal
39	$\overline{\text{NMI}}$	I	Non-maskable interrupt request signal
40	V <sub>DD</sub>	P	Supply pin
41	V <sub>SS</sub>	P	Ground connection pin
42	A15	O	Address bus
43	A14	O	
44	A13	O	
45	A12	O	
46	A11	O	
47	A10	O	
48	A9	O	
49	A8	O	

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Number	Name	I/O <sup>1</sup>	Description
50	PA7	B	General-purpose port A
51	PA6	B	
52	PA5	B	
53	PA4	B	
54	PA3	B	
55	PA2	B	
56	PA1	B	
57	PA0	B	
58	ROSC1	I	RTC crystal oscillator connection pins
59	ROSC2	O	
60	V <sub>DD</sub>	P	Supply pin
61	V <sub>SS</sub>	P	Ground connection pin
62	A7	O	Address bus
63	A6	O	
64	A5	O	
65	A4	O	
66	A3	O	
67	A2	O	
68	A1	O	
69	A0	O	
70	EXRDY(PB7)	B	External ready signal/General-purpose port B
71	PB6	B	General-purpose port B
72	PB5	B	
73	PB4	B	
74	PB3	B	
75	PB2	B	
76	PB1	B	
77	PB0	B	
78	CLKIN	B	System clock crystal oscillator connection pins
79	CLKOUT	O	
80	V <sub>DD</sub>	P	Supply pin
81	V <sub>SS</sub>	P	Ground connection pin
82	INT17(PC7)	B	External interrupt request signals/General-purpose port C
83	INT16(PC6)	B	
84	TCLK1(PC5)	B	Timer external clock inputs/General-purpose port C
85	TCLK0(PC4)	B	
86	PC3	B	General-purpose port C
87	PC2	B	
88	PC1	B	
89	PC0	B	
90	RM3(PE7)	B	Receive motor phase signals/General-purpose port E
91	RM2(PE6)	B	
92	RM1(PE5)	B	
93	RM0(PE4)	B	

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Number	Name	I/O <sup>1</sup>	Description
94	TM3(PE3)	B	Transmit motor phase signals/General-purpose port E
95	TM2(PE2)	B	
96	TM1(PE1)	B	
97	TM0(PE0)	B	
98	PDATA(TXD)	O	Thermal head serial output data/Serial I/O transmit data
99	PCK(SCLK)	B	Thermal head data transmission clock/Serial I/O clock
100	V <sub>DD</sub>	P	Supply pin
101	V <sub>SS</sub>	P	Ground connection pin
102	LATCH(RDX)	B	Thermal head data latch signal/Serial I/O receive data
103	STB3(PF3)	B	Thermal head strobe signals/General-purpose port F
104	STB2(PF2)	B	
105	STB1(PF1)	B	
106	STB0(PB0)	B	
107	EXCLK(PF4)	B	Thermal head control external clock/General-purpose port F
108	HVON	O	Head voltage ON/OFF control signal
109	PROTECT	I	Head protection abnormality signal input
110	ID7	B	Image processor memory data bus
111	ID6	B	
112	ID5	B	
113	ID4	B	
114	ID3	B	
115	ID2	B	
116	ID1	B	
117	ID0	B	
118	ACLK1	O	Image sensor transmission clocks
119	ACLK2	O	
120	V <sub>DD</sub>	P	Supply pin
121	V <sub>SS</sub>	P	Ground connection pin
122	AVDD	P	Analog supply pin
123	AIN	I	Analog image signal input
124	TEMP	I	Thermistor input
125	ATAP	I	Built-in A/D converter reference voltage
126	AVSS	P	Analog ground connection
127	RESET	I	Reset signal
128	SH	O	Image sensor start pulse
129	RS	O	Image sensor reset pulse
130	ASAMP	O	Built-in A/D converter sampling point monitor signal
131	IR <sub>D</sub>	O	Image processor memory read signal
132	I <sub>W</sub> R	O	Image processor memory write signal

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Number	Name	I/O <sup>1</sup>	Description
133	IA13	O	Image processor memory address bus
134	IA12	O	
135	IA11	O	
136	IA10	O	
137	IA9	O	
138	IA8	O	
139	IA7	O	
140	V <sub>DD</sub>	P	Supply pin
141	V <sub>SS</sub>	P	Ground connection pin
142	$\overline{\text{RAS}}$ (PF5)	B	DRAM address strobes/General-purpose port F
143	$\overline{\text{CAS}}$ (PF6)	B	
144	IA6	O	Image processor memory address bus
145	IA5	O	
146	IA4	O	
147	IA3	O	
148	IA2	O	
149	IA1	O	
150	IA0	O	
151	$\overline{\text{ICS}}$	O	Image processor memory chip select
152	ICLK(PD3)	B	Image processor external clock/General-purpose port D
153	SPCLK(PD2)	B	Speaker clock output/General-purpose port D
154	BACK(PD1)	B	External master device bus acknowledge signal/General-purpose port D
155	BREQ(PD0)	B	External master device bus request signal/General-purpose port D
156	TEST1	I	Test pin
157	TEST0	I	
158	$\overline{\text{BACKUP}}$	I	Power-down signal
159	EMU	I	ICE monitor in-operation signal
160	V <sub>DD</sub>	P	Supply pin

1. I = input, B = bidirectional, O = output, P = power

## Specifications

### Absolute Maximum Ratings at V<sub>SS</sub> = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>DD max</sub>	T <sub>a</sub> = 25°C	-0.3 to +7.0	V
Input/output voltage	V <sub>I</sub> , V <sub>O</sub>	T <sub>a</sub> = 25°C	-0.3 to V <sub>DD</sub> + 0.3	V
Allowable power dissipation	P <sub>d max</sub>	T <sub>a</sub> ≤ 70°C	600	mW
Operating temperature	T <sub>opr</sub>		-30 to +70	°C
Storage temperature	T <sub>slg</sub>		-55 to +125	°C
Soldering temperature	T <sub>sol</sub>	Manual soldering (3s)	350	°C
		Reflow soldering (10s)	235	°C

### Allowable Operating Ranges at T<sub>a</sub> = -30 to +70°C, V<sub>SS</sub> = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V <sub>DD</sub>		4.5	-	5.5	V
Input voltage	V <sub>IN</sub>		0	-	V <sub>DD</sub>	V

**DC Characteristics** at  $T_a = -30$  to  $+70^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high-level voltage	$V_{IH1}$	All inputs except PCK (SCLK)	2.2	–	–	V
Input low-level voltage	$V_{IL1}$	All inputs except PCK (SCLK)	–	–	0.8	V
Input high-level voltage	$V_{IH2}$	PCK (SCLK), Schmitt trigger input	2.5	–	–	V
Input low-level voltage	$V_{IL2}$	PCK (SCLK), Schmitt trigger input	–	–	0.6	V
Input leakage current	$I_L$		–25	–	+25	$\mu\text{A}$
Output high-level voltage	$V_{OH}$	$I_{OH} = -3\text{mA}$	2.4	–	–	V
Output low-level voltage	$V_{OL}$	$I_{OL} = 3\text{mA}$	–	–	0.4	V
Output leakage current	$I_{OZ}$	High-impedance output	–100	–	+100	$\mu\text{A}$
Oscillator frequency	$f_{CLK1}$	CLKIN, CLKOUT	–	–	16	MHz
	$f_{CLK2}$	ICLK, TCLK0, TCLK1	–	–	16	MHz
	$f_{CLK3}$	ROSC1,ROSC2	–	32.768	–	kHz
Current dissipation	$I_{DD1}$	Operating normally	–	50	90	mA
	$I_{DD2}$	Power-down, $V_{DD} = 3\text{V}$ , BACKUP = LOW	–	5	–	$\mu\text{A}$

**Function Outline**

**CPU Peripheral Circuits**

- Generates 80-series CPU compatible CS/RD/WR signals
- Chip select signal outputs for program ROM, SRAM and I/O device connections
- ROM, SRAM, and DRAM sizes settable in 64KB units
- Inserts wait cycles when accessing ROM, SRAM and I/O
- Internal/external DMA controller bus arbitration function

**Image Processor**

- Number of processed picture elements (pixels)
  - 2048 pixels/line (uses 64K memory, with black and white correction)
  - 4096 pixels/line (uses 64K memory, with white correction only)
  - 4096 pixels/line (uses 256K memory, with black and white correction)
- 500ns/pixels max. processing rate
- 1 external, medium-speed memory
  - 100ns access time at 500ns/pixels rate
- Various kinds of clocks
  - Internal clock mode, with 1, 1/2, 1/4, 1/8 frequency division capability
  - External clock mode, with optional external clock input capability
- AGC, 8-bit A/D converter built-in (with delay adjust function)
- Thermal printer head temperature monitor function
- Sensor drive circuit (CCD, various CIS types)
- Digital clamp (dot clamp, even-odd clamp)

- Distortion correction (white, black, all pixels)
- $\gamma$  correction (user-definable curve)
- Simple two-value processing (fixed threshold value, density-adjusted threshold value)
- Half-tone processing
  - Systematic dither method (64 gradations), dither threshold value adjustable
  - Error diffusion method (64 gradations)
- Image reduction (thinning out, black fine line hold, white fine line hold)

**Codec Accelerator**

- Image data dot change detection, run-length or line start absolute address output
- Run-length image data coding
- Maximum 4K run-length processing
- Image data DMA transmission capability

**TPH Interface**

- 4MHz, 2MHz, 1MHz and 500MHz transmission clock frequency
- Switchable rising-edge/falling-edge clock phase
- Strobe division: 1, 2, and 4
- Strobe width: 32 $\mu\text{s}$  to 8.16ms
- Switchable strobe and latch pulse polarity
- Strobe and latch pulse can be generated manually and treated as a general-purpose output port
- Head supply ON/OFF control
- Head protection input pin (PROTECT) setup
  - Mode 1: HVON and STB0 to STB3 are set to inactive state after a continuous low-level input of approximately 64 ms
  - Mode 2: HVON and STB0 to STB3 are set to inactive state immediately after a low-level signal input.

**Motor Interface**

- Transmit/receive 2-channel stepping motor interface
- 4-phase motor (excitation method: 1 phase/2 phases/1-2 phases)
- Forward/reverse-selectable control register
- Motor output polarity selectable
- 2 phase change triggers (register-selectable) for both transmit and receive
  - Transmit motor trigger
    - Phase change by register bit ON/OFF
    - Phase change by image processor-controlled motor phase advance trigger
  - Receive motor trigger
    - Phase change by register bit ON/OFF
    - Phase change by timer 3 output

**DMA Controller**

- 3-channel transmission, memory ↔ I/O
  - Channel 0: Image processor → memory
  - Channel 1: Codec accelerator ↔ memory
  - Channel 2: Memory → TPH interface
- Channel 2 supporting a latchless head
- 16MB addresses/64K transfer count
- 2.6MB/s max. transfer speed
- Individual DMA request permit/prohibit
- Auto-initialization function
- Fixed precedence order: channel 0 > channel 1 > Channel 2

**Timer**

- 6 independent 16-bit counters on-chip
- 8-bit prescaler on-chip for each counter
- 244Hz to 15.6kHz speaker clock generator
- External clock inputs selectable for timer 0 and timer 1

**DRAM Controller**

- 256K/1M/4Mb DRAM support, up to 120ns access time supported
- CAS-before-RAS refresh
- Employs early-write mode
- Internal refresh counter: 4ms refresh time for 256K, 8ms for 1M, 16ms for 4M
- Register setting capability for 9 dummy refresh cycle execution

**Interrupt Controller**

- 18-level interrupt control (internal: 14 levels, external: 4 levels)
- Individual level mask processing
- Interrupt vector address output

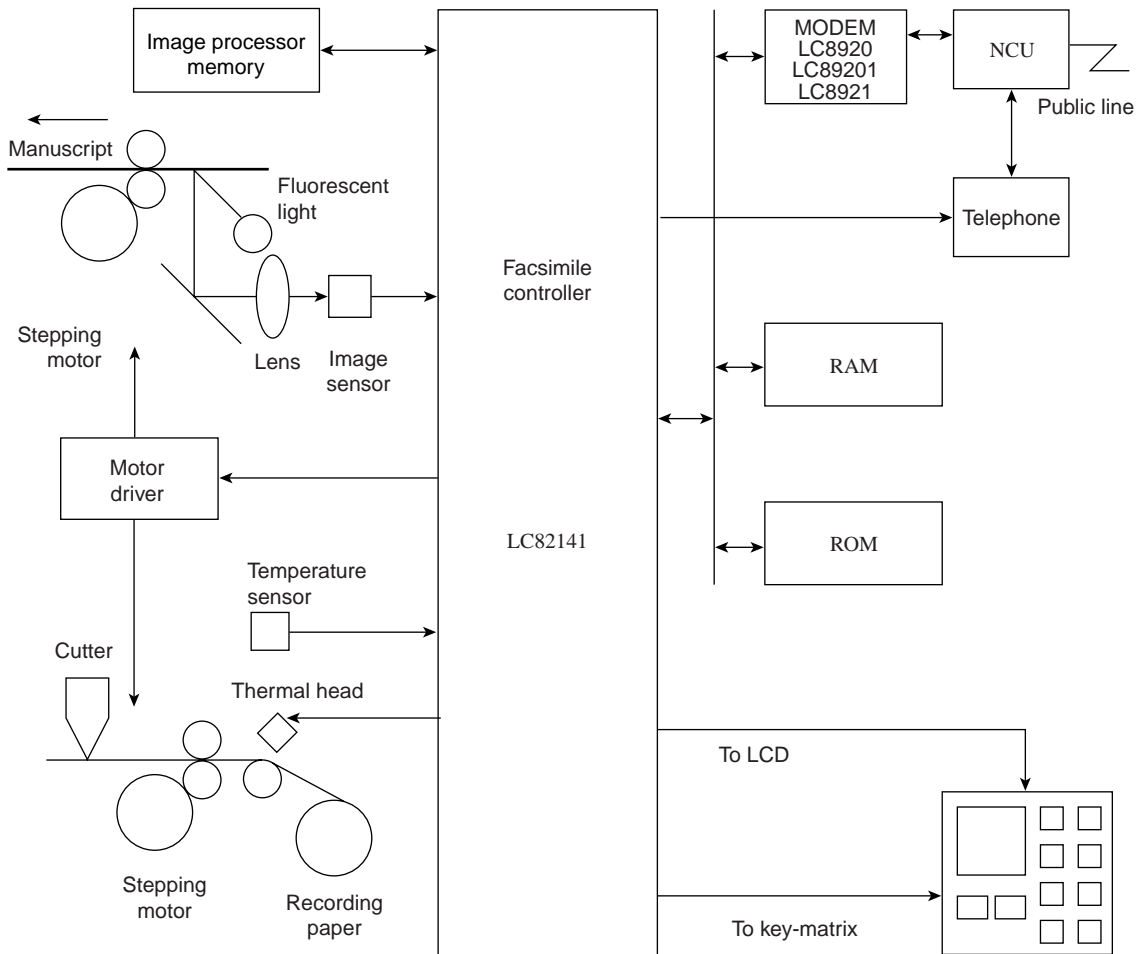
**RTC**

- Time function with alarm
- 100-year calendar
- 12-hour/24-hour time display, summer time set capability
- Leap year, short/long month auto-correction
- Selectable binary or BCD data for time, calendar and alarm
- 3 types of interrupts
  - Alarm interrupt
  - Periodic interrupt
  - Update ended interrupt

**General-Purpose Ports**

- 20 to 32 input/output ports
- Each port can be configured as an input or output
- Extendable up to 47 ports by switchover to dedicated pins

Sample Application Circuit



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