



LC86P6032

8-Bit Single-Chip Microcontroller

Overview

The LC86P6032 microcontroller is a CMOS 8-bit single chip microcontroller with one-time PROM for LC866000 series. This microcontroller has the same functions and pin assignment as for the LC866000 series mask ROM version, and a 32K-byte PROM.
 The LC86P6032 uses the same DIP/QFP package as the mask ROM version.
 This is ideal for faster ramp up of initial set shipments, and for reducing the changeover time when running small production lots or when changing specifications.

Features

- (1) Option switching using PROM data
 The optional functions of the LC866000 series can be specified using PROM data.
 LC86P6032 can be checked the functions of trial piece using mass production board.
- (2) Internal 32K-byte PROM
 32K-byte PROM is built in. This corresponds to LC866032B/24AB/20A/16A/12A/08A.
- (3) The pin and package compatible with mask ROM version
- (4) The characteristics compatible with mask ROM version.
- (5) Factory shipment
 DIP-64S
 QFP-64E (Under development)

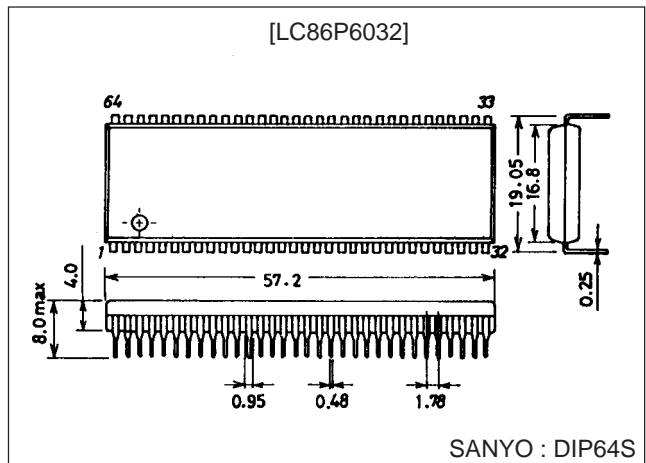
Sanyo's ROM Programming Service

Sanyo offers a fee-based service that programs the ROM in one-time programmable microcontrollers, stamps ths devices, screens the devices, and performs a read check of the devices. For details, contact your sales representative.

Package Dimensions

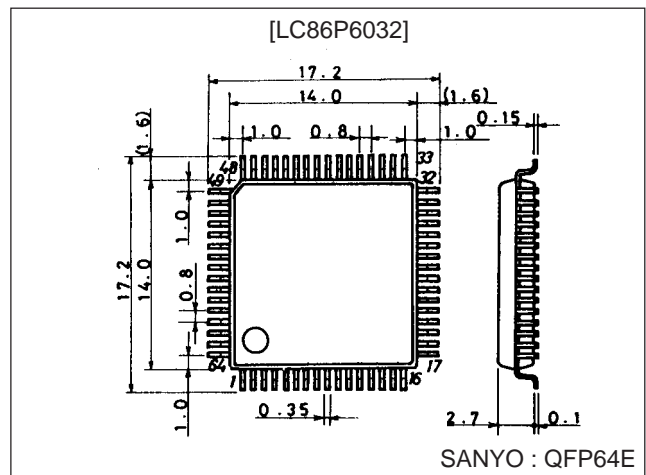
unit : mm

3071-DIP64S



unit : mm

3159-QFP64E



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Notice for Use

LC86P6032 is provided for the first release and small shipping of LC866000 series.
At using, take notice of the followings.

(1) Reset

It is necessary to be sure to go into 'L' level and hold for 200 μ s to reset terminal ($\overline{\text{RES}}$) after power supplied voltage has been over inferior limit of supply voltage.

The option is specified until 3ms after going into 'H' level to reset terminal by degrees.

The program is executed from 00H of program counter.

The output form of all ports are N-channel open-drain while 'L' level to reset terminal.

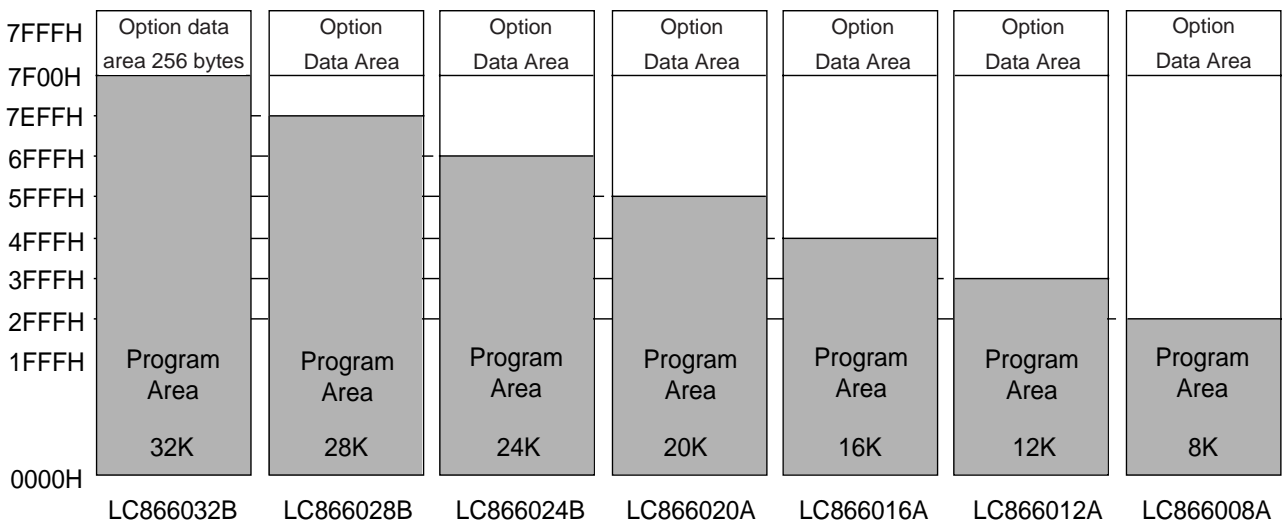
(2) Option

The LC86P6032 uses 256 bytes addressed 7F00H to 7FFFH in program memory as option data area.

This area does not affect the execution of program but means that the LC866032A program memory is 32512 bytes addressed 0000H to 7EFFH.

The option data is specified by the option-setting program "SU866000.EXE". The specified option data is linked to the program area by linkage editor "L866000.EXE".

(3) ROM space



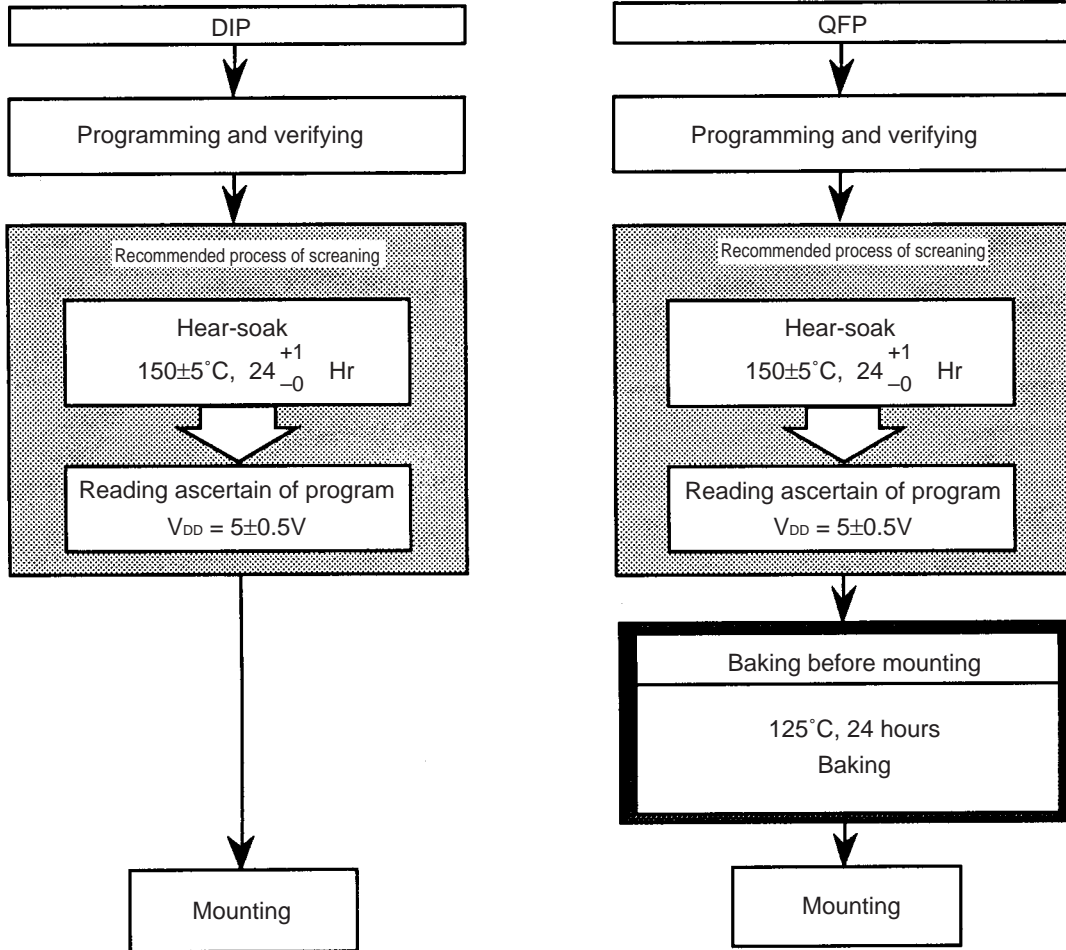
(4) Ordering information

- When ordering identical mask ROM and PROM devices simultaneously.
Provide an EPROM containing the target memory contents together with separate order forms for each of the mask ROM and PROM versions.
- When ordering a PROM device.
Provide an EPROM containing the target memory contents together with an order form.

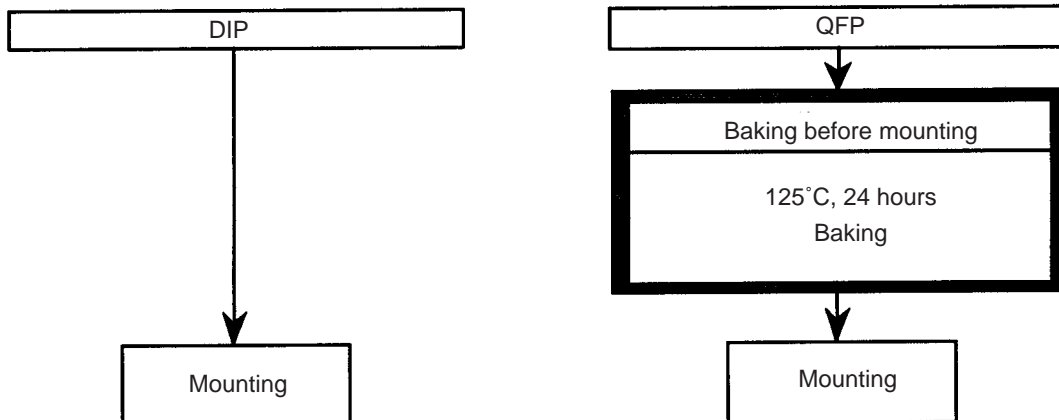
(5) Condition of Pre-mounting

a. Shipping with a blank PROM (Programming the data by yourself)

This microcontroller is provided DIP/QFP packages, but the condition before mounting is not the same. Refer to the mounting procedure as follows;



b. Shipping with a programmed PROM (Programming the data by Sanyo)



[Notes] • Do not immerse the package in the solder dip tank when mounting the QFP on the substrate.

• It is not possible to perform a write test on the blank PROM. 100% yield, therefore, cannot be guaranteed.

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(6) Points of difference LC86P6032 and LC866000 series

Item	LC86P6032	LC866032B/28B/24B/20A/16A/12A/08A
Operating temperature range (Topg)	+10°C to +40°C	-30°C to 70°C
Output form of port at reset	Open-drain output	Output form specified by option data
Output form of segment S0/T0 to S6/T6 S7/T7 to S15/T15 S16 to S23 S24 to S29	Pulldown resistance Not provided Provided (fixed) Provided (fixed) Not provided	Pulldown resistance: Provided/ Not provided Specified by option Provided (fixed) Specified by option Specified by option
Operating supply voltage range (V _{DD})	4.5 to 6.0V	2.5 to 6.0V

Option

A kind of option corresponding LC86P6032

Option type	Pins, Circuits	Contents of option
Input/output form of input/output ports	Port 0 (specified in a bit)	1. Input :No Pullup MOS transistor Output :N-channel open-drain 2. Input :Pullup MOS transistor Output :CMOS
	Port 1 (specified in a bit)	1. Input :Programmable pullup MOS transistor Output :N-channel open-drain 2. Input :Programmable pullup MOS transistor Output :CMOS
Pullup MOS transistor of input port	Port 7 (specified in a bit)	1. No Pullup MOS transistor 2. Pullup MOS transistor

A kind of option not corresponding LC86P6032

Option type	Pins, Circuits	Contents of option
Pulldown resistance of high voltage withstand output terminal	S0/T0 to S6/T6 S16 to S29 (specified in a bit)	1. Pulldown resistance 2. No Pulldown resistance

How to Use

(1) Specification of options

LC86P6032 must be programmed after specifying option data. The option is specified by "SU866000.EXE". The specified option file and the file created by our macro assembler "M866000.EXE" are linked by our linkage loader "L866000.EXE" which creates .HEX file, then the option code is put in the option specified area (7F00H to 7FFFH) of its .HEX file.

(2) How to write data to EPROM

When writing data that was created by the linker to the LC86P6032, a general-purpose EPROM programmer can be used by using special write conversion boards (W86EP6032D, W86EP6032Q).

- Recommended EPROM programmers

Supplier	EPROM programmer
Advantest	R4945, R4944, R4943
Andou	AF-9704
AVAL	PKW-1100, PKW-3000
Minato Electronics	MODEL 1890A

- "27512 (Vp-p = 12.5 V) Intel high-speed programming" mode should be used. The address must be set to "0000H to 7FFFH" and the jumper (DASEC) must be set 'OFF' at programming.

(3) How to use the data security function

"Data security" is a function to prevent the EPROM data from being read.

Instructions on using the data security function:

1. Set the jumper (DASEC) of the attachment 'ON'.
2. Attempt to program the EPROM.

The EPROM programmer displays an error. The error is a result of normal activity of the data security feature, and does not indicate a problem with the programmer or the LSI.

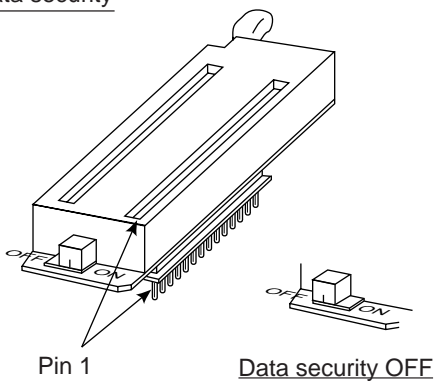
Notes

- The data security function is not carried out when the data of all address contain 'FF' at step 2 above.
- Data security cannot be executed when the sequential writing operation of programming "BLANK=>PROGRAM=>VERIFY" is used at step 2 above.

is used at step 2 above.

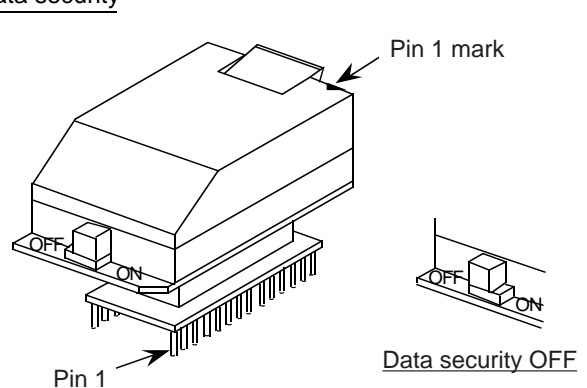
- Set the jumper 'OFF' after the execution of data security.

Data security



W86EP6032D

Data security



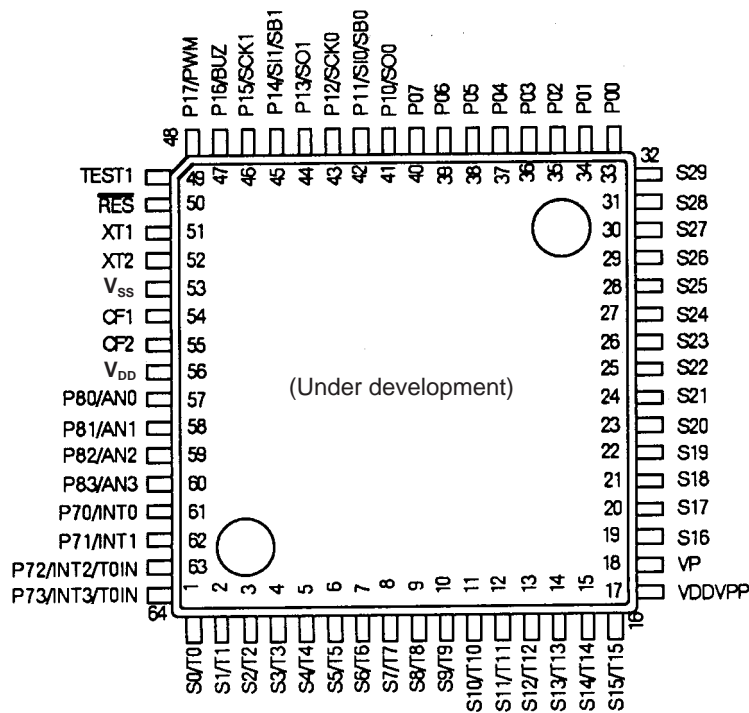
W86EP6032Q

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Pin Assignments

P10/SO0	1	64	P07
P11/SIO/SB0	2	63	P06
P12/SCK0	3	62	P05
P13/SO1	4	61	P04
P14/SI1/SB1	5	60	P03
P15/SCK1	6	59	P02
P16/BUZ	7	58	P01
P17/PWM	8	57	P00
TEST1	9	56	S29
RES	10	55	S28
XT1	11	54	S27
XT2	12	53	S26
V _{SS}	13	52	S25
CF1	14	51	S24
CF2	15	50	S23
V _{DD}	16	49	S22
P80/AN0	17	48	S21
P81/AN1	18	47	S20
P82/AN2	19	46	S19
P83/AN3	20	45	S18
P70/INT0	21	44	S17
P71/INT1	22	43	S16
P72/INT2/TOIN	23	42	VP
P73/INT3/TOIN	24	41	VDDVPP
S0/T0	25	40	S15/T15
S1/T1	26	39	S14/T14
S2/T2	27	38	S13/T13
S3/T3	28	37	S12/T12
S4/T4	29	36	S11/T11
S5/T5	30	35	S10/T10
S6/T6	31	34	S9/T9
S7/T7	32	33	S8/T8

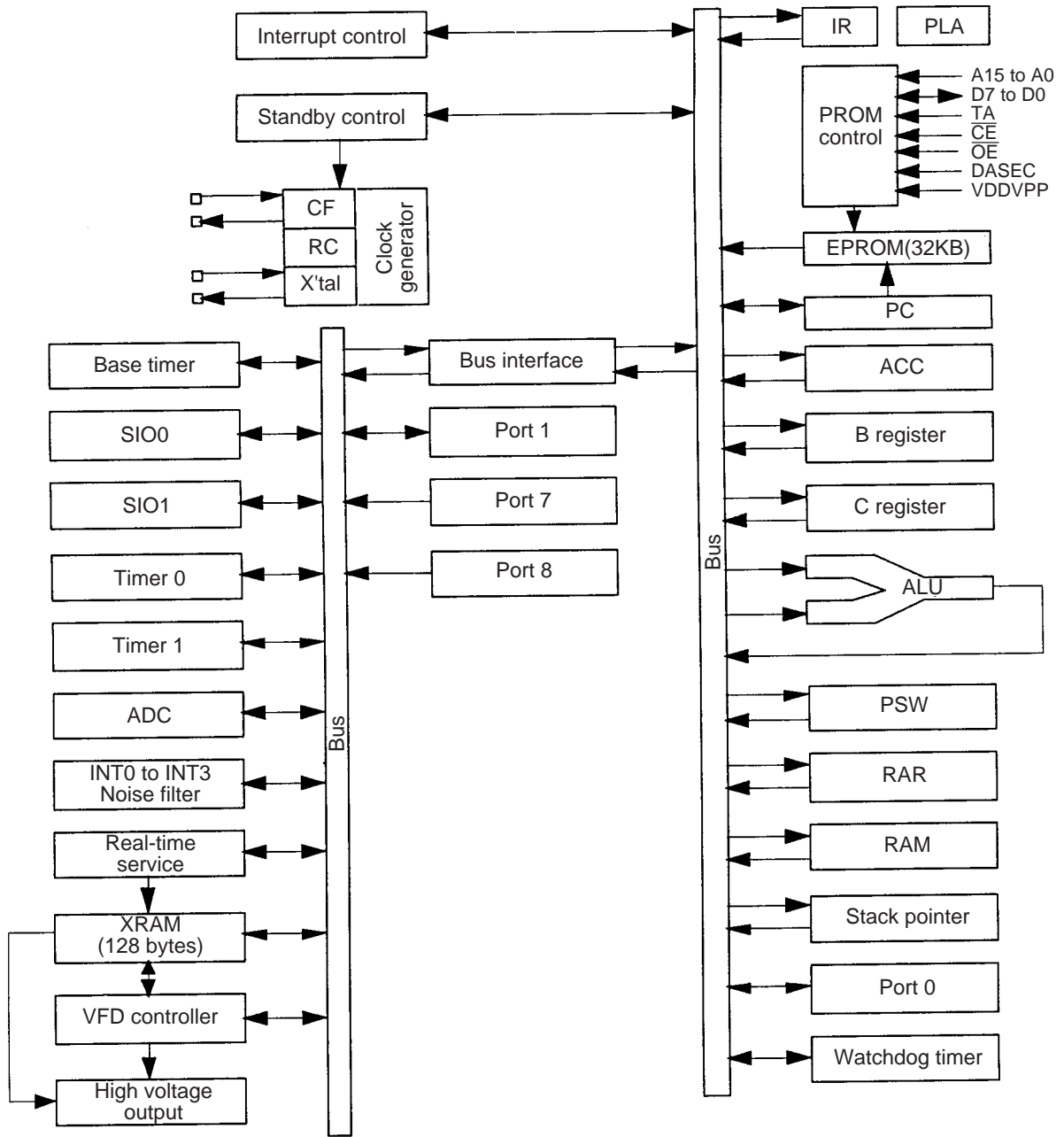
Top view



Top view

- Notes
- Pre-bake before mounting the QFP package on the substrate.
 - Do not immerse the package in the solder dip tank when mounting the QFP on the substrate.

System Block Diagram



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Continued from preceding page.

Pin name	I/O	Function description	Option	Function in PROM mode
S16 to S23	O	Output for VFD display controller Segment output Output with built-in pull-down resistance		Address input •A13 to A0
S24 to S29	O	Output for VFD display controller Segment output		
$\overline{\text{RES}}$	I	Reset pin		
TEST1	O	Test pin Should be left open.		
XT1	I	Input pin for 32.768 kHz crystal oscillation When not used, connect to V_{DD} .		
XT2	O	Output pin for 32.768 kHz crystal oscillation When not used, should be left open.		
CF1	I	Input pin for ceramic resonator oscillation		
CF2	O	Output pin for ceramic resonator oscillation		

*1 Memory select input for data security

*2 Output enable input

*3 Chip enable input

*4 TA → PROM control signal input

*5 A14 → Address input

* All of port options can be specified in bit unit.

* A state of pins at reset.

Pin name	Input/output mode	A state of pullup resistance specified at pullup option
Ports 0,7	Input	Fixed pullup resistance exists
Port 1	Input	Programmable pullup resistance OFF

Pin name	A state of P-channel transistor
S0/T0 to S15/T15	P-channel transistor OFF
S16 to S29	P-channel transistor OFF

Specifications

1. Absolute Maximum Ratings at Ta = 25°C, VSS = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit		
				V _{DD} [V]	min	typ		max	
Maximum supply voltage	V _{DD} max	V _{DD} , V _{DDVPP}	V _{DD} = V _{DDVPP}		-0.3		+7.0	V	
Input voltage	V _I (1)	• P71, 72, 73 • Port 8 • RES			-0.3		V _{DD} +0.3		
	V _I (2)	VP			V _{DD} -45		V _{DD} +0.3		
Output voltage	V _O	• S0/T0 to S15/T15 • S16 to S29			V _{DD} -45		V _{DD} +0.3		
Input/output voltage	V _{IO}	Ports 0, 1, P70			-0.3		V _{DD} +0.3		
High-level output current	Peak output current	I _{OPH} (1)	Ports 0, 1	• CMOS output • At each pin		-4			mA
		I _{OPH} (2)	S0/T0 to S15/T15	At each pin		-30			
		I _{OPH} (3)	S16 to S29	At each pin		-15			
	Total output current	∑I _{OA} H(1)	Port 0	Total of all pins		-10			
		∑I _{OA} H(2)	Port 1	Total of all pins		-10			
		∑I _{OA} H(3)	• S0/T0 to S15/T15 • S16 to S29	Total of all pins		-130			
Low-level output current	Peak output current	I _{OPL} (1)	Ports 0, 1	At each pin				20	
		I _{OPL} (2)	P70	At each pin				15	
	Total output current	∑I _{OAL} (1)	Port 0	Total of all pins				40	
		∑I _{OAL} (2)	Port 1, P70	Total of all pins				40	
Allowable power dissipation	P _d max(1)	DIP64S	Ta = -30°C to +70°C				760	mW	
	P _d max(2)	QFP64E	Ta = -30°C to +70°C		Under development				
Operating temperature range	T _{opr}				-30		70	°C	
Storage temperature range	T _{stg}				-65		150		

Notes • Pre-bake before mounting the QFP package on the substrate.

• Do not immerse the package in the solder dip tank when mounting the QFP on the substrate.

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2. Allowable Operating Conditions at Ta = -30°C to +70°C, VSS = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit	
				VDD[V]	min	typ		max
Operating supply voltage range	VDD	VDD	0.98 μs ≤ tCYC tCYC ≤ 400 μs		4.5		6.0	V
HOLD voltage	VHD	VDD	<ul style="list-style-type: none"> When in HOLD mode RAM and registers retain previous data. 		2.0		6.0	
Pulldown supply voltage	Vp	VP		4.5 to 6.0	-35		VDD	
Input high-level voltage	VIH(1)	Port 0 (Schmitt)	Output disabled	4.5 to 6.0	0.4VDD +0.9		VDD	
	VIH(2)	<ul style="list-style-type: none"> Port 1 P72, 73 (Schmitt) 	Output disabled	4.5 to 6.0	0.75VDD		VDD	
	VIH(3)	<ul style="list-style-type: none"> P70 Port input/interrupt. P71 RES (Schmitt) 	Output N-channel transistor OFF	4.5 to 6.0	0.75VDD		VDD	
	VIH(4)	P70 Watchdog timer	Output N-channel transistor OFF	4.5 to 6.0	0.9VDD		VDD	
	VIH(5)	Port 8			4.5 to 6.0	0.75VDD		VDD
Input low-level voltage	VIL(1)	Port 0 (Schmitt)	Output disabled	4.5 to 6.0	VSS		0.2VDD	
	VIL(2)	<ul style="list-style-type: none"> Port 1 P72, 73(Schmitt) 	Output disabled	4.5 to 6.0	VSS		0.25VDD	
	VIL(3)	<ul style="list-style-type: none"> P70 Port input/interrupt. P71 RES (Schmitt) 	N-channel transistor OFF	4.5 to 6.0	VSS		0.25VDD	
	VIL(4)	P70 Watchdog timer	N-channel transistor OFF	4.5 to 6.0	VSS		0.8VDD -1.0	
	VIL(5)	Port 8			4.5 to 6.0	VSS		0.25VDD
Operation cycle time	tCYC			4.5 to 6.0	0.98		400	μs
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	<ul style="list-style-type: none"> 12 MHz (ceramic resonator oscillation). Refer to Figure 1. 	4.5 to 6.0	11.76	12	12.24	MHz
	FmCF(2)	CF1, CF2	<ul style="list-style-type: none"> 3 MHz (ceramic resonator oscillation). Refer to Figure 1. 	4.5 to 6.0	2.94	3	3.06	
	FmRC		RC oscillation	4.5 to 6.0	0.4	0.8	2.0	
	FsXtal	XT1, XT2	<ul style="list-style-type: none"> 32.768 kHz (crystal oscillation). Refer to Figure 2. 	4.5 to 6.0		32.768		kHz
Oscillation stable time period (Note 1)	tmsCF(1)	CF1, CF2	<ul style="list-style-type: none"> 12 MHz (ceramic resonator oscillation). Refer to Figure 3. 	4.5 to 6.0		0.02	0.2	ms
	tmsCF(2)	CF1, CF2	<ul style="list-style-type: none"> 3 MHz (ceramic resonator oscillation). Refer to Figure 3. 	4.5 to 6.0		0.1	1	
	tssXtal	XT1, XT2	<ul style="list-style-type: none"> 32.768 kHz (crystal oscillation). Refer to Figure 3. 	4.5 to 6.0		1	1.5	s

(Note 1) Refer to Table 1 and Table 2 for the oscillation constants.

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3. Electrical Characteristics at Ta= -30°C to +70°C , VSS = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit	
				VDD [V]	min	typ		max
Input high-level current	I _{IH} (1)	<ul style="list-style-type: none"> Port 1 Port 0 without pull-up MOS transistor 	<ul style="list-style-type: none"> Output disabled Pull-up MOS transistor OFF. V_{IN} = V_{DD} (including off-state leak current of output transistor) 	4.5 to 6.0			1	μA
	I _{IH} (2)	<ul style="list-style-type: none"> Port 7 without pull-up MOS transistor Port 8 	V _{IN} = V _{DD}	4.5 to 6.0			1	
	I _{IH} (3)	<ul style="list-style-type: none"> RES 	V _{IN} = V _{DD}	4.5 to 6.0			1	
Input low-level current	I _{IL} (1)	<ul style="list-style-type: none"> Port 1 Port 0 without pull-up MOS transistor 	<ul style="list-style-type: none"> Output disabled Pull-up MOS transistor OFF. V_{IN} = V_{SS} (including off-state leak current of output transistor) 	4.5 to 6.0	-1			
	I _{IL} (2)	<ul style="list-style-type: none"> Port 7 without pull-up MOS transistor Port 8 	V _{IN} = V _{SS}	4.5 to 6.0	-1			
	I _{IL} (3)	<ul style="list-style-type: none"> RES 	V _{IN} = V _{SS}	4.5 to 6.0	-1			
Output high-level voltage	V _{OH} (1)	Ports 0, 1 at CMOS output	I _{OH} = -1.0 mA	4.5 to 6.0	V _{DD} -1			V
	V _{OH} (2)		I _{OH} = -0.1 mA	4.5 to 6.0	V _{DD} -0.5			
	V _{OH} (3)	S0/T0 to S15/T15	I _{OH} = -20 mA	4.5 to 6.0	V _{DD} -1.8			
	V _{OH} (4)	S16 to S29	<ul style="list-style-type: none"> I_{OH} = -1.0 mA The current of any unmeasurement pin is not over 1 mA. 	4.5 to 6.0	V _{DD} -1			
	V _{OH} (5)		I _{OH} = -5 mA	4.5 to 6.0	V _{DD} -1.8			
	V _{OH} (6)		<ul style="list-style-type: none"> I_{OH} = -1.0 mA The current of any unmeasurement pin is not over 1 mA. 	4.5 to 6.0	V _{DD} -1			
Output low-level voltage	V _{OL} (1)	Ports 0,1	I _{OL} = 10 mA	4.5 to 6.0			1.5	
	V _{OL} (2)		<ul style="list-style-type: none"> I_{OL} = 1.6 mA The total current of the Ports 0,1 is not over 40 mA 	4.5 to 6.0			0.4	
	V _{OL} (3)	P70	I _{OL} = 1 mA	4.5 to 6.0			0.4	
Pull-up MOS transistor resistor	R _{pu}	<ul style="list-style-type: none"> Ports 0, 1 Port 7 	V _{OH} = 0.9 V _{DD}	4.5 to 6.0	15	40	70	kΩ
Output off-state leak current	I _{OFF} (1)	<ul style="list-style-type: none"> S0/T0 to S6/T6 S24 to S29 (Without pulldown resistor) 	<ul style="list-style-type: none"> Output P-channel transistor OFF. V_{OUT} = V_{SS} 	4.5 to 6.0	-1			μA
	I _{OFF} (2)		<ul style="list-style-type: none"> Output P-channel transistor OFF. V_{OUT} = V_{DD}-40V 	4.5 to 6.0	-30			

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Parameter	Symbol	Pins	Conditions	Ratings			Unit	
				V _{DD} [V]	min	typ		max
Pulldown resistor	R _{pd}	<ul style="list-style-type: none"> S7/T7 to S15T15 S16 to S23 (With pulldown resistor) 	<ul style="list-style-type: none"> Output P-channel transistor OFF. V_{OUT}= 3V V_P= -30V 	5.0	60	100	200	kΩ
Hysteresis voltage	V _{HIS}	<ul style="list-style-type: none"> Ports 0,1 Port 7 $\overline{\text{RES}}$ 	Output disabled	4.5 to 6.0		0.1V _{DD}		V
Pin capacitance	CP	All pins	<ul style="list-style-type: none"> f=1MHz Unmeasurement terminals for input are set to V_{SS} level. T_a= 25°C 	4.5 to 6.0		10		pF

4. Serial Input/Output Characteristics at T_a = -30°C to +70°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit		
				V _{DD} [V]	min	typ		max	
Serial clock	Input clock	Cycle	tCKCY(1)	SCK0, SCK1	Refer to Figure 5.	4.5 to 6.0	2		tCYC
		Low-level pulse width	tCKL(1)			4.5 to 6.0	1		
		High-level pulse width	tCKH(1)			4.5 to 6.0	1		
	Output clock	Cycle	tCKCY(2)	SCK0, SCK1	<ul style="list-style-type: none"> Use pull-up resistance (1 kΩ) when set to open-drain output. Refer to Figure 5. 	4.5 to 6.0	2		
		Low-level pulse width	tCKL(2)			4.5 to 6.0		1/2tCKCY	
		High-level pulse width	tCKH(2)			4.5 to 6.0		1/2tCKCY	
Serial input	Data set-up time	tICK	<ul style="list-style-type: none"> SI0, SI1 SB0, SB1 	<ul style="list-style-type: none"> Data set-up to SCK0, 1 Refer to Figure 5. 	4.5 to 6.0	0.1		μs	
	Data hold time	tICKI			4.5 to 6.0	0.1			
Serial output	Output delay time (Serial clock is external clock.)	tCKO(1)	<ul style="list-style-type: none"> SO0, SO1 SB0, SB1 	<ul style="list-style-type: none"> Data hold from SCK0, 1 Use pull-up resistance (1 kΩ) when set to open-drain output. Refer to Figure 5. 	4.5 to 6.0			7/12tCYC +0.2	
	Output delay time (Serial clock is internal clock.)	tCKO(2)	<ul style="list-style-type: none"> SO0, SO1 SB0, SB1 	<ul style="list-style-type: none"> Data hold from SCK0, 1 Use pull-up resistance (1 kΩ) when set to open-drain output. Refer to Figure 5. 	4.5 to 6.0			1/3tCYC +0.2	

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5. Pulse Input Conditions at Ta = -30°C to +70°C, VSS = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit
				VDD [V]	min	typ	
High/low-level pulse width	tPIH(1) tPIL(1)	• INT0, INT1 • INT2/T0IN	• Interrupt acceptable • Timer 0 pulse countable	4.5 to 6.0	1		tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection clock selected to 1/1.)	• Interrupt acceptable • Timer 0 pulse countable	4.5 to 6.0	2		
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection clock selected to 1/64.)	• Interrupt acceptable • Timer 0 pulse countable	4.5 to 6.0	128		
	tPIL(4)	$\overline{\text{RES}}$	Reset acceptable	4.5 to 6.0	200		μs

6. A/D Converter Characteristics at Ta = -30°C to +70°C, VSS = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit	
				VDD [V]	min	typ		max
Resolution	N			4.5 to 6.0		8	bit	
Absolute precision	ET		(Note 2)				±1.5 LSB	
Conversion time	tCAD		A/D conversion time = 16 x tCYC (ADCR2 = 0) (Note 3)			15.68 (tCYC = 0.98 μs)	65.28 (tCYC = 4.08 μs)	μs
			A/D conversion time = 32 x tCYC (ADCR2 = 1) (Note 3)			31.36 (tCYC = 0.98 μs)	130.56 (tCYC = 4.08 μs)	
Analog input voltage range	VAIN	AN0 to AN3			VSS		VDD	V
Analog port input current	I _{AINH}		V _{AIN} = V _{DD}				1	μA
	I _{AINL}		V _{AIN} = V _{SS}		-1			

(Note 2) Absolute precision excepts quantizing error (±1/2 LSB).

(Note 3) The conversion time is the time from execution of the instruction to start conversion to the completion of shifting the A/D converted value to the register.

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7. Current Drain Characteristics at Ta = -30°C to +70°C , VSS = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit	
				V _{DD} [V]	min	typ		max
Current drain during basic operation (Note 4)	I _{DDOP} (1)	V _{DD}	<ul style="list-style-type: none"> • FmCF = 12 MHz for ceramic resonator oscillation. • FsXtal = 32.768 kHz for crystal oscillator. • System clock : 12 MHz side • Internal RC oscillator stopped. 	4.5 to 6.0		13	26	mA
	I _{DDOP} (2)		<ul style="list-style-type: none"> • FmCF = 3 MHz for ceramic resonator oscillation. • FsXtal = 32.768 kHz for crystal oscillator. • System clock : 3 MHz side • Internal RC oscillator stopped. 	4.5 to 6.0		6.5	14	
	I _{DDOP} (3)		<ul style="list-style-type: none"> • FmCF = 0 Hz (when oscillator stops). • FsXtal = 32.768 kHz for crystal oscillator. • System clock : RC oscillator. 	4.5 to 6.0		4	10	
	I _{DDOP} (4)		<ul style="list-style-type: none"> • FmCF = 0 Hz (when oscillator stops). • FsXtal = 32.768 kHz for crystal oscillator. • System clock : 32.768 kHz side • Internal RC oscillator stopped. 	4.5 to 6.0		3.5	9	

Continued on next page.

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Parameter	Symbol	Pins	Conditions	Ratings			Unit	
				V _{DD} [V]	min	typ		max
Current drain at HALT mode (Note 4)	I _{DDHALT} (1)	V _{DD}	<ul style="list-style-type: none"> • HALT mode • FmCF = 12 MHz for ceramic resonator oscillation. • FsXtal = 32.768 kHz for crystal oscillator. • System clock : 12 MHz side • Internal RC oscillator stopped. 	4.5 to 6.0		5	10	mA
	I _{DDHALT} (2)		<ul style="list-style-type: none"> • HALT mode • FmCF = 3 MHz for ceramic resonator oscillation. • FsXtal = 32.768 kHz for crystal oscillator. • System clock : 3 MHz side • Internal RC oscillator stopped. 	4.5 to 6.0		1.8	4.6	
	I _{DDHALT} (3)		<ul style="list-style-type: none"> • HALT mode • FmCF = 0 Hz (when oscillator stops). • FsXtal = 32.768 kHz for crystal oscillator. • System clock : RC oscillator 	4.5 to 6.0		400	800	μA
	I _{DDHALT} (4)		<ul style="list-style-type: none"> • HALT mode • FmCF = 0 Hz (when oscillator stops). • FsXtal = 32.768 kHz for crystal oscillator. • System clock : 32.768 kHz side • Internal RC oscillator stopped. 	4.5 to 6.0		20	60	
Current drain at HOLD mode (Note 4)	I _{DDHOLD} (1)	V _{DD}	HOLD mode	4.5 to 6.0		0.05	30	
	I _{DDHOLD} (2)			2.5 to 4.5		0.02	20	

(Note 4) The currents of output transistors and pull-up MOS transistors are ignored.

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Oscillation type	Supplier	Oscillator	C1	C2
12 MHz ceramic resonator oscillation	Murata	CSA12.0MTZ	33 pF	33 pF
		CSA12.0MT	33 pF	33 pF
	Kyocera	CST12.0MTW	on chip	
3 MHz ceramic resonator oscillation	Murata	CSA3.00MG	33pF	33 pF
		CST3.00MGW	on chip	
	Kyocera	KBR-3.0MS	47 pF	47 pF

* Both C1 and C2 must use K rank ($\pm 10\%$) and SL characteristics.

Table 1. Ceramic Resonator Oscillation Guaranteed Constants (Main-clock)

Oscillation type	Supplier	Oscillator	C3	C4
32.768 kHz crystal oscillation	Dai SINKU	DT-38(1TA252E00)	18 pF	18 pF
	Kyocera	KF-38G-13P0200	18 pF	18 pF

* Both C3 and C4 must use J rank ($\pm 5\%$) and CH characteristics.
(If high precision is unnecessary, use K rank ($\pm 10\%$) and SL characteristics.)

Table 2. Crystal Oscillation Guaranteed Constants (Sub-clock)

- Notes
- Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest pattern length.
 - If you use other oscillators herein, we provide no guarantee for the characteristics.

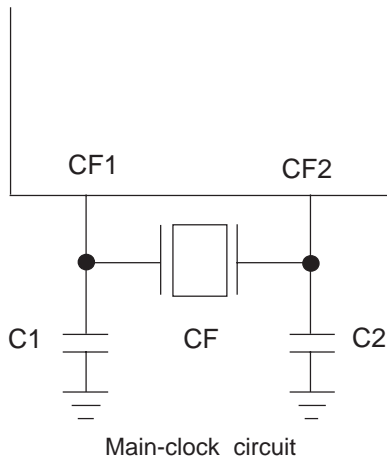


Figure 1 Ceramic Resonator Oscillation

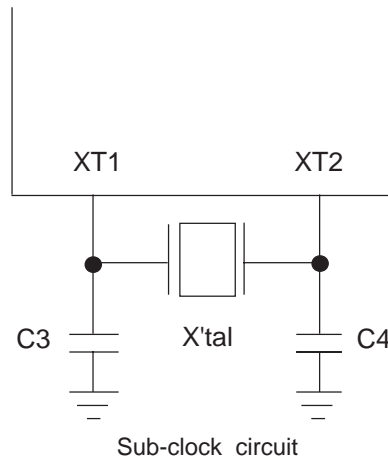


Figure 2 Crystal Oscillation

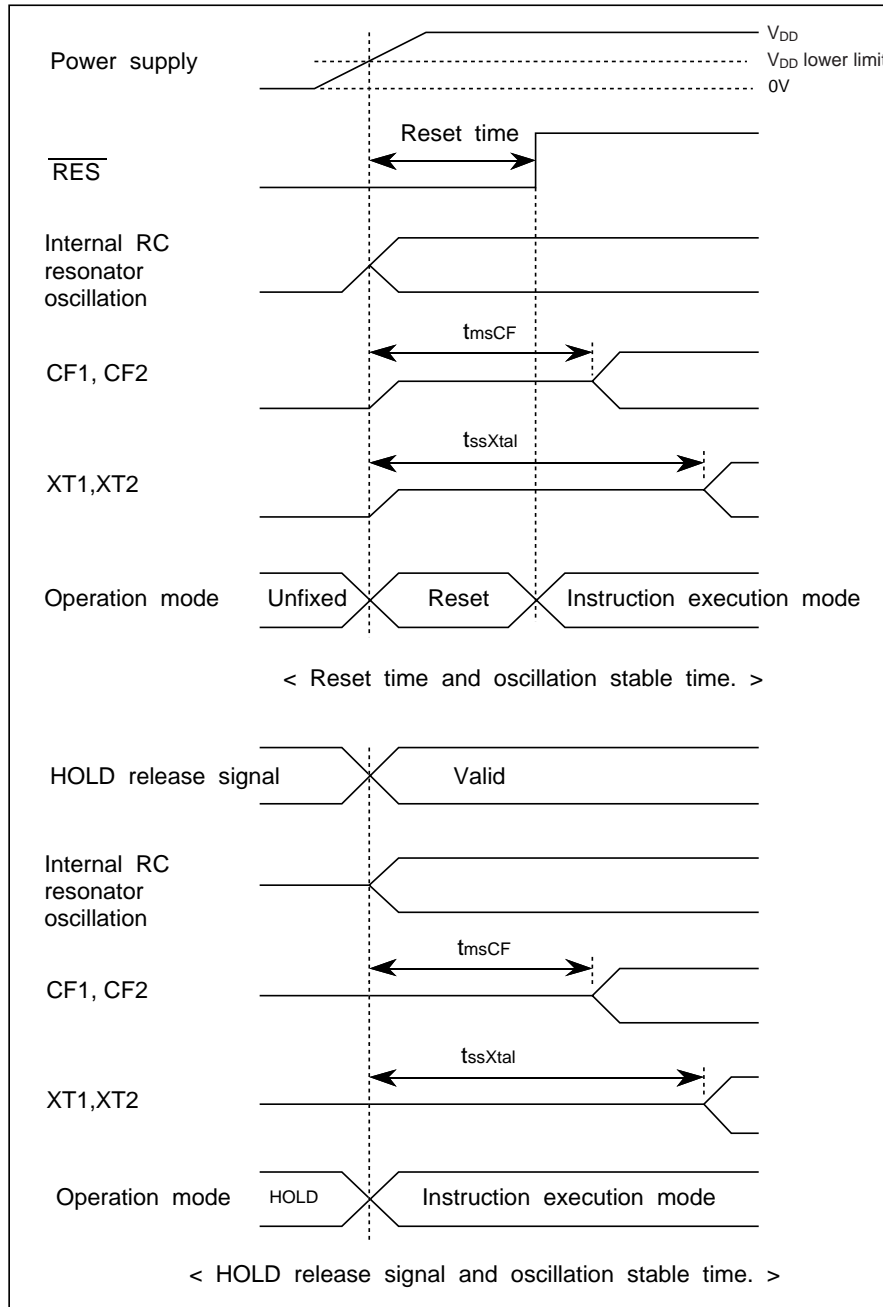
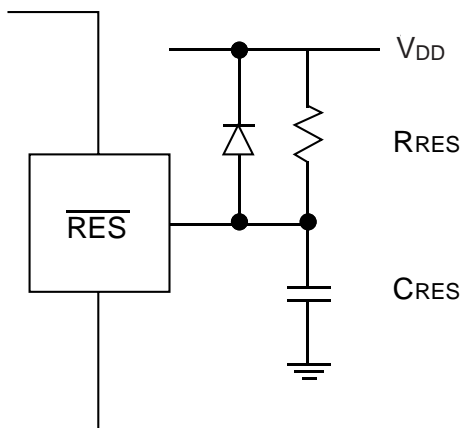


Figure 3 Oscillation Stable Time



(Note)
The values of C_{RES} and R_{RES} should be determined such that reset time is at least 200 μs, measured from the moment the power exceeds the V_{DD} lower limit.

Figure 4 Reset Circuit

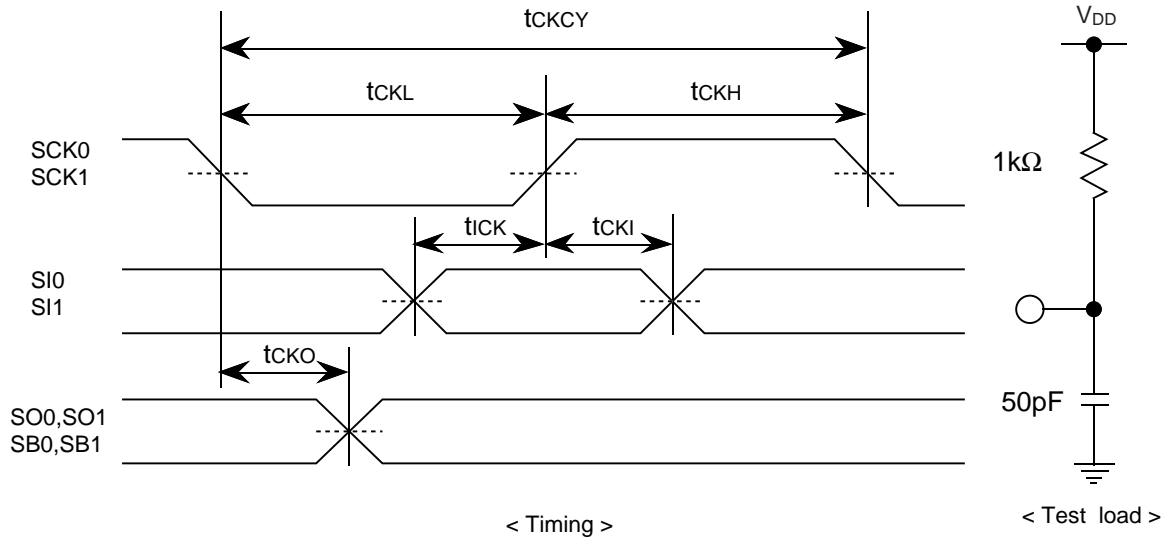
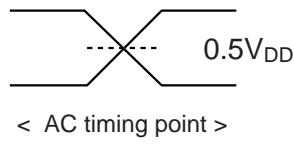


Figure 5 Serial Input/Output Test Conditions

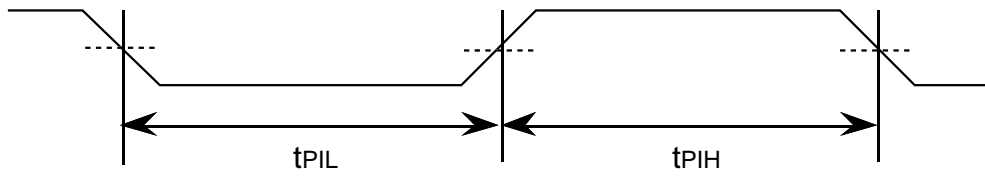


Figure 6 Pulse Input Timing Conditions

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