

MITSUBISHI ICs (TV)  
**M52025SP**

**PAL/NTSC VIDEO CHROMA DEFLECTION**

**DESCRIPTION**

The M52025SP is a semiconductor integrated circuit for video, chroma, and deflection signal processing. Combined with IC component M51496P for VIF/SIF, it realizes practical color television using only two IC components. Circuit configuration includes built-in sync separation, horizontal AFC, horizontal oscillator, horizontal count-down, vertical count-down, contrast control, luminance control, picture quality control, ACC/killer detector, ident detector, APC detector, chroma oscillator, NTSC tint control, and chroma demodulator functions.

**FEATURES**

- PAL / NTSC / SECAM multi-system processing can be realized by adding IC component M52026SP for processing SECAM chroma signals.
- Large-scale, single-chip construction enhances practicality and reliability of the television set itself while contributing to lower power consumption.
- Places of adjustment and number of external components are minimized.
- NTSC system switch enables construction of a PAL/NTSC system with a minimal amount of peripheral components. (Switches demodulator axis, demodulation ratio, PAL matrix, and tint control.)
- Employs a sync detector system for ACC/killer detector; realizes superior weak electric field killer level.
- Double AFC in the horizontal circuit effectively reduces weak electric field horizontal "jitter," and "bending" on the screen is minimized thanks to luminance alteration. Sync sensor circuit can be used as a sensor signal for sound muting, automatic channel selection, etc.
- Contains built-in service switch. (Contrast minimum killer ON, vertical output OFF)
- No vertical blanking for -Y output

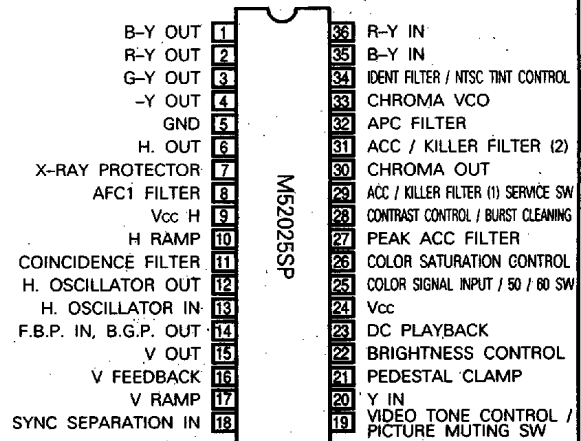
**APPLICATION**

PAL/SECAM Dual, PAL/NTSC System Color Television Receiver

**RECOMMENDED OPERATING CONDITION**

Supply voltage range ..... 10.0~12.5V (Pin 24)  
 Rated supply voltage ..... 11V (Pin 24)  
 Rated supply Current ..... 33mA (Pin 9)

**PIN CONFIGURATION (TOP VIEW)**

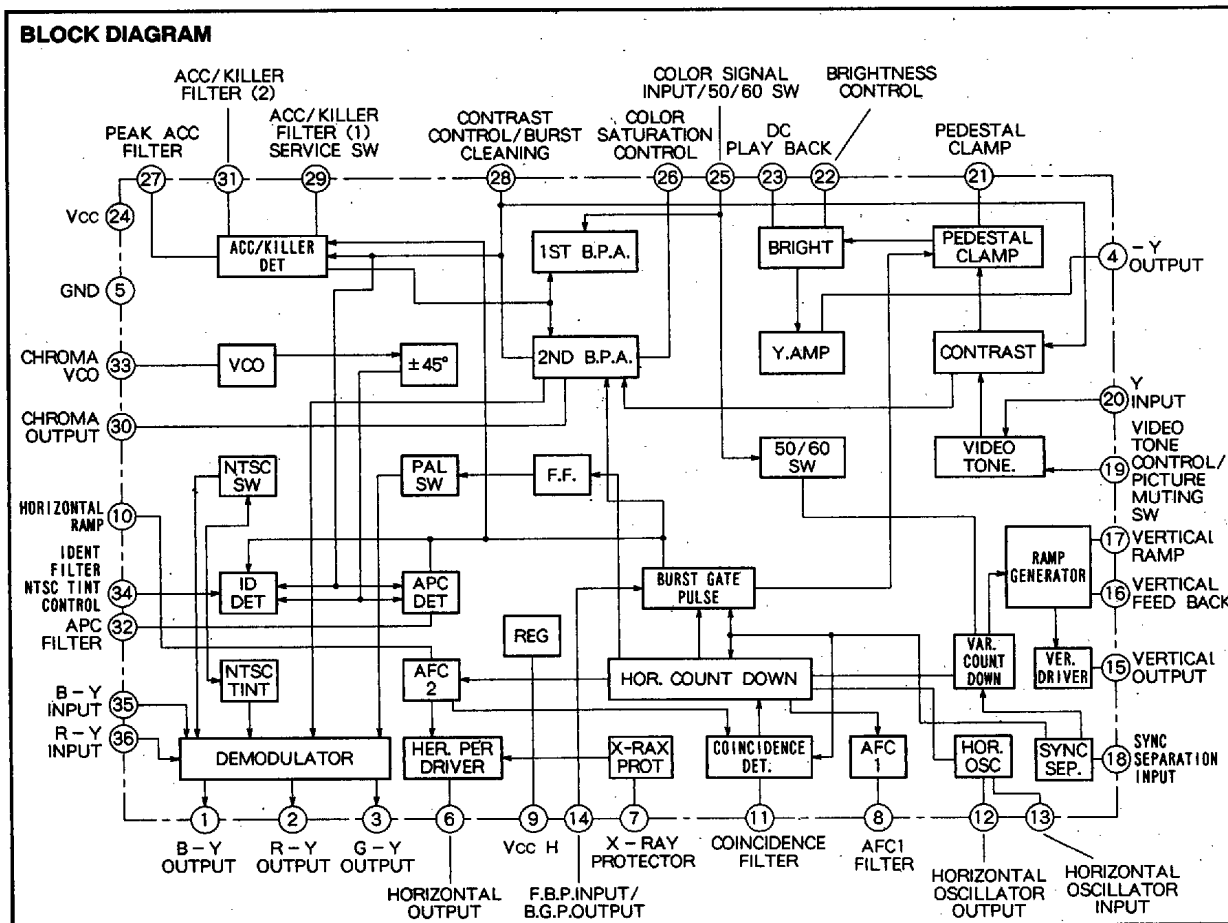


Outline 36P4E



PAL/NTSC VIDEO CHROMA DEFLECTION

**BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Ratings	Unit
V <sub>cc</sub>	Supply voltage	13.5	V
P <sub>d</sub>	Power dissipation	1.25	W
Surge	Surge voltage resistance	± 200	V
V <sub>16</sub>	Pin ⑮ voltage	0.28V <sub>cc</sub> + 6	V
I <sub>17</sub>	Pin ⑰ input current	+ 6	mA
I <sub>14</sub>	Pin ⑭ input current	- 1.0	mA
T <sub>opr</sub>	Operating temperature	- 20~65	°C
T <sub>stg</sub>	Storage temperature	- 40~125	°C

**M52025SP**

**PAL/NTSC VIDEO CHROMA DEFLECTION**

**ELECTRICAL CHARACTERISTICS** (Ta = 25°C, unless otherwise noted)

**VIDEO SECTION**

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
Icc - YC	Circuit current		46	60	74	mA
Ymax	Maximum output		6.9	8.0		V <sub>P-P</sub>
GY	Video amplifier gain		18	21	24	dB
GYmid	Contrast control characteristics - 1		0.65	0.95	1.35	V <sub>P-P</sub>
GYmin	Contrast control characteristics - 2			-39	-29	dB
GYmax	Contrast control characteristics - 3		4.3	7.3	10.3	dB
YTmid	Video tone control characteristics-1		0.95	1.35	1.85	V <sub>P-P</sub>
YTmin	Video tone control characteristics-2		-11	-8	-5	dB
YTmax	Video tone control characteristics-3		1.6	4.6	7.6	dB
YBRTmid	Brightness control characteristics-1		3.4	4.0	4.6	V
YBRTmin	Brightness control characteristics-2		7.4	8.0	8.6	V
YBRTmax	Brightness control characteristics-3			0.8	1.4	V
Yf	Frequency characteristics		-2	2	6	dB
H.BLKTH	Horizontal blanking threshold voltage		8.9	9.5	10.1	V

**CHROMA SECTION**

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
Cmax	Maximum output		1.6	2.2	2.8	V <sub>P-P</sub>
GC	Chroma maximum gain		35	40	45	dB
Acc1	ACC characteristics - 1		-8	-2.5	0	dB
Acc2	ACC characteristics - 2		-2	0.4	3	dB
KIL	Killer operation input		-34	-28	-22	dB
D.KIL	Killer color residual				200	mV <sub>P-P</sub>
CCmid	Color control characteristics - 1		0.65	0.95	1.35	V <sub>P-P</sub>
CCmin	Color control characteristics - 2			-40	-36	dB
CCmax	Color control characteristics - 3		5	9	13	dB
UCmid	Color tracking characteristics - 1		0.45	1.1	1.75	V <sub>P-P</sub>
UCmin	Color tracking characteristics - 2			-40	-36	dB
UCmax	Color tracking characteristics - 3		1	5	8	dB
APC1	APC pull - in range - 1		500	900		Hz
APC2	APC pull - in range - 2		870	1500		Hz
Ddc	Demodulated output DC voltage		5.9	6.4	6.9	V
Doffset	Demodulated output DC offset				0.3	V
Dmax	Demodulated output maximum amplitude		5.5	6.5	7.5	V <sub>P-P</sub>
DB-Y	B - Y demodulated sensitivity		2.5	3.0	3.5	V <sub>P-P</sub>
R/B	Demodulation ratio - 1		0.53	0.60	0.67	-
G/B	Demodulation ratio - 2		0.30	0.36	0.42	-
V23	Pin ⊗ voltage (killer ON)			0.13	1.00	V
NTSC B	Demodulated output (NTSC)		2.25	3.25	4.55	V <sub>P-P</sub>
NTSC R/B	Demodulation ratio - 1 (NTSC)		0.60	0.70	0.80	-
NTSC G/B	Demodulation ratio - 2 (NTSC)		0.20	0.31	0.36	-
Dbw	Demodulated output bandwidth		0.8	1.0		MHz
CD	Chroma input dynamic range		1.0	1.4		V <sub>P-P</sub>
∠R-Y-P	PAL demodulated phase angle			90		deg.
∠R-Y-N	NTSC demodulated phase angle			100		deg.
Tmin	NTSC TINT		27	-47	67	deg.
Tmax			20	+40	60	deg.

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**DEFLECTION SECTION**

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
Icc - D	Circuit current		26	35	44	mA
Vemin	Horizontal oscillator starting voltage			6	7.2	V
fH	Horizontal free run frequency		15.45	15.625	15.8	kHz
fPHIL	Horizontal pull - in range - 1			- 970	- 600	Hz
fPHIH			+ 550	+ 900		Hz
VgH	Coincidence detection maximum voltage		8.5	9.1		V
VgL	Coincidence detection minimum voltage				0.5	V
$\tau$ H	Horizontal output pulse amplitude		22	25	28	$\mu$ sec
VHmin	Horizontal output voltage			0.04	0.16	V
VHmax			3.1	3.9	4.8	V
tGP	Burst gate pulse position		4.1	5.0	5.9	$\mu$ sec
fv50	Vertical free run frequency 50 (Hz)		45.6	47	48.6	Hz
fv60	Vertical free run frequency 60 (Hz)		52.7	55	57.2	Hz
fpv50	Vertical pull - in range 50 (Hz)		54	55.7	58	Hz
fpv60	Vertical pull - in range 60 (Hz)		65	66.3	69	Hz
$\tau$ v50	Vertical output pulse amplitude 50 (Hz)		474	544	614	$\mu$ sec
$\tau$ v60	Vertical output pulse amplitude 60 (Hz)		474	544	614	$\mu$ sec
Vvmax	Vertical output maximum voltage		3.2	4.2		Vo - P
Vvmin	Vertical output minimum voltage				0.3	V
PRamp	Ramp peak voltage		5.6	6.05	6.5	V
VRamp	Ramp amplitude		1.5	1.8	2.1	Vp - P
GvV	Vertical open loop gain		16	20	24	dB
Iss	Sync separation input sensitivity current		0.07	0.1	0.15	mA
TBGP1	Burst gate pulse timing - 1		0.35	0.5	0.7	$\mu$ sec
TBGP2	Burst gate pulse timing - 2		3.2	3.6	4.1	$\mu$ sec
VFBP	Flyback pulse clamp voltage		4.3	4.8	5.3	V
VGBP	Burst gate pulse voltage		9.5	10.0	10.5	V

**ELECTRICAL CHARACTERISTICS TEST METHOD****GY Video Amplifier Gain**

1. Test -Y output amplitude and make  $V_{C0}$  the testing value.
2.  $GY = 20 \times \log \frac{V_{C0} \text{ (mV}_{PP})}{200 \text{ (mV}_{PP})}$  (dB)

**GYmid Contrast Control Characteristics-1**

1.  $GY_{mid} = Y_{C0} \text{ (V}_{PP})$

**GYmin Contrast Control Characteristics-2**

1. Test -Y output amplitude and make  $V_{C1}$  the testing value.
2.  $GY_{min} = 20 \times \log \frac{V_{C1}}{V_{C0}}$  (dB)

**GYmax Contrast Control Characteristics-3**

1. Test -Y output amplitude and make  $V_{C2}$  the testing value.
2.  $GY_{max} = 20 \times \log \frac{V_{C2}}{V_{C0}}$  (dB)

**YTmid Video Tone Control Characteristics-1**

1. Test -Y output amplitude and make  $V_{T0}$  the testing value.
2.  $YT_{mid} = V_{T0} \text{ (V}_{PP})$

**YTmid Video Tone Control Characteristics-2**

1. Test -Y output amplitude and make  $V_{T1}$  the testing value.
2.  $YT_{min} = 20 \times \log \frac{V_{T1}}{V_{T0}}$  (dB)

**YTmax Video Tone Control Characteristics-3**

1. Test -Y output amplitude and make  $V_{T2}$  the testing value.
2.  $YT_{max} = 20 \times \log \frac{V_{T2}}{V_{T0}}$  (dB)

**Y<sub>arr</sub>mid Brightness Control Characteristics-1**

1. Test -Y output DC voltage.

**Y<sub>arr</sub>min Brightness Control Characteristics-2**

1. Same as Y9.

**Y<sub>arr</sub>max Brightness Control Characteristics-3**

1. Same as Y9.

**Y<sub>f</sub> Frequency Characteristics**

1. Test -Y output amplitude.
2. Make  $V_{f1}$  the amplitude when SG2 is input.
3. Make  $V_{f2}$  the amplitude when SG4 is input.
4.  $Y_f = 20 \times \log \frac{V_{f2}}{V_{f1}}$  (dB)

**DG Differential Gain**

1. Test -Y output DC voltage.
2. Make  $V_{G1}$  the amplitude when ② is set to 2.4V.
3. Make  $V_{G2}$  the amplitude when ② is set to 1.8V.
4.  $DG = \frac{|V_{G1} - V_{G2}|}{V_{G2}} \times 100$  (%)

**H. BLK TH Horizontal Blanking Threshold Voltage**

1. Apply voltage to pin ④ and increase from 8V.
2. Test the voltage of pin ④ when signal ceases to be output by ①A.

**GC Chroma Maximum Gain**

1. Test output amplitude (P-P) and make  $V_{Gc}$  the testing value.
2.  $GC = 20 \times \log \frac{V_{Gc} \text{ (mV}_{PP})}{\text{Input Amplitude (}\approx 7.94\text{mV}_{PP})}$  (dB)

**ACC 1 ACC Characteristics-1**

1. Test output amplitude (P-P).
2. Make  $V_{A0}$  the testing value when SG5 0dB is input.
3. Make  $V_{A1}$  the testing value when SG5 -22dB is input.
4.  $ACC 1 = 20 \times \log \frac{V_{A1}}{V_{A0}}$  (dB)

**ACC 2 ACC Characteristics-2**

1. In the same manner as in C3, make  $V_{A2}$  the testing value when SG5 +6dB is input.
2.  $ACC 2 = 20 \times \log \frac{V_{A2}}{V_{A0}}$  (dB)

**KIL Killer Operation Input**

1. Gradually attenuate the level of SG5.
2. While monitoring DC voltage of pin ⑥, input level of SG5 when voltage becomes less than 1V.

**D. KIL Killer Color Residual**

1. Test output amplitude within 1H interval.

**CCmid Color Control Characteristics-1**

1. Test output amplitude (P-P) and make  $V_{C10}$  the testing value.
2.  $CC_{mid} = V_{C10} \text{ (V}_{PP})$

**CCmin Color Control Characteristics-2**

1. Test output amplitude (P-P) and make  $V_{C11}$  the testing value.
2.  $CC_{min} = 20 \times \log \frac{V_{C11}}{V_{C10}}$  (dB)

**CCmax Color Control Characteristics-3**

1. Test output amplitude (P-P) and make  $V_{C12}$  the testing value.
2.  $CC_{max} = 20 \times \log \frac{V_{C12}}{V_{C10}}$  (dB)

**UCmid Color Tracking Characteristics-1**

1. Test output amplitude (P-P) and make  $V_{U0}$  the testing value.
2.  $UC_{mid} = V_{U0} \text{ (V}_{PP})$

**UCmin Color Tracking Characteristics-2**

1. Test output amplitude (P-P) and make  $V_{U1}$  the testing value.
2.  $UC_{min} = 20 \times \log \frac{V_{U1}}{V_{U0}}$  (dB)

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**UCmax Color Tracking Characteristics-3**

1. Test output amplitude (P-P) and make  $V_{U2}$  the testing value.
2.  $UC_{max} = 20 \times \log \frac{V_{U2}}{V_{U0}}$  (dB)

**APC 1 APC Pull-In Range-1**

1. Set so that the frequency of SG6 is less than 4.433MHz and pin ② is Lo.
2. Gradually increase the frequency of SG6.
3. Test the frequency when the voltage of pin ② changes from Lo to Hi and make  $F_{Au}$  the testing value.
4.  $APC 1 = 4433619$  (Hz) -  $F_{Au}$  (Hz)

**APC 2 APC Pull-In Range-2**

1. Set so that the frequency of SG6 is more than 4.434MHz and pin ② is Lo.
2. Gradually decrease the frequency of SG6.
3. Test the frequency when the voltage of pin ② changes from Lo to Hi and make  $F_{Ad}$  the testing value.
4.  $APC 2 = F_{Ad}$  (Hz) - 4433619 (Hz)

**Ddc Demodulated Output DC Voltage**

1. Test DC voltage at ①A, ②A and ③A.

**Dffset Demodulated Output DC Offset**

1. Calculate each voltage difference of, ①A②A, ②A③A and ③A①A from the testing value of C15.

**R/B Demodulation Ratio-1**

1. Test output amplitude and make  $D_{R-Y}$  the testing value.
2.  $R/B = \frac{D_{R-Y}}{D_{B-Y}}$  (Testing Value at C18)

**G/B Demodulation Ratio-2**

1. Test output amplitude and make  $D_{G-Y}$  the testing value.
2.  $G/B = \frac{D_{G-Y}}{D_{B-Y}}$  (Testing Value at C18)

**AD/H Demodulated Output 1H Level Difference**

1. Test both AC, DC for each 1H level difference.

**C leak Demodulated Output Carrier Leak**

1. Test output carrier element for 1A, 2A, and 3A.

**Vntsc NTSC Operation Control Voltage**

1. Gradually decrease voltage of 34A from the area of 8V.
2. Test the 34A voltage when signal ceases to be output by 1A.

**NTSC R/B Demodulation Ratio (NTSC)-1**

1. Test output amplitude and make  $NTSC_R$  the testing value.
2.  $NTSC R/B = \frac{NTSC_R}{NTSC_B}$  (Testing Value at C25)

**NTSC G/B Demodulation Ratio (NTSC)-2**

1. Test output amplitude and make  $NTSC_G$  the testing value.
2.  $NTSC G/B = \frac{NTSC_G}{NTSC_B}$  (Testing Value at C25)

**V P/N PAL/NTSC Demodulated Output DC Voltage Difference**

1. Test the difference in DC voltage when S34 is ON and when it is OFF.

**SS Service Switch Operation**

1. No output signal from ④
2. No vertical sync pulse from ⑤
3. Voltage of ⑥ drops below 1V.
4. Check 1, 2 and 3.

**Dsw Demodulated Output Bandwidth**

1. Set frequency of SG8 to 4.5MHz, and test output amplitude of ①, ② and ③.
2. Gradually increase the frequency of SG8.
3. Test output frequency of ①, ② and ③ when output amplitude is 3dB less than when 4.5MHz is input.

**CD Chroma Input Dynamic Range**

1. Increase the level of SG5 and test the input amplitude when output becomes distorted.

**∠R-Y-P, ∠G-Y-P PAL Demodulated Phase Angle**

1. Make ∠R-Y-P the phase difference of ①A ②A.
2. Make ∠G-Y-P the phase difference of ①A ③A.

**∠R-Y-N, ∠G-Y-N NTSC Demodulated Phase Angle**

1. Make ∠R-Y-N the phase difference of ①A ②A.
2. Make ∠G-Y-N the phase difference of ①A ③A.

**Tmin, Tmax NTSC Tint**

1. Set oscilloscope to X-Y. Connect ①A to X and ②A to Y.
2. Open ④ and set SG6 frequency to 4.433619MHz.
3. At this time the oscilloscope waveform is shown as 180°.
4. Make Tmin the remainder of subtracting 180° from the angle when ④ was set to 4V.
5. Make Tmax the remainder of subtracting 180° from the angle when ④ was set to 1V.

**Horizontal Oscillator Starting Voltage**

1. Increase ④ from 0V.
2. Test ④ voltage where the output waveform cycle of ⑥ is approx. 64μs.

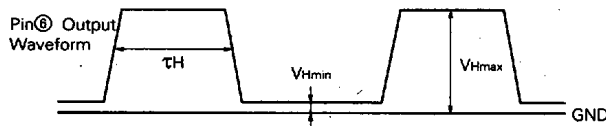
**fPHIL, fPHIH Horizontal Pull-In Range-1**

1. Decrease the frequency of input signal so that the SGB input signal and pin ⑥ output waveform are not synchronized.
2. Increase the frequency of SGB.
3. Test the SGB frequency when SGB and pin ⑥ output waveform become synchronized and make  $f_{L1}$  the testing value.

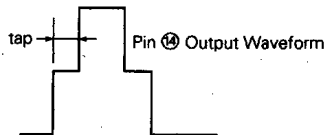
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4.  $f_{PH1L} = f_{L1} - f_H$  (Testing Value at J3)
5. Test the upper side pull-in in the same manner and make  $f_{H1}$  the SGb frequency when the two become synchronized.
6.  $f_{PH1H} = f_{H1} - f_H$  (Testing Value at J3)

**$\tau_H$  Horizontal Output Pulse Amplitude**  
 **$V_{Hmin}$ ,  $V_{Hmax}$  Horizontal Output Voltage**



**$t_{BGP}$  Burst Gate Pulse Position**



**$f_{PV}$  50 Vertical Pull-In Range 50 (Hz)**

1. Increase the frequency of input signal so that the SGc input signal and pin 15 output waveform are not synchronized.
2. Decrease the frequency of SGc and test the SGc frequency when SGc and the output waveform of pin 15 become synchronized.

**$f_{PV}$  60 Vertical Pull-In Range 60 (Hz)**

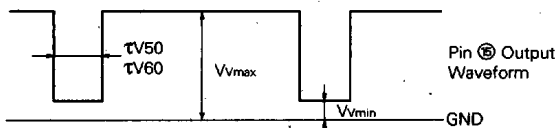
1. Same as J12.

**$\tau_{V50}$  Vertical Output Pulse Amplitude 50 (Hz)**

**$\tau_{V60}$  Vertical Output Pulse Amplitude 60 (Hz)**

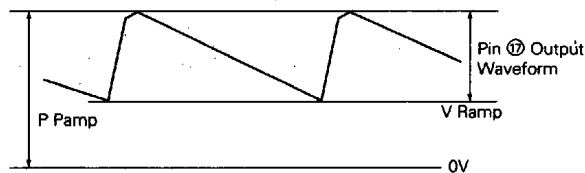
**$V_{Vmax}$  Vertical Output Maximum Voltage**

**$V_{Vmin}$  Vertical Output Minimum Voltage**



**P Ramp Ramp Peak Voltage**

**V Ramp Ramp Amplitude**



**$G_{Vv}$  Vertical Open Loop Gain**

1. Test the output amplitude of pin 16 and make  $V_{Vo}$  the testing value.

$$2. G_v = 20 \times \log \frac{V_{Vo} \text{ (mVPP)}}{\text{Input Amplitude (=50mVPP)}} \text{ (dB)}$$

**$I_{SS}$  Sync Separation Input Sensitivity Current**

1. Increase  $I_s$  from 0 mA.
2. Test  $I_s$  when burst gate pulse ceases to be output by 14.

**$t_{BGP}$  1 Burst Gate Pulse Timing-1**

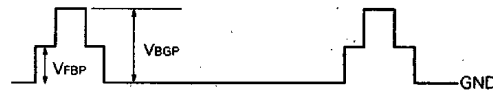
1. Test the time from SGa rise to burst gate pulse rise.

**$t_{BGP}$  2 Burst Gate Pulse Timing-2**

1. Test burst gate pulse amplitude.

**$V_{FBP}$  Flyback Pulse Clamp Voltage**

**$V_{BGP}$  Burst Gate Pulse Voltage**



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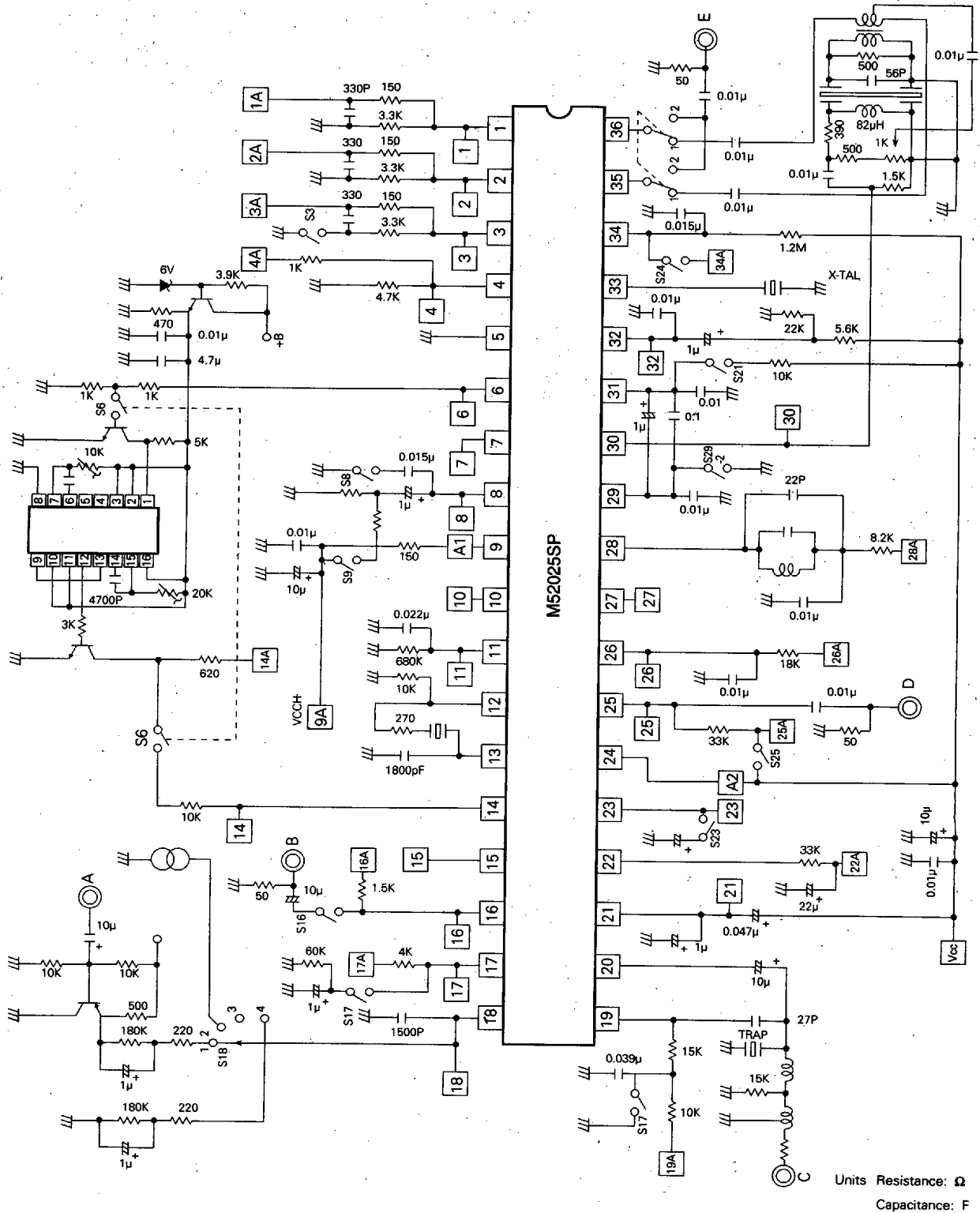
INPUT SIGNAL

SG No.	Signals		
SG 1	100 kHz	CW	3 V <sub>P-P</sub>
SG 2	100 kHz	CW	200 mV <sub>P-P</sub>
SG 3	2 MHz	CW	200 mV <sub>P-P</sub>
SG 4	5 MHz	CW	200 mV <sub>P-P</sub>
SG 5	<p>PAL Simple Chroma Signal</p> <p>0 db 50mV<sub>p-p</sub> 100mV<sub>p-p</sub></p> <p>Burst Chroma Burst Chroma</p> <p>1H<sub>(n)</sub> 1H<sub>(n+1)</sub></p> <p><math>f_{ab(m)} = f_{ac(m)} = 4.433619\text{MHz}</math> (Same Phase)</p> <p>The phase correlation between the about signals is outlined in the figure on the right. The phase correlation with burst of <math>e_c(n)</math> and <math>e_c(n+1)</math> does not always have to be as shown in the figure on the right, and in particular must be adjustable according to conditions when testing phase correlation.</p>		
SG 6	With PAL simple chroma signals for SG5, the phase of burst and chroma signals should be the same and the frequency should be adjustable.		
SG 7	4.42 MHz	CW	0.2~0.5 V <sub>P-P</sub>
SG 8	4~6 MHz	CW	
SG 9	$f_{sb}$ (Burst) = 4.433619 MHz, $f_{sc}$ (Chroma) = 4.53 MHz at SG5.		
SG a	<p>Input for sync separation should be APL 100% standard combined image signal 1.5 V<sub>P-P</sub> for PAL system such as illustrated by the figure on the right.</p>		
SG b	<p>2V<sub>pp</sub> Duty 90%</p>		
SG c	<p>2V<sub>pp</sub> Duty 95%</p>		
SG d	2 kHz, CW; 500 mV <sub>P-P</sub> = 0 dB		

# M52025SP

## PAL/NTSC VIDEO CHROMA DEFLECTION

### TEST CIRCUIT



M52025SP



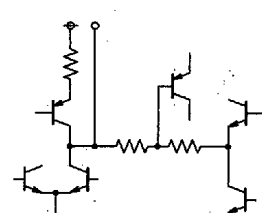
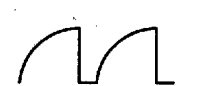
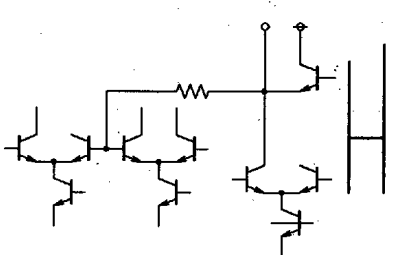
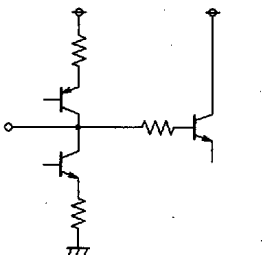

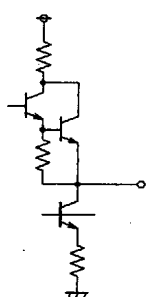
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DESCRIPTION OF PIN

Pin No.	Name	Description	Peripheral circuit of pins	DC voltage(V)
① ②	B-Y output R-Y output	<ul style="list-style-type: none"> <li>• Chroma output B - Y</li> <li>R - Y</li> </ul>		6.4
③	G-Y output	<ul style="list-style-type: none"> <li>• Chroma output G - Y</li> <li>• If color tracking switch external resistor (emitter resistor) is removed, color tracking is ineffectual.</li> </ul>		6.4
④	-Y output	<ul style="list-style-type: none"> <li>• -Y output</li> <li>• Horizontal blanking input</li> </ul>		—
⑤	GND	—	—	0
⑥	Horizontal output	<p>Approx. 4V 0V</p> <p>25 <math>\mu</math> sec</p> <p>Horizontal pre - driver output</p>		—
⑦	X - RAY protector	X - RAY protector is actuated when pin voltage exceeds approx. 0.75V.		—


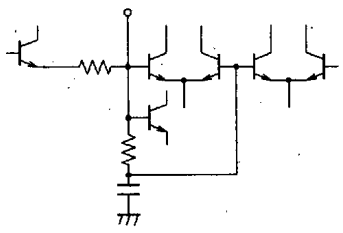
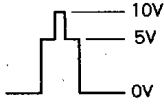
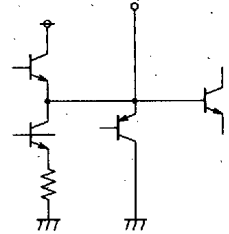
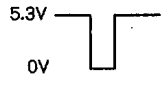
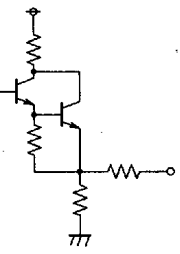
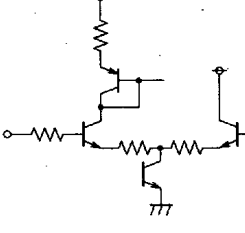
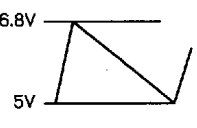
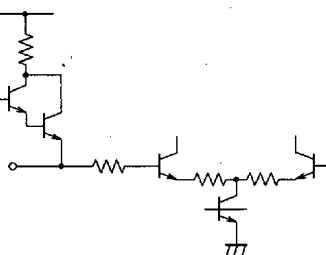
PAL/NTSC VIDEO CHROMA DEFLECTION

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Description	Peripheral circuit of pins	DC voltage(V)
⑧	AFC1 filter	 <p>When VCO frequency becomes high filter voltage decreases causing VCO frequency to drop. Operates oppositely when frequency becomes high.</p> 		6.6
⑨	Vcc H	Built-in regulator	—	10
⑩	Horizontal ramp	 <p>Generates horizontal ramp. Horizontal output pulse is created according to this ramp.</p>		—
⑪	Coincidence detection filter	High when horizontal SYNC and horizontal output are synchronized, low when not synchronized.		Low 0.2 High 9.1
⑫	Horizontal oscillator output	 <p>f = approx. 500kHz Output to external phase shifter.</p>		9.5

PAL/NTSC VIDEO CHROMA DEFLECTION

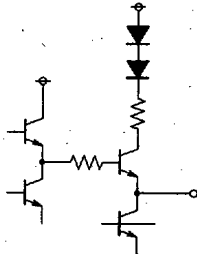
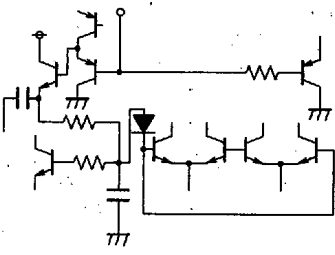
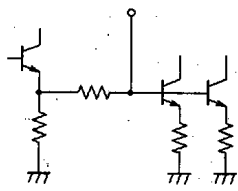
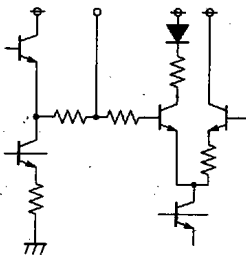
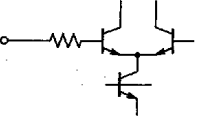
DESCRIPTION OF PIN (cont.)

Pin No.	Name	Description	Peripheral circuit of pins	DC voltage(V)
13	Horizontal oscillator input	 f = approx. 500kHz Output to external phase shifter.		5.2
14	F.B.P. input/ B.G.P. output	4.3 μ sec  B.G.P. and F.B.P. output as sand castle.		—
15	Vertical output	 5.3V 0V		—
16	Vertical return	AC/DC return input pin		—
17	Vertical ramp	 6.8V 5V Vertical ramp generation		—



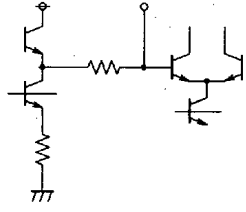
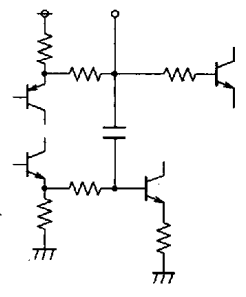
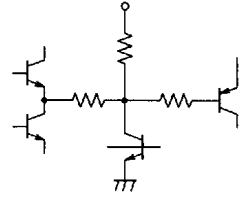
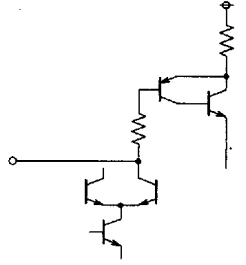
PAL/NTSC VIDEO CHROMA DEFLECTION

DESCRIPTION OF PIN (cont.)

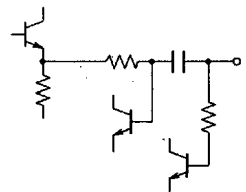
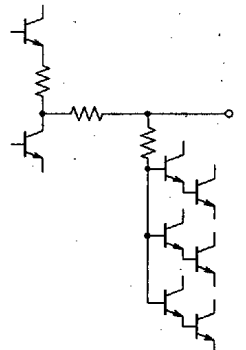
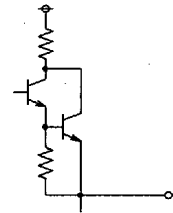
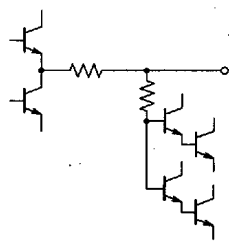
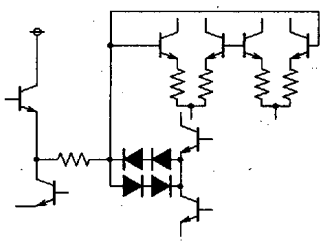
Pin No.	Name	Description	Peripheral circuit of pins	DC voltage(V)
18	Sync separation input	Sync separation of emitter input		8.4
19	Picture quality control/picture muting switch	<ul style="list-style-type: none"> <li>Picture quality control High-pass increases as pin voltage is decreased.</li> <li>Picture muting If voltage is less than 2V, picture muting is actuated and -Y output becomes BLK level.</li> <li>Built-in buffer</li> </ul>		—
20	Y input	Y signal input		1.3
21	Pedestal clamp	Pedestal DC voltage of -Y output is determined by this clamp voltage.		2
22	Luminance control	Luminance control Becomes brighter as voltage is increased.		—

PAL/NTSC VIDEO CHROMA DEFLECTION

DESCRIPTION OF PIN (cont.)

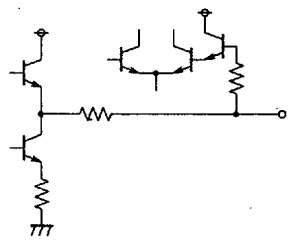
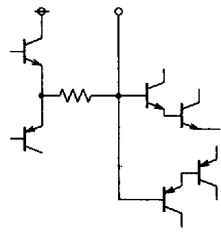
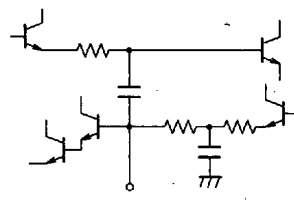
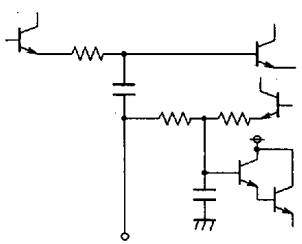
Pin No.	Name	Description	Peripheral circuit of pins	DC voltage(V)
⑫	DC playback	DC playback ratio can be changed by external CR. 100% when open.		—
⑭	Vcc	—	—	11
⑮	Color signal input 50/60 SW	<ul style="list-style-type: none"> <li>• Chroma input</li> <li>• 50/60 switching</li> </ul> Vertical countdown toggles between 50Hz and 60Hz. When voltage exceeds 5.6V, toggles to 60Hz.		2.7
⑯	Color saturation control	Changes amplitude of chroma output.		—
⑰	Peak ACC filter	Gain of chroma amp is controlled by this filter in order to maintain a constant chroma amplitude.		—

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Description	Peripheral circuit of pins	DC voltage(V)
⑳	Contrast control/ burst cleaning	Burst cleaning Coil connection contrast control Changes amplitude of -Y output. Amplitude increases as voltage is increased.		—
㉑	ACC/ killerfilter (1) / service switch	Sync ACC/killer filter ACC and killer are operated according to voltage differential between this pin and pin ㉒. When this pin is connected to GND, the service switch is ON. (Vertical stop and contrast MIN. killer ON.)		7.3
㉒	Chroma output	PAL system ACC chroma signals are output. NTSC system Low DC chroma signals are output.		7.1 4.2
㉓	ACC/killer filter (2)	Sync acc/killer filter ACC and killer are operated according to voltage differential between this pin and pin ㉑.		7.3
㉔	APC filter	Chroma VCO phase is controlled by this voltage in order to check burst.		9.1

PAL/NTSC VIDEO CHROMA DEFLECTION

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Description	Peripheral circuit of pins	DC voltage(V)
⑤	Chroma VCO	Generates carrier for chroma.		8
⑥	Ident filter NTSC tint control	PAL system Functions as ident filter. When voltage drops below reference voltage, F.F. is stopped. NTSC system (less than 5V) Tint control is carried out at 2~4V. If NTSC switch is less than 5V, switches to NTSC mode.		8
⑦	B-Y input	PAL system Synthesized B-Y chroma signal input		6
⑧	R-Y input	PAL system Synthesized R-Y chroma signal input		2